Extreme Environment Capable, Modular and Scalable Power Processing Unit for Solar Electric Propulsion

Gregory A. Carr¹, Christopher J. Iannello², Yuan Chen³, Don J. Hunter¹, Linda Del Castillo¹, Arthur T. Bradley³, Christopher Stell¹, Mohammad M. Mojarradi¹

¹Jet Propulsion Laboratory, California Institute of Technology, Pasadena, CA 91109
²NASA Kennedy Space Center, Cocoa Beach, FL 32899
³NASA Langley Research Center, Hampton, VA 23681

Abstract — This paper is to present a concept of a modular and scalable High Temperature Boost (HTB) Power Processing Unit (PPU) capable of operating at temperatures beyond the standard military temperature range. The various extreme environments technologies are also described as the fundamental technology path to this concept. The proposed HTB PPU is intended for power processing in the area of space solar electric propulsion, where reduction of in-space mass and volume are desired, and sometimes even critical, to achieve the goals of future space flight missions. The concept of the HTB PPU can also be applied to other extreme environment applications, such as geothermal and petroleum deep-well drilling, where higher temperature operation is required.

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1. INTRODUCTION

High power solar electric propulsion systems are required for NASA’s next generation deep space and manned missions. A formulation study, focused on the power processing unit of the solar electric propulsion system, is authorized and supported by the Game Changing Technology Division, NASA Office of the Chief Technologist. A concept of a modular, power scalable and extreme environment technology enabled High Temperature Boost (HTB) Power Processing Unit (PPU) has been proposed [1].

The concept relies on the new approaches applied in system and topology designs and operating the HTB PPU at a higher junction temperature of 160°C, which can only be realized with the emerging extreme environments technologies. It should be noted that, unlike other extreme environment applications where the operating temperatures are beyond military temperature range, such as geothermal and petroleum deep-well drilling, the solar electric propulsion system does not need to operate at higher temperatures. However, by using and taking advantage of the emerging extreme environment technologies, our preliminary analysis indicates that the high temperature operation of the proposed HTB PPU based on the new design has shown a factor of five improvement in PPU specific power/mass, a factor of ten improvement in the specific power/mass of the high power anode discharge unit within the PPU, and over 30% in-space solar electric mass saving for the overall system.

This is one example where the new extreme environment technologies provide the critical path to the next generation power processing for both conventional and extreme temperature environments, not only in space missions but also in other applications.

This paper details the concept of the HTB PPU, including its enabling extreme environment electronics (Section 2), the new approaches on system architecture and power conversion topology (Section 3), as well as the modularity and scalability, which includes advanced system and device packaging (Section 4). A number of applications of the concept are outlined in Section 5 and a summary is provided in Section 6.

2. EXTREME ENVIRONMENT ELECTRONICS

The proposed HTB PPU was designed for operation at an expected maximum junction temperature of 160°C, based on the system design detailed in Section 4. The enabling extreme environment technologies, therefore, include high temperature active and passive technology as well as high temperature packaging technology. The high temperature packaging technology is included along with the system packaging in Section 4. This Section focuses on the active and passive technologies for this extreme environment application.

SiC Technology

In general, Silicon Carbide (SiC) and Gallium Nitride (GaN) technologies are the two most promising and matured technologies for high temperatures, each having its advantages and disadvantages over the other for different applications. GaN devices are being used for lower power/voltage and high frequency applications, while SiC devices are being used for high power and high voltage switching power applications. SiC technology, including power MOSFETs and diodes, were therefore chosen for this concept.

Theoretical appraisals have indicated that SiC power
MOSFET’s and diode rectifiers would operate over higher voltage and temperature ranges, have superior switching characteristics, and yet have die sizes nearly twenty times smaller than correspondingly rated silicon-based devices [2-4]. These tremendous theoretical advantages have yet to be widely realized in commercially available SiC devices, primarily owing to the fact that SiC’s relatively immature crystal growth and device fabrication technologies are not yet sufficiently developed to the degree required for reliable incorporation into most electronic systems. For high-temperature and high-power system applications, MOSFETs and IGBTs are strongly preferred, largely because the MOS gate drives are insulated from the conducting power channel, require little drive signal power, and the devices are Normally Off in that there is no current flow when the gate is unbiased at zero V. The performance and reliability of the SiC-based MOS field effect gates has long been limited by poor inversion channel mobility and questionable gate-insulator reliability; however, over the past three years, the reliability of SiC MOSFETs has shown a significant improvement [5].

There are a number of SiC based sensors and actuators developed by NASA Glenn Research Center, which are very well documented [6].

Even though SiC diodes have been commercially available from various manufacturers for years, SiC transistor availability has been the key condition to visualizing significant market growth during the past couple of years.

Cost issues have slowed down SiC penetration into its target markets. In a Yole Development report released in late 2009 [7], only ~4% of the overall Silicon-based power discrete market was forecasted to be displaced by SiC in 2019. The report was based on the observation that no switch had reached large volume production yet and the car makers were still improving silicon IGBT technology, indicating that “power electronic industry is still waiting for a SiC transistor and expects its release in 2010”.

2011 is the year of the first SiC JFET and MOSFET introduction with simultaneous offers from SemiSouth, Rohm and CREE. A 2011 Yole Development report announced that “SiC market is now a real industry, not a niche anymore” [8]. SiC device manufacturers now offer both diode and transistor devices in the power electronics industry, and significant effort is being directed toward the packaging side to capture all the added-value of the SiC such as high temperature and high frequency.

In February 2011, SemiSouth Laboratories, Inc., announced that it had started shipping its vertical trench JFETs in commercial volume quantities [9]. SemiSouth utilizes a self-aligned JFET chip design enabling up to ten times smaller die size when compared to silicon super-junction MOSFETs or the latest trench IGBTs. It has three families: Normally-OFF, Normally-ON and Normally-Off for audio. Its Normally-Off trench SiC power JFETs, i.e., SJEP120R100, SJEP120R063 and SJEP170R550, offer a blocking voltage of either 1200V or 1700V, and exhibit temperature-independent switching behavior. The SJEP120R100 with an on-resistance of 100mΩ enables fast switching with no ‘tail’ current up to its maximum operating temperature of 175°C, and the SJEP120R063, with an on-resistance of 63 mΩ, can enable switch losses of 356µJ at 24A. Its newest Normally-Off SiC JFET is its 1700V and 4A SJEP170R550 which delivers an on-resistance of 550mΩ and an output capacitance of 20pF. SemiSouth also offers two Normally-On 1200V SiC JFETs, i.e., SJD120R085 and SJD120R085, both with the same switching performance and a saturation current of 50A, and on-resistance per unit area of 85mΩ and 45 mΩ total, respectively. All the JFETs are in TO-247 packages.

In May 2011, Cree, Inc. announced its new 1200V SiC MOSFET family, i.e., Z-FET™ CMF10120D and Z-FET™ CMF20120D, with 12A at its operating temperature of 100°C, a blocking voltages up to 1200V, and an on-resistance of 160mΩ or 80 mΩ at 25°C [10]. This reduces switching losses in many applications by up to 50 percent, increasing overall system efficiencies up to 2 percent while operating at 2 – 3 times the switching frequencies when compared to the best silicon IGBTs. As a result of this improved efficiency, SiC devices have lower operating temperatures and fewer thermal management requirements, which combine with their ultra-low leakage current (<1µA) to reduce system size and weight while increasing reliability.

The SiC transistors, including JFET and MOSFET, are also available from a couple of other manufacturers by contacting the manufacturer directly. For example, ROHM is developing SiC MOSFETs, including SiC MOSFET SCU 210AX(N) with 600V block voltage and TO-220FM package, and SCU220KE(N) with 120V block voltage and TO-247 package [11].

**Passives**

Availability of passive components designed or specified for use at high temperatures is generally limited. The behaviour of passive devices at elevated temperatures can be influenced by materials and design: however, suitability often depends on the required characteristics as a function of temperature and time. When high temperatures are coupled with high voltages for capacitors and high currents for inductors, the number of available long-life, high-value devices is further limited. In addition, significant derating of survivable components may result from power dissipation, current, voltage and operating life requirements, due to an increase in loss and a reduction in thermal conductivity. The resulting increase in internal temperature could destroy or reduce the lifetime of the devices. Finally, packaging and material degradation issues, such as degradation of plastic encapsulants/adhesives, melting of solders, fatigue and overstress failure of leads, could result in variation of device behaviour and possibly failure if the passive component is not properly designed [12, 13].

While some capacitors, which are stable at elevated temperatures, are commercially available, they are often
made of insulating materials with low dielectric constants and therefore have low energy densities. Commercially available capacitors made with higher dielectric constant insulators tend to exhibit unstable capacitance and high leakage currents at elevated temperatures. Therefore, the more stable low dielectric constant materials were selected. However, due to the low dielectric constant and significant derating required, the devices selected are quite large. Three companies capable of providing adequately sized and mechanically robust NP0 capacitors were identified. One additional company provided two different high temperature mica solutions.

For high temperature inductors, the performance and survivability at elevated temperatures is dependent upon the choice of materials, including the magnetic core material as well as the conductive and insulating materials for the windings. Standard transformer technologies are usable to 200°C \[12\]. To minimize the size and mass of this supply, planar magnetics may be feasible for low power, while fine powder cores based on MPP (Mo-Ni-Fe) and Sendust (Al-Si-Fe) with high temperature polymer insulated Cu wire conductors are being considered for the higher power components.

Robust, large sized wirewound resistors, made from heat resistant wire and ceramic, can be used well above 200°C and are simply limited by the degradation (loss of insulation resistance and fatigue fracture) of their vitreous enamel coatings, which perform well to 300°C. Discrete and embedded thick and thin film resistors provide the most miniaturized solutions for high temperature operation. Produced by deposition, patterning and oxidation (to form a protective coating layer) of thin metal films on silicon or ceramic substrates, thin film resistors provide high resolution, stability, high frequency performance, small size and low TCRs. Such resistors are most often made from tantalum, tantalum nitride, nickel chromium, titanium and cermets. Long term high temperature survivability is dependent upon the material used, but each of those mentioned is capable of operation above 200°C. The presence of oxygen may influence the aging of these materials. Thick film resistors are produced using proprietary ink formulations made from palladium, ruthenium, iridium and rhenium, with ruthenium silver, palladium silver and ruthenium oxide being the most often used resistive materials. Ruthenium oxide is resistant to degradation in air to 1000°C, and exhibits low TCR, good stability and low noise. Stresses generated at the interface between the substrate and the resistor due to CTE mismatches and thermal or power cycling remains a concern \[1, 12, 13\].

Embedded resistors are selected to be used on the ceramic substrates. Surface mount resistors designed for high temperature operations will be used for the printed circuit boards and where needed on the ceramic substrates.

### 3. Architecture and Power Conversion

The power processing unit for the solar electric propulsion system is shown in Figure 1 below. There are five modules within the power processing unit, i.e., Anode Discharge Power Module, Magnetic Supply Module, Cathode Supply Module, Control/Valve Drive/House Keeping Module, and Input/output Filter Module. The Anode Discharge Power Modules is a 10kW module with other modules relatively low power. It is the biggest challenge of the PPU and also benefits most from the extreme environments technologies.

**Figure 1. Solar Electric Propulsion system with HTB PPU and its five modules.**
An end-to-end system engineering approach was applied with a new design to extract the most value from the emerging high temperature semiconductor and packaging technology, and to achieve high temperature operation with non-isolated topology for high power and low specific mass.

System Architecture

Our approach to evaluating the overall system architecture is to break down component mass and power of the current state-of-the-art, which achieved TRL 9 in 2010. In evaluating the components of a Hall thruster system, we looked for areas where applying the new higher temperature technology could improve the overall performance. The power system is broken down into the Solar Array, Cabling, PMAD, PPU and the radiator for the PPU. The solar array has the lowest specific power, which greatly affects the sensitivity of the parameters that impact the size of the array. We looked at systems ranging in power from 10 to 320 kW. Although the current state of the art is in the range of 4.5 to 18 kW, we scaled the specific power of the different components to see the benefit at higher power levels.

The architecture goal of the HTB PPU is to reduce the end-to-end mass of the Solar Electric Propulsion system. Improving the specific power, increasing the efficiency and increasing the operating temperature of the PPU will achieve the goal of improving the system level performance.

The first parameter of the PPU in improving the system level performance is to focus on the specific power of the PPU. The PPU mass and volume can significantly impact the spacecraft configuration particularly when scaling up the power level to the order of 320 kW. The PPU design and packaging are keys to achieving a higher specific power resulting in higher performance at higher power levels.

One aspect of the design is to take advantage of the new higher temperature power devices that have higher operating voltages. By increasing the solar array voltage, the mass associated with carrying the high current for high power operation is lower. The high input voltage on the PPU design will reduce the mass in the PMAD and cabling.

A higher output voltage will enable the Hall thrusters to run at higher specific impulse, reducing the mass of the xenon to achieve the same amount of delta-V [14].

A simple power conversion topology for the Anode Power Supply will reduce the number of components that need to operate at higher temperature. With fewer components, the specific power will be dominated by the performance of the power devices and passive devices. The input and output voltages need to stay within the capability of the power technology to maintain a simple topology and fewer components. If the voltages exceed the capability of the technology, more components will be needed to either stack the power stage on the input or the outputs, resulting in lower specific power.

In evaluating different topologies, a key difference at the system level is whether the PPU anode power supply is isolated or not. Non-isolated topologies offer simplest designs with fewer components, but require system level compensation to balance the currents in the Cathodes when two or more thrusters are in operation. Without compensation, the total current of all thrusters will most likely flow through one Cathode, impacting the life of that component [15]. Active current sharing or ballast resistors can provide compensation with some impact in mass and power. An isolated topology will require more components, but not require current sharing compensation at the system level.

With a simple design for the Anode Power Supply, the packaging can be optimized for the high power components. The packaging design is dominated by the high power passive components that transfer the energy. The end result is an efficient high specific power packaging design. The architecture needs to be scalable to improve the performance for higher power thrusters and systems. An optimized package for the anode supply at 10 kW can scale with parallel power stages to higher power thrusters, maintaining the high specific power up to 80 kW without the penalty for redesign to accommodate different thruster power levels. The auxiliary functions outside the anode supply are not as sensitive to the power level of the thruster.

The efficiency of the anode power supply impacts the local performance of the PPU as well as the size of the solar array and radiator. The total system level mass is affected by 1.4% for the difference between 95% and 96% efficiency at the 10 kW level. This can be as high as 20kg per efficiency percentage point at 320 kW.

The final parameter of the PPU design that can improve the system level performance is the operating temperature. The current SOA PPU operates at a 50°C baseplate. As we increase the power at the system level, maintaining this temperature will require changes to the spacecraft configuration. At the same power level, if the PPU is able to operate at 100°C baseplate, the area of the radiator is cut by a factor of two. This could be a significant impact to the spacecraft configuration when scaling up to the 320 kW at the system level.

Power Conversion

Traditionally, the conventional conversion topology is the full bridge for this application’s power level. This paradigm is so fundamentally accepted, it’s no wonder that many miss that the trade to the full bridge presupposes the use of Si parts and the constraints these parts bring to the topology selection discussion. Most often, this topology is required to achieve conversion ratio, isolation, and/or reduce power semiconductor device stress [16-17]. Further, the topology operating point (i.e. selected switching frequency, duty ratio, conduction mode) and design values (inductance/capacitance values, device selections, etc.) are also selected as a part of this trade space. Influencing the
outcome of the study we have things like the need to stack secondaries (high voltage applications), easing primary switch stress, greater power handling capability, hard requirements for galvanic isolation, the thermal characteristics of commercial device packaging, and sometimes the prioritization of performance parameters. In most cases, the trade results in the full bridge or some isolated variant [18-19].

However, conventional wisdom on topology and operating point doesn’t capitalize fully on the availability of new devices nor does it fully consider the differences in the space application or its environment. With SiC MOSFETs in production and more feasible, we have devices with higher junction temperature tolerance, higher breakdown voltage, and lower switching loss. Further, over time, could prove to be more tolerant of the radiation environment in deep space as well. What does this mean to the power conversion stage? First, the lowered switching loss means we can operate with a higher switching frequency resulting in drastically reduced magnetic mass which, with thermal mass, makes up the largest portion of the converter mass fraction. Second, the higher junction temperature tolerance means we can operate with less heat rejection mass both in the converter as well as throughout the system. In addition, the SiC switch has a higher breakdown voltage than a Si part with comparable on state resistance meaning stacked secondaries may not be necessary in the high voltage supply. Finally, the new materials may offer higher tolerance to the extreme environment as outlined in section 4.

In total, the team considered seven combinations of topology, design operating point, and module size. These included (1) 10kW Hard-switched Boost, (2) 5kW Hard-switched Boost (Aggressive), (1) 10 KW Soft-switched Boost, (2) 5kW Soft-switched Boost, (1) 10kW Full Bridge and (2) 5kW Full Bridge. In general, preliminary calculations showed that the boost had the potential to have the least mass. Since the team was pursuing nonisolated options for the converter, described in the previous sub-section, the only other reasons to go with full bridge (conversion ratio and lowered device stress) were somewhat less compelling for our target application with a 1:4 conversion ratio and SiC devices. Given these considerations along with the part count comparisons and preliminary loss and mass predictions, the full bridge was ruled out.

The trade study included loss predictions and showed the soft switching boost doubler as the lowest loss and highest power density [20]. However, this topology was not selected due to its added complexity. In the end, the simplicity of the hard-switched boost coupled with its good performance when compared to a soft-switched variety was selected as the target topology. The choice of (2) parallel 5kW modules to yield the 10kW capacity were based on the desire to distribute heat across the device case to sink area. Our first order analysis shows that in combining improvements in device materials/physics (increase junction temperature tolerance, lower switching losses) with improvements in junction to case thermal resistance we can work all sides of the equation and achieve the gain predictions.

4. SYSTEM AND PACKAGING

The system architecture is designed for modularity, scalability, flexible integration, flexible test scenarios, and reworkability to reduce spacecraft volume and mass.

Modularity

Shown in Figure 2, the configuration implements a packaging baseline architecture consisting of five horizontally mounted Al slices, each measuring 208.7mm (8.2in) x 110.0mm (4.3in). The five slices corresponds to the five modules described in the previous Section. Slice-to-slice and slice-to-radiator retention are achieved through bolted interfaces.

Scalability

The architecture is easily scaled to the required power levels by adding the appropriate number of slices. Since all modules are bolted mechanically, and can be separated as five individual modules. The four modules, i.e. Magnetic Supply, Cathode Supply, Control/Valve Drive/House Keeping Supply, and Input/output Filter, are designed to support up to eight of the 10kW Anode Discharge Power Supply, which provides an 80kW PPU, shown in the right lower corner in Figure 2.

Slice/Module Definition

With the slices mounted in a horizontal configuration each slice provides its own dynamic and thermal paths. The machined web and mounting feet provide the unidirectional conduction path for each slice. Heat from the Printed Wire Board Assembly (PWBA) or individual web mounted components can maintain desired or allowable components junction temperatures with the base plate at 100°C.

Thermal analyses were performed using the different device packaging technologies, and the COB technology was chosen because of its superb thermal conductance. The expected maximum operating junction temperature was then decided as 160°C, shown in Table 1, along with the maximum current, maximum voltage and complexity, such as the number of components and layers of circuitry. A summary of device packaging technologies that will be considered for the high power and low power modules is provided in Table 2.
Figure 2. Modular and Scalable HTB PPU System.

Table 1. Slice/Module Summary

<table>
<thead>
<tr>
<th>Slice/Board</th>
<th>Temp (°C)</th>
<th>Current (A)</th>
<th>Voltage (V)</th>
<th>Complexity (Parts/Layers)</th>
<th>Size (cm x cm)</th>
<th>Cycles (°C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>I/O Filter</td>
<td>160</td>
<td>50</td>
<td>800</td>
<td>10µF Capacitors</td>
<td>Cap size</td>
<td>160 to -15</td>
</tr>
<tr>
<td>10kW Anode Power Supply</td>
<td>160</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Power</td>
<td>160</td>
<td>50</td>
<td>800</td>
<td>1-2 layer</td>
<td>2.54 x 2.54</td>
<td>160 to -15</td>
</tr>
<tr>
<td>PWM Control Board</td>
<td>160</td>
<td>0.18</td>
<td>28</td>
<td>8 layer</td>
<td>17.78 x 10.16</td>
<td>161 to -15</td>
</tr>
<tr>
<td>Magnetic Supply</td>
<td>160</td>
<td>20</td>
<td>200 (in)</td>
<td>8 layer</td>
<td>17.78 x 10.17</td>
<td>162 to -15</td>
</tr>
<tr>
<td>Cathode/Heater</td>
<td>160</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Cathode Keeper</td>
<td>160</td>
<td>0.125</td>
<td>800</td>
<td>8 layer (30 components)</td>
<td>17.78 x 10.17</td>
<td>162 to -15</td>
</tr>
<tr>
<td>Cathode Heater</td>
<td>160</td>
<td>5</td>
<td>100</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Ctrl/Buck Power/Valve Drive</td>
<td>160</td>
<td>2</td>
<td>28</td>
<td>12 layer (200 components)</td>
<td>17.78 x 10.17</td>
<td>162 to -15</td>
</tr>
</tbody>
</table>

Table 2. Device Packaging Summary

<table>
<thead>
<tr>
<th></th>
<th>High Power Board</th>
<th>Low Power Board</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Substrate</strong></td>
<td>Direct Bond Cu (DBC) AlN, DBC Al₂O₃, Si₃N₄ Active Metal Bonding (AMB) Cu</td>
<td>HTCC, LTCC, High Temp Polyimide</td>
</tr>
<tr>
<td><strong>Component Attachment</strong></td>
<td>Direct Chip Atatch: Au80Sn20</td>
<td>Mixed Tehcnology: Au80Sn20, Sn5Pb95, ME8863</td>
</tr>
<tr>
<td><strong>Conductor</strong></td>
<td>Ni/Au plated Cu, Au wire, Au pad</td>
<td>Substrate Dependent, Au top metal</td>
</tr>
</tbody>
</table>
5. Other Applications

Power electronic components and packaging technology used for the HTB are also finding their way into many other applications. These applications include power management and actuation for electric vehicles, drive and control of high power industrial electric motors, automotive and avionic engine control and real time down-hole monitoring of the geothermal and oil wells. In all these applications, the desire for reduction of volume and mass of the controllers is forcing the deployment of highly efficient high voltage/high temperature switching semiconductor devices instead of Si based equivalent. Similar to the HTB properly designed high temperature capable power electronics for these applications takes advantage of emerging high temperature packaging technologies and passive components. Without exception these high temperature systems once optimally designed, are demonstrating longer life and higher reliability.

6. Summary

The paper describes a proposed concept of the modular and scalable High Temperature Boost Power Processing Unit. It features a new system-level implementation and a non-isolated converter topology that is unconventional in current state-of-the-art PPU designs. The novel design can also address two critical issues: cathode current sharing across multiple thrusters, and leakage current from the spacecraft plasma through micrometeoroid holes in the cover of the solar array.

Efficiency and power density are generally considered to be the most important performance parameters. By using emerging technologies, including SiC and advanced Chip-on-Board and Multi-Chip Module high temperature packaging, the topology is designed to significantly improve over the conventional state of the art. This is especially true when the design is operated at high-temperature conditions that take full advantage of the high temperature SiC devices.

The use of high-temperature technologies enables the operation at a higher operating temperature, and, therefore, dramatically reduces the mass and volume of the thermal management required by a conventional power conversion and processing system. The high-temperature operation also yields a factor of five improvement in PPU specific power or specific mass, which can be translated to be equivalent to over 88% mass saving at the PPU level and over 30% mass saving at the power system level for a 320kW thruster-powered Human Exploration mission.

The system packaging architecture, along with the device level packaging configuration, is designed for modularity, scale-ability, flexible integration, flexible test scenarios, and re-workability to reduce spacecraft volume and mass. The configuration implements a packaging baseline architecture consisting of five horizontally mounted Al slices, each measuring 208.7mm (8.2in) x 110.0mm (4.3in). Slice-to-slice and slice-to-radiator retention are achieved through bolted interfaces. The design is easily scaled to the required power levels by adding the appropriate number of slices.

Compared to the current state-of-the-art technology, the HTB PPU provides both high power and high specific impulse, with low mass and high efficiency. This capability enables spacecraft missions that require high power, such as cargo transport, as well as deep space missions that require high specific impulse.

The effort is currently on-going. The technology challenges, including active and passive device reliability at high temperatures, high-temperature device and system level packaging, and guidelines for space qualification and applications, are being investigated and addressed.

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References:


Biographies

**Greg Carr** is a Power System Engineer for Power and Sensor Systems Section 346 at JPL. His primary responsibility is the development of new power system architectures. He recently served as the Avionics Power Chief Engineer on the Mars Science Laboratory (MSL), which is a radioisotope powered rover designed for the surface of Mars. Prior to that Greg served as the Power Electronics Design Group Supervisor. Greg is currently a member of the NASA Engineering and Safety Center (NESC) Electrical Power Technical Discipline Team (TDT). Greg has over 20 years of experience in power electronics design and power system engineering. He started his career designing the power control and power distribution interface for Cassini, which is a Radioisotope Thermoelectric Generator (RTG) powered spacecraft exploring the Saturn system. Greg has a BSEE degree from UCLA.

**Chris Iannello** received his BSEE, MSEEE, and PhD EE at the University of Central Florida in ’94, ’99, and ’01 respectively all in Power Electronics. He serves as the Deputy Technical Fellow for Power as well as a Deputy Chief Engineer at NASA’s Kennedy Space Center where he has worked since 1989. In addition to his NASA career, Dr. Iannello has worked as a senior designer for an advanced power electronics design firm focusing on power electronics R&D with clients including John Deere, Emerson Electronics, Engineering Acoustics, NSF, and the Department of Defense. He has also served as senior researcher in UCF’s Florida Power Electronics Center, focusing on R&D activities to advance the state-of-the-art in Power Electronics with specific emphasis on power stage analysis / design as well as control loop design. As a Researcher, he has published over 20 papers in engineering journals, leading discipline conferences, and tutorial seminars.

**Yuan Chen** received her Ph.D. degree in reliability engineering from the University of Maryland at College Park, Maryland, in 1998, with a Graduate Fellowship from the National Institute of Standards and Technologies. Currently, she is a senior technical member with the Electronic Systems Branch, NASA Langley Research Center. She was with Jet Propulsion Laboratory during 2002-2009, and with Bell Labs, Lucent Technologies, during 1999-2002. Her research area is on the reliability and qualification methodologies on the electrical, electronic and electro-mechanical parts, and development of new technologies for space applications.
She is a senior member of IEEE and AIAA, and the editor of IEEE Transactions on Device and Materials Reliability.

Don J. Hunter has been with the Jet Propulsion Laboratory and a member of the Advanced Electronic Packaging Engineering section since 1993. Major contributions included the development of a ruggedized 6U-VME flight system design for the Mars Pathfinder Mission, Cal Tech and US Patents for work in advanced packaging systems architectures: Integrated 3D Technology on a Spacecraft Panel, development of technology pertaining to miniaturization of science instruments and flight design of a multifunctional antenna design for the Deep Impact Mission. He holds a B.S. in mechanical engineering from California State University Los Angeles and has been involved in electro-mechanical packaging environment for over 25 years. He possesses experience ranging from commercial applications to military (DOD) cold temperature and high-G integrated packaging applications.

Linda Del Castillo is a Senior Materials Scientist/ Microdevices Engineer in the Nano and Microsystems Group at JPL. She received her B.S. in Mechanical Engineering from California State Polytechnic University, Pomona, followed by M.S. and Ph.D. degrees in Materials Science and Engineering from the University of California, Irvine. Since beginning her work at JPL in 2000, she has performed research on extreme environment survivable electronic sensors and systems for Venus and highly corrosive, high temperature terrestrial environments, electronic packaging for active membrane radar applications, flexible embedded active devices, as well as advanced materials evaluation for high voltage, high heat flux and high frequency hybrid electronics.

Mohammad Mojarradi is the group supervisor for advanced instruments electronics group at the Jet Propulsion Laboratory. He received the Ph.D. degree in electrical engineering from the University of California, Los Angeles (UCLA) in 1986. Prior to joining Jet Propulsion Laboratory, Pasadena, CA, he was an Associate Professor at Washington State University and the Manager of the mixed-voltage/specialty integrated circuit group at the Xerox Microelectronics Center, El Segundo, CA. He is a Specialist in integrated mixed-signal/mixed-voltage electronic sensors, micromachined interface circuits, and mixed-mode integrated circuit design. He has more than 30 years of combined industrial and academic experience in his field. His current work focuses on developing highly efficient, extreme environment capable, integrated mixed-signal electronics for sensors, actuators, and power management and distribution systems (PMAD) for space borne instruments.

Arthur Bradley received his B.S., M.S., and Ph.D. degrees in Electrical Engineering from Auburn University in 1990, 1992, and 1999 respectively. In August of 2003, he joined NASA as a senior analog engineer for Langley Research Center’s Electronics Systems Branch. Significant work to date has included establishing LaRC’s Robotics and Intelligent Machines Laboratory, serving as the principal investigator for NASA’s Joint Technical Architecture for Robotic Systems (JTARS) project, and leading the development of a handbook for low-noise system design. He currently serves as the Assistant Branch Head of Electronic Systems and assists on a variety of spaceflight projects.