

# DESDynI Quad First Stage Processor – A Four Channel Digitizer and Digital Beam Forming Processor

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**Abstract**—The proposed Deformation, Eco-Systems, and Dynamics of Ice Radar (DESDynI-R) L-band SAR instrument employs multiple digital channels to optimize resolution while keeping a large swath on a single pass. High-speed digitization with very fine synchronization and digital beam forming are necessary in order to facilitate this new technique. The Quad First Stage Processor (qFSP) was developed to achieve both the processing performance as well as the digitizing fidelity in order to accomplish this sweeping SAR technique. The qFSP utilizes high precision and high-speed analog to digital converters (ADCs), each with a finely adjustable clock distribution network to digitize the channels at the fidelity necessary to allow for digital beam forming. The Xilinx produced FX130T Virtex 5 part handles the processing to digitally calibrate each channel as well as filter and beam form the receive signals.

Demonstrating the digital processing required for digital beam forming and digital calibration is instrumental to the viability of the proposed DESDynI instrument. The qFSP development brings this implementation to Technology Readiness Level (TRL) 6. This paper will detail the design and development of the prototype qFSP as well as the preliminary results from hardware tests.

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## 1. INTRODUCTION

Software Defined Radios (SDRs) remains an attractive theoretical model to radar design. With advancements in ADC and digital signal processing technology, even the most advanced Synthetic Aperture Radars (SARs) are approaching the ideal receiver architecture. One key aspect

of SDRs is direct sampling of the signal from the antenna without down-conversion to baseband. For an L-band SAR, careful bandwidth frequency selection and filtering can be used to allow direct digital down-conversion during the ADC sampling process. Additional digital filtering is then employed to achieve required out-of-band rejection and suppression of aliased images. These techniques have been implemented in the design of the DESDynI Quad First Stage Processor (qFSP) and their validation is a key element of the subsequent testing.

Another benefit of shifting much of the signal processing to the digital domain is the ability to digitize individual receive channels independently. Combined with a reflector antenna this would enable receiving of multiple radar returns on different antenna patches simultaneously. We could also digitally beam form the data to optimize the antenna and receiver response throughout the swath. The qFSP implements four independent receive channels on a single board in order to optimize the use of resources available in a single Xilinx Virtex 5 FPGA.

The Virtex 5 FPGA offers dramatic increases in available resources to implement digital signal processing algorithms. We are able to utilize the full capacity of the FPGA resources because the rad-hard by design approach of this chip eliminates the need for triple modular redundancy at the logic level for space applications. Since this chip can simplify the system architecture significantly one of the main goals of the development of this board is to demonstrate the performance and implementation of the Virtex 5 FPGA.

The qFSP was designed specifically with the proposed DESDynI SAR instrument in mind. Although there are many system specific features in this design, the core of the architecture is applicable over a wide range of instruments that need multi-channel digitizers.

## 2. DESDYN I INSTRUMENT ARCHITECTURE

The proposed DESDynI SAR instrument is designed as a multi-channel digital beam forming radar employing the SweepSAR technique to maximize swath width while maintaining high resolution. This instrument is designed to meet science requirements to make measurements for solid earth, ecosystem structures, and cryosphere studies. In order to fulfill these requirements, this radar would be able

to support repeat-pass interferometric SAR operations as well as fully polarimetric SAR measurements.

The current instrument design would use identical H-pol and V-pol receive chains (shown in figure 1), each beginning with a set of L-band antenna patches. Each set of patches in the antenna array connects to a single Transmit and Receive Module (TRM). A set of four TRMs would interface with a single qFSP, which would convert the analog radar return signals from each channel to digital sample format. Multiple qFSPs would digitize the return signal from the full array of RF channels and send the digitized and processed samples to the digital back-end electronics for further processing and storage on the recorder.

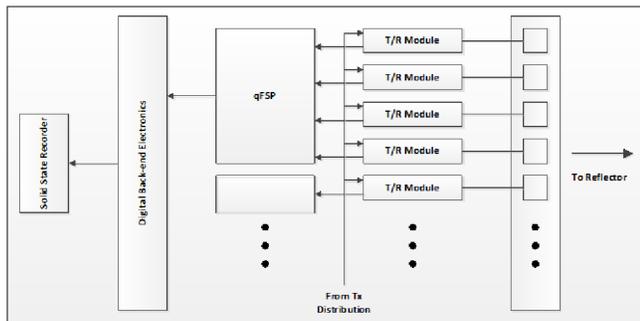


Figure 1 : DESDynI Receive Chain (Single Pol)

### 3. SWEEPSAR TECHNIQUE

Traditional spaceborne SAR instruments have had to limit their swath width to a size that could be collected between the times of two consecutive transmit events. Since orbital velocities are high and long antennas are expensive, this limit has been around 30 to 100 km for full resolution systems. ScanSAR is a technique that can increase this range, but it requires burst mode operation, which reduces azimuth resolution and can cause along track variations in the imaging performance.

SweepSAR ([1]) is a new technique that would expand the swath to enable full Earth access in a 12-day cycle. It would take advantage of the fact that an echo returning from a pulse transmitted from a side looking geometry “sweeps” across the range of look angles as a function of time. At any instant in the receive window, only a portion of the look angle range would contain energy from a given pulse. As a result, it would not be necessary for the receive antenna pattern to cover the full swath at once. Instead, it could be focused into a narrower beam and digitally steered through dynamic beam formation to follow the return of the echo as it moves across the angle space. In the case of the proposed DESDynI instrument, this technique would allow the instrument to take full advantage of the antenna’s extent in the range direction and form a narrower receive pattern with improved antenna gain and a faster roll off to reject radar range ambiguities. Figure 2 shows the transmit and receive geometries proposed for SweepSAR.

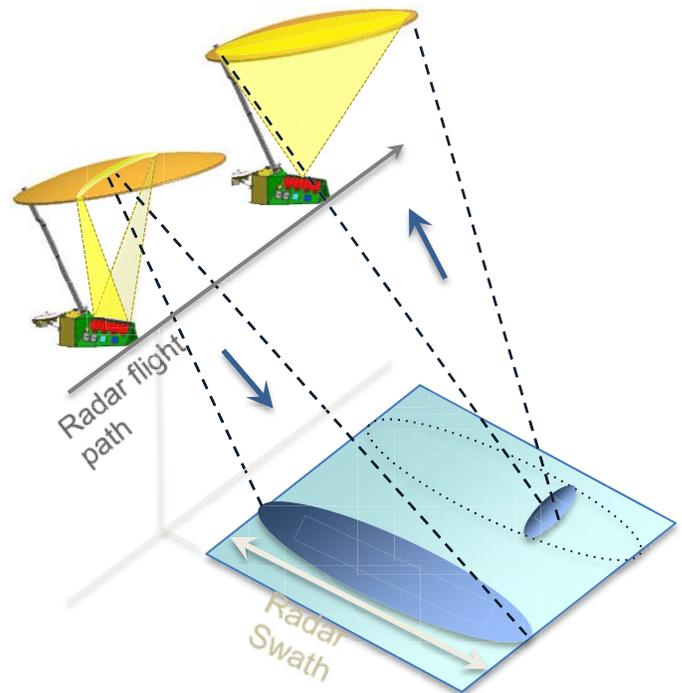


Figure 2 : Proposed SweepSAR Transmit/Receive Configuration

### 4. DIGITAL SIGNAL PROCESSING ALGORITHMS

A significant constraint on DESDynI’s overall projected performance is the ability to downlink radar data to the ground. As a result, several on-board processing steps have been implemented to reduce data volume and improve performance. The processing algorithms implemented in the qFSP include: digital calibration, first stage filtering, and digital beam forming.

With access to the raw ADC data prior to beam forming, the qFSP has a unique ability to measure performance of individual radar channels. During transmit events, the qFSP would capture a coupled and attenuated version of the transmit waveform from each of the four channels that it monitors. These waveforms would then be time domain correlated with a reference waveform using three separate time lags. The three resulting complex correlation values would be used to detect and compensate for time and phase shifts in the transmit chain. Being able to sample and process this signal on-board would avoid the need for routinely sending the raw transmit waveforms to the ground, making corrections much more timely and allowing more communication bandwidth for science data. During the receive portion of the measurement cycle, a tone would be injected into the front end of the receiver. Like the transmit pulse, this tone would be correlated with an ideal sinusoid to monitor phase and amplitude drifts in the electronics. Any changes detected in the complex correlation by the FSP would be forwarded to the downstream processing for compensation prior to beam forming.

The L-band echo would be digitally down converted using an intermediate sampling rate that, depending on radar

mode, would still be significantly higher than the bandwidth of the science data. The qFSP is responsible for the first stage of digital filtering to reduce the data that needs to be downlinked. The Multi-rate Finite Impulse Response filter was implemented using the thread decomposition method as described in [2].

To reduce instrument cost while still preserving swath width, the antenna feed element spacing along the elevation direction would be increased such that individual receive beams overlap each other near the 3dB point on the patterns. Without beam forming, science data would have significant amplitude and phase ripple across the swath. Digital beam forming would be used to improve the performance between the beams ([3]). If applied on the ground, however, the data rate from the instrument would need to increase by at least a factor of 3. The solution was to apply beam forming on-board. The qFSP would use a three tap, table-based beam forming implementation to form the composite range lines for each echo.

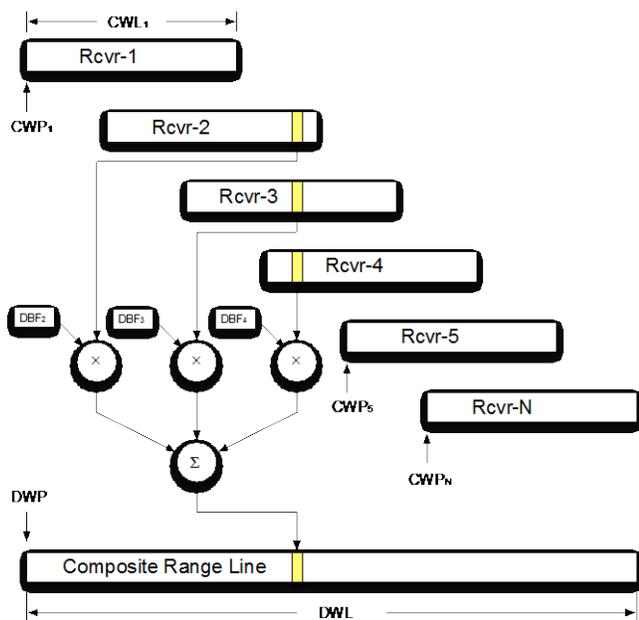


Figure 3 : qFSP DBF algorithm to form Composite Range Line

The baseline coefficient set used for beam forming is based on the Conjugate Field Matching technique to optimize Signal to Noise Ratio (SNR) across the swath, but the table storing these coefficients could be updated so adjustments could be made throughout the mission if antenna patterns change or other optimizations are found to give better science results. To achieve a smooth uniform gain across the swath, beam forming coefficients would be updated every 0.1 degrees in look angle.

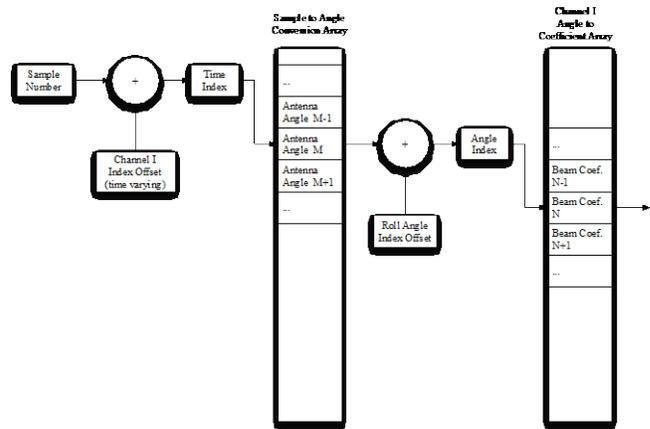


Figure 4 : Sample to DBF coefficient lookup

The angles are related to the sample time within the receive window based on information in the command word.

### 5. qFSP HARDWARE BLOCK DIAGRAM

The qFSP is designed around the Virtex 5 FPGA (XC5VFX130T). There are four ADCs, which digitize four independent receive channels. The surrounding supporting circuits enable high fidelity synchronous clock distribution as well as high-speed transmission of digital data. The qFSP also performs the additional function of providing a control interface to the TRMs as well as telemetry acquisition. Figure 5 shows the block diagram of the qFSP.

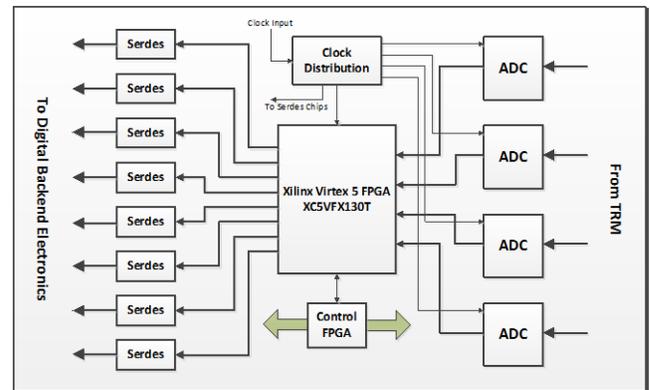


Figure 5 : qFSP Block Diagram

The clock distribution is highly critical in multi-channel digital beam forming applications. To achieve proper algorithm performance the channels need to be aligned on the scale of tens of picoseconds. We have implemented clock skew control capability at each ADC to accomplish this. The skew control is set with feedback from the calibration algorithm on the FPGA. A combination of fine skew control internal to the ADC and coarser skew control with a step size of 10ps external to the chip is used. The current clock design expects an input clock rate of 240MHz.

The qFSP uses an Actel FPGA to control the internal operations of the board. This FPGA also provides signals to control each of the four TRMs.

## 6. DATA HANDLING AND TRANSMISSION

Data handling and transmission is a challenge in digital beam forming systems because data rates increase linearly with the number of digital channels. The qFSP was designed to handle data rates of 16 Gbps of continuous throughput. Multi-gigabit transmission lines are used as the conduit for these high data rates. Currently, Texas Instruments produced chips are utilized as the transceivers due to their space heritage.

The SweepSAR technique would require high duty cycles for each receive channel, which would make buffered processing of real-time data unrealistic. The firmware design in the qFSP is able to keep pace with the sampling so that no extended buffering is needed on chip. The supported output data rate would also be greater than the rate of data acquisition in order to facilitate continuous operation.

## 7. ADC PERFORMANCE ANALYSIS

A series of tests have been performed to evaluate the performance of the ADCs on this board. Signal to Noise And Distortion ratio (SINAD), Spurious-Free Dynamic Range (SFDR), and SNR, are the primary performance metrics being investigated.

SINAD is estimated in the time domain by fitting a sinusoidal function of the form  $f(t) = A \cos(\omega t + B) + C$  to the sampled sine wave measured at various frequencies and input power levels. In the previous equation, A, B, and C are fitting parameters;  $\omega$  is angular frequency in rad/s; and t is time in seconds. The signal power is estimated based on an optimally fit sine wave while the residual are treated as noise/distortion. As a quality check, SINAD is also computed in parallel based on FFT analysis. Using 32k FFT (7.5kHz resolution) SFDR and SNR are also estimated.

A typical frequency spectrum shown in Figure 6 was sampled at 240 MSPS. The estimated performance metrics based on this measurement are also listed in Figure 6. Note that the ADC specifications state that 54.5 dBc SFDR is expected for this particular configuration. 51.6 dBc SFDR is measured. However, the measured SINAD and SNR are ~15 dB lower than expected. This suboptimal performance is partly contributed by excessive sampling jitter, which is a combination of clock jitter and ADC's aperture uncertainty. Figure 7 shows the SNR for 7 distinct input frequencies. The SNR performance decreases as the input power increases. The degradation is more prominent at high frequencies. This behavior is consistent with the effect of sampling jitter and can be translated into equivalent time jitter of 2.6 to 3 ps for all frequencies shown in Figure 7. Improvement is on-going to provide better quality clock input for the ADC.

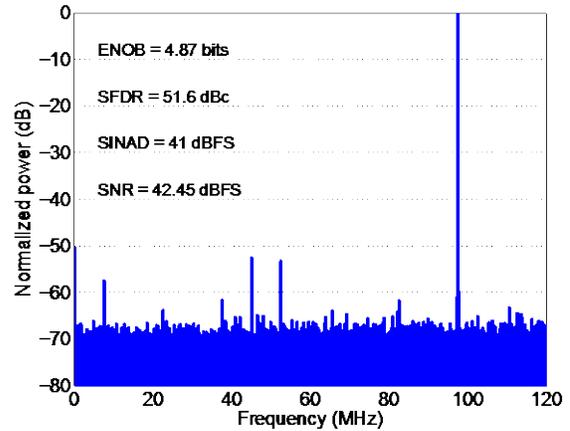


Figure 6: Frequency spectrum of 1297.5 MHz sinusoidal input at -10 dBFS power level

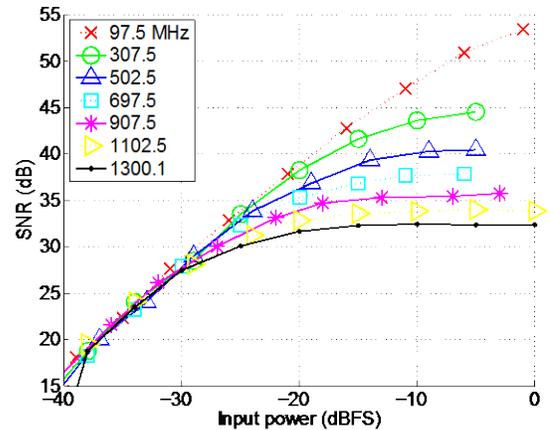


Figure 7 : SNR for multiple distinct input frequencies from 97.5 MHz(first Nyquist zone) to 1300.1 MHz (L-band)

## 8. ALGORITHM PERFORMANCE ANALYSIS

Algorithm performance evaluation is also on-going and a bit-true simulation test bed has been developed for this purpose. The algorithm is being tested in the sub-component level as well as the system level. Figure 8 shows the simulated filter response along with the actual filter response obtained by feeding the ADC with sine waves at different frequencies across the passband. The signal power was estimated at the output of the first stage filter (80 MHz bandwidth) on the Virtex 5 FPGA. Note that the simulation result is also verified with the FPGA functional simulator and bit-by-bit equivalence has been achieved. The measurement result shown in Figure 8 generally agrees with the simulation although the passband performance clearly needs improvement (0.1 dB passband ripple is desired).

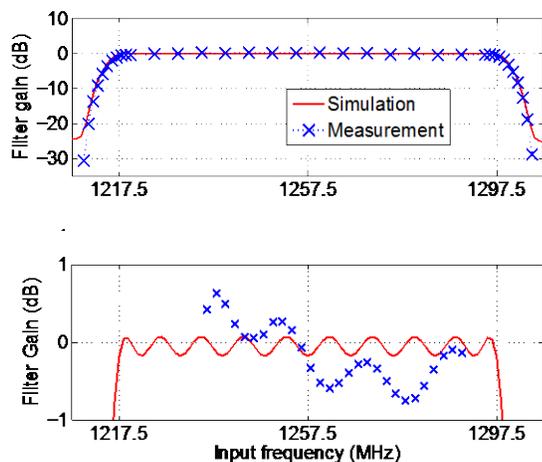


Figure 8 : Gain of the 80 MHz digital filter on Virtex 5 FPGA

Amplitude calibration capability of qFSP is also tested. In this setup, a 40 MHz chirp (1217.5—1257.5 MHz) pulse is input to the board along with a calibration tone signal (caltone) centered at 10 MHz below the passband of 80 MHz digital filter. The pulse-to-pulse amplitude variation of signal power on the receive chain is captured and compensated based on the power level of the caltone evaluated internally on the FPGA.

To emulate varying power loss on the receive chain of the system, the coupled chirp/caltone signal is attenuated at ADC's input. The attenuation level is varied from -1 to -20 dB. Figure 9 shows the total power of each pulse before and after amplitude correction. Like other tests, it is expected that improving quality of the input signal would also improve the performance of the amplitude calibration process.

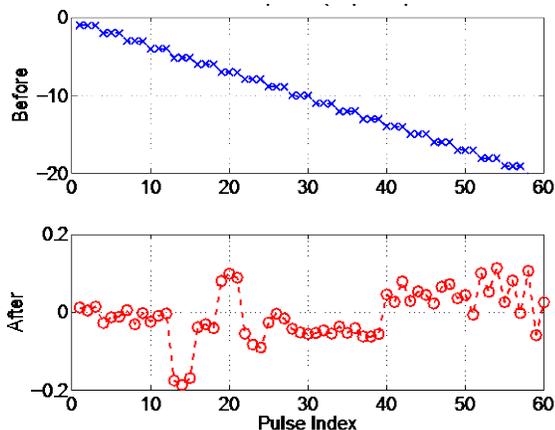


Figure 9 : (normalized) total power of the chirp waveform before and after amplitude calibration

## 9. CONCLUSIONS

We have implemented a key block in the proposed DESDynI instrument that would enable the ability to perform SweepSAR. We have described the motivation for the architecture and design of this board and detailed the

technology implementation used to achieve this capability. Although improvements still need to be made to achieve the required performance, the basic infrastructure and functionality have been demonstrated.

## 10. FUTURE WORK

The ADC performance on this board will need to be improved to meet system requirements. As we understand board level interactions of the circuits and signals we can implement the optimizations needed to achieve required performance.

In order to advance the TRL level even further this unit could be integrated in an airborne or spaceborne system for validation in relevant environmental conditions.

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We would like to thank Don Hunter and Mau-Huu Tran for providing the mechanical fixture and design to enable testing of this board. This is not a trivial matter for a board that is 13" x 20".

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## BIOGRAPHIES

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