National Aeronautics and Space Administration

Aeroflex Technology as Class-Y Demonstrator

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1.0 INTRODUCTION

Modern space field programmable gate array (FPGA) devices with increased functional density and operational frequency, such as Xilinx Virtex 4 (V4) and 5 (V5), are packaged in non-hermetic ceramic flip chip forms. These next generation space parts were not qualified to the MIL-PRF-38535 Qualified Manufacturer Listing (QML) class-V when they were released because class-V was only intended for hermetic parts. In order to bring Xilinx V5 type packages into the QML system, it was suggested that class-Y be set up as a new category. From 2010 through 2014, a JEDEC G12 task group developed screening and qualification requirements for Class-Y products. The Document Standardization Division of the Defense Logistics Agency (DLA) has completed an engineering practice study. In parallel with the class-Y efforts, the NASA Electronic Parts and Packaging (NEPP) program has funded JPL to study potential reliability issues of the class-Y products. The major hurdle of this task was the absence of adequate research samples. **Figure 1-1** shows schematic diagrams of typical structures of class-Y type products. Typically, class-Y products are either in ceramic flip chip column grid array (CGA) or land grid array (LGA) form. In class-Y packages, underfill and heat spread adhesive materials are directly exposed to the spacecraft environment due to their non-hermeticity. One of the concerns originally raised was that the underfill material could degrade due to the spacecraft environment and negatively impact the reliability of the package. In order to study such issues, it was necessary to use ceramic daisy chain flip chip package samples so that continuity of flip chip solder bumps could be monitored during the reliability tests. However, none of the commercially available class-Y daisy chain parts had electrical connections through flip chip solder bumps; only solder columns were daisy chained, which made it impossible to test continuity of flip chip solder bumps without using extremely costly functional parts. Among space parts manufacturers who were interested in producing class-Y products, Aeroflex Microelectronic Solutions-HiRel had been developing assembly processes using their internal R&D class-Y type samples. In early 2012, JPL and Aeroflex initiated a collaboration to study reliability of the Aeroflex technology as a class-Y demonstrator.

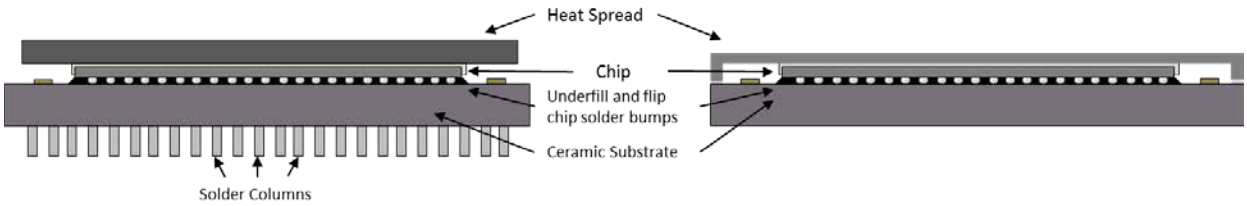

Figure 1-1. Schematic diagrams of class-Y type packages, column grid array (left) and land grid array (right).

1.1 Relevance of the Aeroflex Test Sample Configuration to General Class-Y Products

In order for the current study to serve as a demonstrator for class-Y, the Aeroflex samples would need to have packaging configuration somewhat representative of most class-Y products. The currently commercially available class-Y type products, Xilinx V4 and V5, have configurations shown in **Figure 1-1**. The CGA package has solder columns attached, while the LGA has pads finished with Ni/Au plating. Since reliability of solder columns is extensively studied through other NEPP tasks [1] and does not depend on the hermeticity, the reliability of solder columns is not within the scope of the current study. The current study focused on the reliability of the flip chip solder bumps and underfill. **Table 1-1** compares packaging constructions of the Aeroflex sample, Xilinx CN, and Xilinx CF packages. The table was constructed under the assumption that the new CN package has the same flip chip solder bump geometry and the under bump metallurgy (UBM) as the old CF package, since the flip chip die will be identical for both CF and CN packages.

Table 1-1. Comparison of Aeroflex, Xilinx CF, and Xilinx CN packages.

Component	Aeroflex Sample	Xilinx CN Package	Xilinx CF Package
Heat Spread	None	Al-SiC	SiC (38.5x38.5x2mm)
Heat Spread Adhesive	None	Kyocera proprietary	ATI material; IBM proprietary
Die	Si(15.24 x 15.24 x 0.7mm)	Si (2 5x 25x 1 mm)	Si (25x25x1mm)
Under Bump Metallurgy (UBM)	Al/NiV/Cu	Ti/Cu/Ni	Ti/Cu/Ni
Flip chip Solder Bump Material	Sn63Pb37 (T_m=183˚C)	Sn63Pb37 (T_m=183˚C)	95Pb 5Sn (T_m= 308~312 ˚ C)
Flip chip passivation opening size	80 µm	~80 µm	~80 µm
UBM Diameter	102 µm	~105 µm	~105 µm
Flip chip Solder Bump height (assembled)	~80 µm	~90 µm	~90 µm
Flip chip Solder Bump width	~150 µm	~150 µm	~150 µm
Flip chip Solder Bump pitch size	254 µm	~250 µm	~250 µm
Underfill Material	Aeroflex proprietary	Kyocera proprietary	LP2 material; IBM proprietary.
Substrate/Carrier	Multilayer ceramic	Multilayer ceramic	Multilayer ceramic
Solder Column	None	Pb80Sn20 with copper helix	Pb90Sn10

The major factors that are known to affect reliabilities of flip chip solder joints are die size, underfill material, substrate material, UBM configuration, flip chip solder bump material, and flip chip solder geometry.

Figure 1-2 is a picture of the Aeroflex sample. The Aeroflex sample consists of daisy chain flip chip dies with two different sizes: 15 × 15 mm die with 2853 bumps and 5 × 5 mm die with 317 bumps. Die size of the Aeroflex sample is smaller than that of Xilinx packages. Flip chip packages with larger dies tend to exhibit shorter thermal cycling life, since the stress induced by the coefficient of thermal expansion (CTE) mismatch between the die and the substrate is proportional to the distance from the center of the die. Therefore, one should take the difference of the die sizes into account when translating thermal cycling results shown in the current study into other packages.

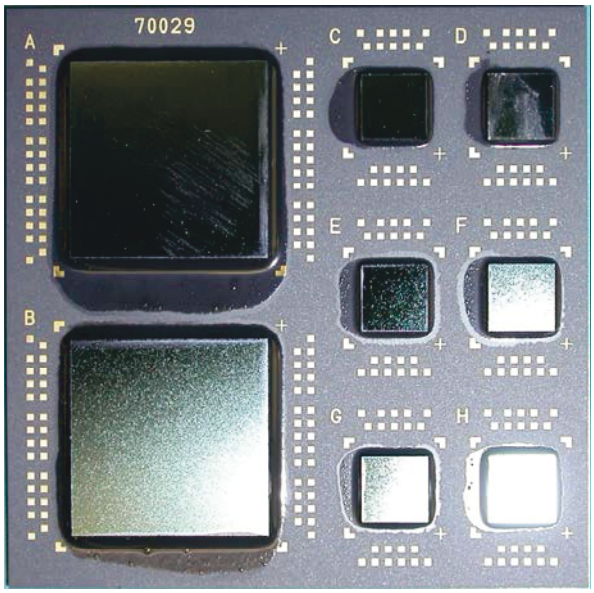

Figure 1-2. An Aeroflex sample, with two 15 x 15 mm size dies and six 5 x 5 mm size dies.

Underfill material plays a critical role in thermal cycling reliability of flip chip solder joints [2]. A properly formulated and applied underfill will carry most of the thermal cycling stress instead of the flip

chip solder joints, reducing stress on flip chip solder bumps by more than an order of magnitude. As a result, flip chip solder bumps will show greatly increased thermal cycling fatigue life when underfill is used. For example, flip chips that would exhibit 50% interconnection failure (N_{50}) after about 1300 cycles of thermal cycling in the absence of underfill will not show enough failures to calculate N_{50} after 10,000 cycles in the presence of underfill [3]. The general wisdom among flip chip engineers is that failure of flip chip solder joints generally does not occur until the underfill starts to break down. All three packages in **Table 1-1** use different underfill materials.

The UBM structure of the Aeroflex sample is Al/Ni(V)/Cu, while that of the Xilinx package is Ti/Cu/Ni. The Al/Ni(V)/Cu UBM structure, developed by Flip Chip International, Inc., has been widely used with eutectic SnPb solder for commercial applications since the 1990s. Xilinx's Ti/Cu/Ni UBM somewhat resembles typical UBM for Pb-free solder bumps. It is not clear why the UBM is used for Pb-free solders with Pb95Sn5 or Sn63Pb37 solder. Since there are commercial Pb-free versions of the V4 and the V5, it might be because of the decreased wafer manufacturing cost achieved by using the same UBM structure for both the commercial and the space versions.

It should also be noted that both Aeroflex sample and Xilinx CN package use Sn63Pb37 solder as flip chip solder bump material, while the currently discontinued Xilinx CF package used high-Pb (95Pb5Sn) solder. 95Pb high-Pb solder has a higher melting temperature (308 to 312˚C) than the eutectic SnPb solder (183˚C); therefore, it will not reflow during the subsequent column attach and board mounting process, which makes it preferred solder material when used in ceramic packages. However, high-Pb solders cannot be used in plastic packages because plastic chip carriers cannot withstand their high reflow temperatures. Due to the decreasing demand for ceramic packages in commercial applications and the impact of the European Union's Restriction of Hazardous Substances (RoHS) directive, experienced high-Pb solder bumping facilities are becoming less available. Consequently, many military parts manufacturers, including Aeroflex and Xilinx, are beginning to use eutectic SnPb solder as flip chip solder bumps. The implications of using Sn63Pb37 solder alloy as flip chip solder material require further discussion in-depth and will be discussed in the section 2.1.3.

As shown in **Table 1-1**, flip chip solder bump configurations (such as bump opening size, pad size, bump height, bump width, and bump pitch size) are almost identical for all three packages. This is because all these packages are following classic design rules from the IBM C4 wafer bumping.

2.0 THE SOURCES OF POTENTIAL RELIABILITY ISSUES OF THE CLASS-Y PRODUCTS

2.1.1 Non-Hermeticity Issues

Since the class-Y type products are ceramic-based non-hermetic microcircuits by definition, the primary reliability concern raised from the aerospace community was whether the non-hermeticity would compromise the reliability of the package. The purpose of the hermetic packaging is to protect interconnects from the outside environment, such as moisture, carbon dioxide, or oxygen. Before underfill was invented, flip chip packages had often been hermetically sealed. For commercial purposes, the underfilled flip chip package does not need hermetic packaging [4]; the underfill protects the flip chip solder joints from the environment, though its primary advantage is to reduce the stress on the flip chip solder bumps. The common wisdom among packaging engineers is that there are two predominant flip chip failure modes to consider—solder fatigue and underfill breakdown. In general, solder fatigue is the preferred failure mode, as it can be readily de-rated as a wear-out failure mechanism. Further, if underfill breakdown is to occur, it typically does so prior to solder fatigue. Hence, if the flip chip assembly can be optimized to drive the limiting failure mechanism to solder fatigue, reliability can in turn be optimized. Therefore, a relevant concern for the space and military applications would be whether the underfill would prematurely break down when exposed to harsh environments, especially since the underfill is directly exposed to the environment. As a part of the efforts to answer this question, the NEPP program tasked JPL during FY11 and FY12 to investigate the effect of environmental exposure on the reliability of the Xilinx V4/V5 packages. Because there were no available class-Y type samples with daisy chained flip chip bumps, the FY11/FY12 tasks mainly focused on the behavior of the underfill (LP2 material) and the lid adhesive materials (ATI materials) and studied how the mission environments would affect their properties relevant to the reliability of the package. Among many constituents of the low-Earth orbit (LEO) environment, long-term vacuum exposure was concluded to be the most realistic risk factor; other risk factors, such as ionizing radiation and atomic oxygen, have been mitigated by shielding practices since the electronics are located inside the spacecraft. The concerns on the long-term vacuum exposure originated from the fact that the carbon-carbon molecular cleaving may be accelerated at elevated temperatures by the combined effect of the vacuum and the thermomechanical stress, resulting in degradation of the underfill. Another concern was potential exposure to humidity on Earth prior to the launch. Epoxy materials can absorb moisture and change properties. Underfill materials, which belong to the epoxy family, can absorb moisture under 85˚C/85% relative humidity (RH) environment past 700 hours, resulting in 50% reduction in interfacial fracture toughness [5]. Underfill swelling caused by moisture absorption can increase the stress level on flip chip solder joints. Moisture can also reduce elastic modulus, shear modulus, yield strength, and ultimate tensile strength of an epoxy through plasticizing, crazing, and chain scissioning. Even though baking can remove moisture from underfill, underfill properties can only be partially recovered through baking once an underfill material suffers degradation by moisture [6].

During the FY12 task, effects of exposure to humidity, vacuum thermal aging, and thermal aging on the properties of LP2 and ATI materials were investigated [7]. Lap shear strength of LP2 materials increased after both vacuum thermal aging and thermal aging, indicating that vacuum and heat will not degrade but improve the adhesion of LP2 material. However, the lap shear strength of LP2 material dropped approximately by 23% after 7 days of exposure to 85˚C/85% relative humidity (RH), and remained about the same after the 27 days of extended exposure. Adhesion of underfill material is known to critically affect thermal cycling reliability of flip chip packages, since underfill cannot effectively dissipate stress if it loses adhesion. Therefore, this result indicated that thermal cycling life of class-Y products might decrease when exposed to humidity. The humidity exposure also resulted in the reduction of glass transition temperatures (Tg) of both underfill and the lid adhesive materials. Glass transition temperatures of LP2 materials were reduced roughly by 30˚C after the humidity exposure. However, to what extent the reduction of lap shear strength and Tg would affect the thermal cycling life of the class-Y packages was not fully conclusive, because daisy chained flip chip bump samples were unavailable. In the current study,

Aeroflex's daisy chained flip chip bump samples were utilized to study the effect of the environmental exposure to thermal cycling life of the class-Y type packages.

2.1.2 Fine Feature Size and High Power Issues

In addition to the non-hermeticity, another potential cause for reliability issues in the class-Y packages are class-Y products' fine feature sizes and high power characteristics. The non-hermetic packaging configuration of the class-Y product is, in a way, a result of the device miniaturization. One of the reasons why the class-Y products are non-hermetic is that the modern fine featured, high-power devices were generating large amounts of heat, and a direct attachment of the heat spread on the die for better thermal management was required. The non-hermetic configuration allows this direct heat spread attachment. Since the future class-Y type packages will have even smaller feature sizes and higher power consumption, it was necessary to reflect the fine feature size and the high power characteristics to the current study on the reliability of class-Y packages.

2.1.2.1 Electromigration of Flip Chip Solder Joints

As the size of flip chip solder bumps decreases, the current density in the flip chip bumps will increase. The increased current density will increase the chance of electromigration failure of the flip chip solder joints. The risk of failure by electromigration in flip chip solder bumps is greater than or equal to the risk in Al and Cu interconnects because solders have low critical products of electromigration and can fail at a current density two orders of magnitude smaller than that needed for Al and Cu [8]. There have been extensive studies on flip chip solder bump electromigration over many years [9,10,11,12,13,14], and it has been found that the electromigration of the flip chip solder bumps has its own unique characteristics compared to the electromigration of the copper or the aluminum interconnects. Among the many characteristics, only what is relevant to the results shown in the current study will be briefly explained in this section.

In flip chip solder joints, the thickness of the die side interconnect is only 1/80 to 1/40 of the opening size of the flip chip solder bump, as shown in **Figure 2-1** (a). This dimensional difference creates a bottleneck of current flow at the corner of the solder bump, increasing the current density about an order of magnitude higher at the corner than the average current density of the entire solder bump [10]. This phenomenon is referred to as "current crowding". The current crowding induces a higher level of Joule heating at the corner [14]. Due to the high current density and the high Joule heating, electromigration is more predominant at the corner, causing the void to initiate always from the corner and to propagate along the upper contact interface of the solder bump as shown in **Figure 2-1** (b) [10]. As the void propagates, the current crowding point moves along with the tip of the void since the current cannot flow through the void [14]. As a result, a pancake-type void forms along the upper contact interface of the solder bump [15].

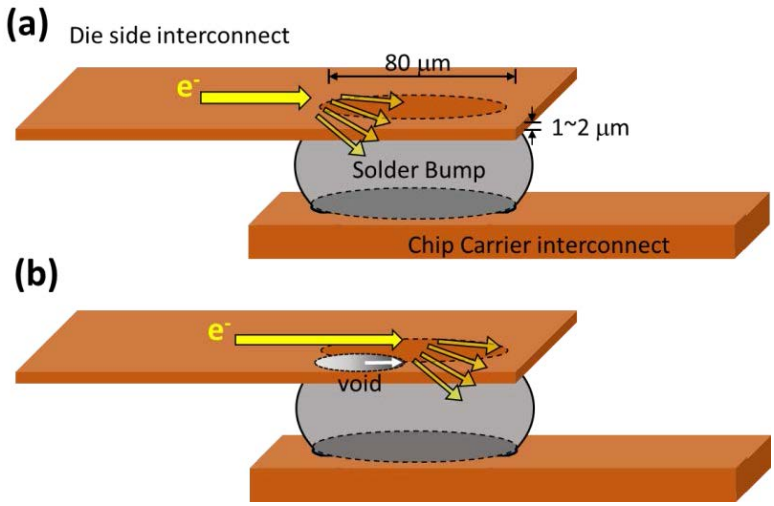

Figure 2-1. Schematic diagram depicting (a) current crowding and (b) void formation and propagation in a flip chip solder bump.

As shown in the **Table 1-1**, the UBM material and the solder bump alloys vary according to the part manufacturer. The UBM material and solder alloy composition significantly affects electromigration behavior of solder joints. When a flip- chip solder joint is subjected to a high current density, electromigration forces the UBM metal to dissolve, diffuse, and react with the solder. As a result, failure modes greatly vary according to the UBM material and solder alloy composition. Cu UBM tends to dissolve into solder and create Cu-Sn intermetallic compounds in the bulk of the solder; on the other hand, Ni UBM has less dissolution than the Cu UBM and does not form as much intermetallic. The UBM dissolution induced by electromigration also depends on the composition of the solder; Pb-free solders have higher solubility of UBM than SnPb solder. Thickness of the UBM also greatly affects electromigration failure mechanisms. **Figure 2-2** shows two-dimensional current density simulation results of flip chip solder joints with different UBM thicknesses. The dimension of the flip chip solder joint is 100 µm in diameter and 70 µm in height. If the UBM is thick (~10 µm), the current crowding is confined within the UBM (**Figure 2-2** (c)). In such a case, the high current density within the UBM drives the UBM metal into the solder, causing a massive UBM dissolution. Consequently, the dissolved UBM metal reacts with the Sn in the solder and causes a massive intermetallic compound formation [16]. Therefore, a massive intermetallic compound formation is generally observed before the void formation when the UBM is thick. If the UBM is thin (1 to 2 µm), the current crowding occurs both inside and outside of the UBM. In such case, the high current mainly drives the solder along the direction of electron flow, and void formation and propagation take place only with a small amount of UBM dissolution and intermetallic compound formation. Since the electromigration failure mechanism of flip chip solder bump is influenced by many factors, the electromigration reliability of flip chip solder joints needs to be approached case-by-case. Therefore, the electromigration life of the Aeroflex samples cannot be directly translated into electromigration life of other class-Y packages with different flip chip solder joint configurations.

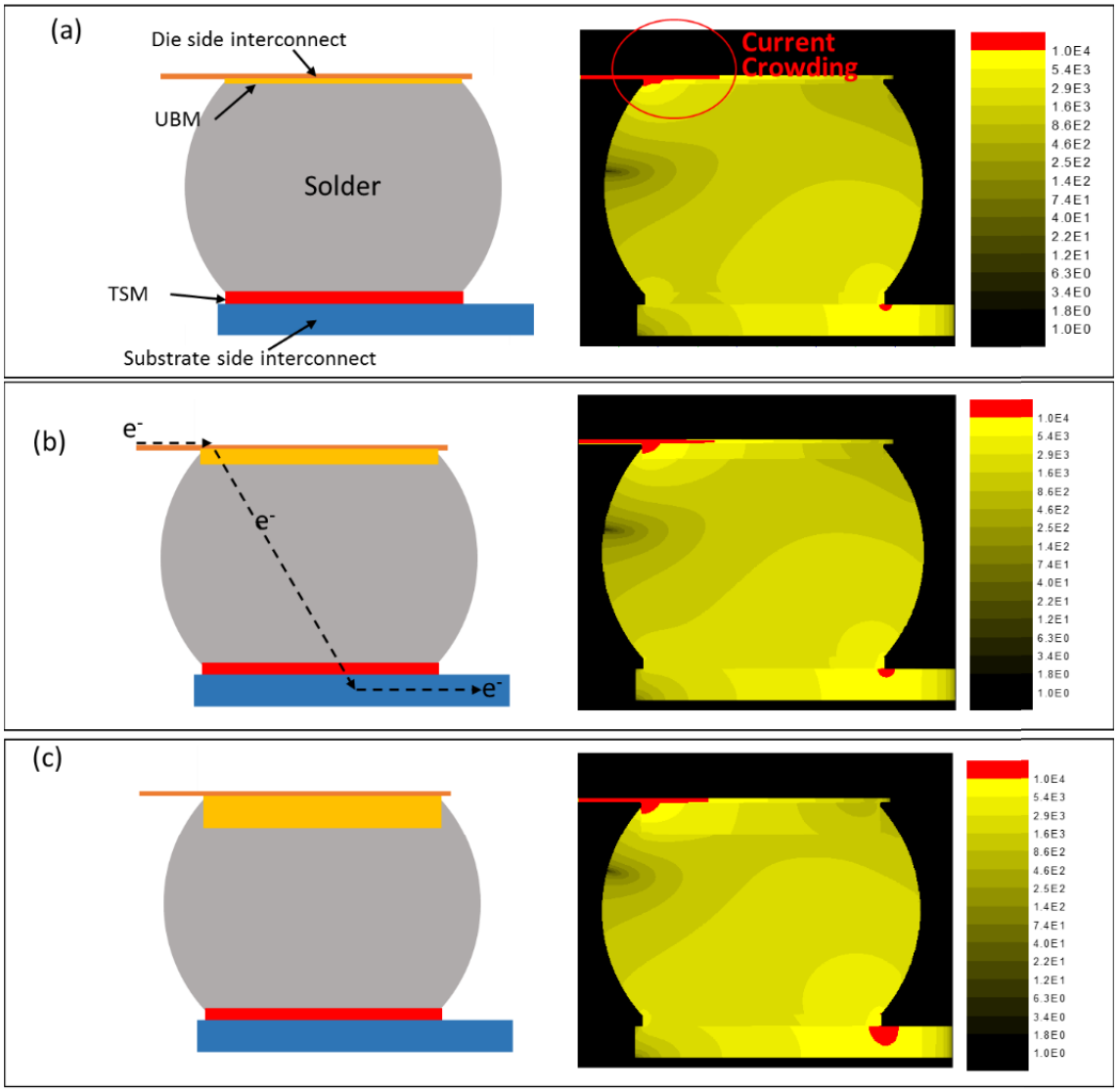

Figure 2-2. Two-dimensional current distribution simulation of 100µm diameter flip chip solder bump, with (a)1.5µm, (b) 5µm, and (c) 10µm thick UBM.

2.1.3 Multiple Reflow Issues of Sn63Pb37 Flip Chip Bumps

As shown in **Table 1-1**, the flip chip solder bump material in the old CF version of Xilinx V4/V5 packages was 95Pb5Sn high-Pb solder, while the solder material in the new Xilinx CN packages and Aeroflex sample is Sn63Pb37 eutectic SnPb. Historically, the Sn63 solder material was introduced to use organic materials instead of ceramic materials as the substrate. In the early version of the IBM C4 flip chip packages, the Pb95 high-Pb solder was used instead of the Sn63 solder with ceramic chip carrier. The high-Pb solder exhibited an excellent reliability and process forgiveness when combined with Cr/Cu-Cr/Cu/Au UBM. The consumption rate of the UBM during reflow was slow due to the low Sn concentration of Pb95 solder, which allowed the UBM to withstand prolonged reflow. Reliability concerns related to solid-state diffusion were not as serious in the high-Pb solder as in the Sn63 solder, due to the lower diffusivity of the high-Pb solder. Most of all, the high-Pb solder had a much higher melting temperature (308 to 312°C) than the Sn63 solder; the high-Pb solder did not melt during the

subsequent reflows of board attachment using the Sn63 solder. However, as the industry moved toward using organic substrates for low-cost applications, high-Pb solder could not be used as flip chip solder bump material anymore because organic substrates could not withstand the high reflow temperature of the high-Pb solder. In consequence, the industry had no choice but to use Sn63 solder and to develop compatible UBM configurations.

Another reason why Sn63 is used as the bump material is that the military and aerospace parts manufacturers are indirectly being forced to not use high-Pb solders. This is because high-Pb bumping facilities are becoming increasingly scarce; maintaining a high-Pb bumping line is not profitable any more for flip chip bumping service providers due to low volume demand. Even though there are demands in the military and space sector for high-Pb solder bumped flip chip parts, the size of the market is too small for the manufacturers to maintain the high-Pb production facilities. In addition, the large market in the commercial sector enabled rapid advancement of the plastic flip chip technologies, and the reliability of the plastic flip chip parts has become reliable enough for the server and the mainframe applications. Since the plastic parts are less expensive than the ceramic parts and reliable enough, the demand for the ceramic flip chip parts has been greatly reduced. The reduced demand of ceramic flip chip parts also reduced the demand of high-Pb solder, because high-Pb solder was only compatible with ceramic substrates.

In addition, the RoHS directive also has indirectly contributed to the increasing unavailability of high-Pb bumping facilities. Using the high-Pb solder as the flip chip bump material for the class-Y packages is, in fact, exempt from the RoHS legislation on multiple grounds [17]. First, the RoHS directive inherently does not apply to the military and space parts. Second, high melting temperature solders with more than 85% Pb are exempted, according to the Annex III, 7(a). Third, using Pb for die-level flip chip solder bumps is exempt by the Annex III, 15. However, the commercial industries have developed Pb-free flip chip technologies despite the exemptions, to prepare for the future revocation of the exemptions and to meet consumer demands of environment-friendly products. The overall advancement of the Pb-free technology in the commercial sector and the increased logistical difficulties in maintaining high-Pb bumping facilities have greatly reduced demand for the Pb-containing part production lines. Consequently, class-Y products manufacturers are having difficulties in finding reliable high-Pb bumping facilities. As a result, the new Xilinx CN packages are using Sn63 bumps instead of high-Pb bumps. Aeroflex anticipated a diminishing supply of high-Pb wafer bumping sources and initiated its high reliability flip chip qualification efforts with eutectic SbPb solder from the onset [18,19].

One of the reliability concerns related to using the Sn63 bump is the multiple reflow issue. Due to its low melting temperature, the Sn63 bumps will be reflowed during the column attach, board attach, and rework processes. There are about 10,000 flip chip solder bumps in V4 and V5, and all 10,000 bumps need to survive the subsequent reflow processes. This may appear to be a challenging task, but it is actually an old issue; although Sn63 flip chip bump is new for the space sector, it is a very mature technology for the commercial sector. The multiple reflow was once an issue in the commercial sector when the plastic substrate was first introduced, but solutions were found nearly 15 years ago. Considering Moore's law, 15 years is an extremely long time for microelectronics industries, and now the multiple reflow issue of the Sn63 bumps is considered an old issue. The industry has found reliable UBM configurations that can withstand multiple reflows of various solder materials. Materials compatibility is not a main concern when assessing the risk of failure by the multiple reflows; in modern flip chip packages, flip chip solder bumps fail during the multiple reflow mainly by workmanship issues, such as underfill voiding at the vicinity of a flip chip solder bump, not by materials issues. However, the multiple reflow is known to affect microstructure and mechanical properties of solder joints, and its effects on thermal cycling life of the packages need to be investigated.

2.1.4 Concerns from Synergistic Effects between Reliability Issues

Reliability issues of class-Y type packages, such as thermal cycling, electromigration, and multiple reflow have been extensively studied in both industry and academia for many years. Failure mechanisms of

class-Y type packages under such conditions are well understood. However, most studies were focused around conditions relevant to commercial applications, not to high reliability military and space applications. This study focused on how different reliability issues would synergistically affect each other.

2.1.4.1 Moisture Exposure on Thermal Cycling Reliability

In the previous FY12 NEPP task, the effect of moisture exposure on LP2 underfill material in Xilinx V4 and V5 was investigated [7]. Glass transition temperatures of LP2 material were reduced roughly by 30˚C after the humidity exposure. LP2 underfill material also exhibited a drop in lap shear strength from 2050 psi to 1577 psi after 7 days of exposure to 85˚C/85% RH, and remained about the same (1576 psi) after further exposure for 27 days. The FY12 results indicated that exposure to humidity would expedite underfill breakdown of class-Y packages during the thermal cycling. In the current study, the Aeroflex samples were exposed to 85˚C/85% RH for 27 days and subjected to thermal cycling from –55 to +125˚C.

2.1.4.2 Electromigration on Thermal Cycling Reliability

As explained in the section 2.1.2.1, the current density and the Joule heating are the highest at the corner of a flip chip solder bump where electrons enter during the electromigration. Consequently, the void formation initiates at the corner of the flip chip solder bump. It has been considered that the incubation time for void formation takes about 90% of the mean time to failure (MTTF), and the void propagation takes only about 10% of the MTTF [11, 20]. On the other hand, the corner of a bump furthest away from the center of the die has the highest stress from the CTE mismatch between the die and the substrate and acts as a crack initiation point [21,22]. Since both void formation and crack initiation take place at the corner of a flip chip solder bump, fatigue cracks and electromigration voids can potentially serve as nuclei for each other. If a flip chip solder bump with a preexisting electromigration void is subjected to thermal cycling stress, the pancake-type void formed by electromigration will act as a crack initiation site, just as how a surface defect acts as fatigue crack initiation site. On the other hand, if a solder bump with a preexisting crack formed by thermal cycling stress is subjected to electromigration, the void incubation period will be greatly reduced because the crack will act as a void nucleation site. In addition, a flip chip solder bump that has been previously subjected to electromigration can fail in a brittle manner when subjected to mechanical force [23,24], which indicates that electromigration may reduce thermal cycling life of flip chip solder joints.

2.1.4.3 Multiple Reflow on Thermal Cycling Reliability

Both the Xilinx CN packages and the Aeroflex daisy chain assemblies utilize the Sn63 alloy as a flip chip solder bump material. Due to its low melting temperature, the Sn63 flip chip bumps will be reflowed during the subsequent reflows. Historically, the main reliability issue related to the multiple reflow was spalling of intermetallic compounds, which causes loss of solder adhesion and dewetting of solder. During the reflow, the consumption of the UBM wetting layer takes place as the UBM wetting layer material (typically, Cu or Ni) diffuses into the molten solder through channels between intermetallic compound scallops. As the total reflow time increases during the multiple reflow, the diffusion of the wetting layer leads to full consumption to the wetting layer; thin UBMs, deposited by vacuum process such as sputtering or evaporation, are typically only about 2 μm thick and therefore can only afford limited consumption. After the wetting layer is fully consumed, the scallop-type intermetallic compounds undergo Ostwald ripening, and their morphology changes from scallop-type to spheroid. The intermetallic compounds inherently do not have strong adhesion to the adhesion layer, and the spalling of intermetallic compound occurs as the spherical intermetallic compounds detach from the adhesion layer. Since the molten solder does not have wettability to the adhesion layer, dewetting of the solder takes place after the spalling of the intermetallic compounds [25,26,27,28]. As the mainstream flip chip solder material evolved from high-Pb to Sn63 to Pb-free, the UBM material configuration has evolved accordingly to resolve the spalling issue. The modern flip chip technology is mature enough to prevent spalling and

dewetting during the multiple reflow; in modern flip chip packages, failures during the multiple reflow are mostly due to workmanship issues.

In addition to the spalling, the heat from the multiple reflow induces Kirkendall voiding in the solder joint [29].The Kirkendall voids cause embrittlement of the solder joint. Kirkendall voiding is predominant in both cases when the UBM wetting layer is Cu or electroless Ni. When Cu is the wetting layer, the Cu_6Sn_5 intermetallic compound forms first during the reflow, and the Cu_3Sn forms between Cu_6Sn_5 and Cu as reflow time increases [30]. After the reflow, when the solder joint undergoes a solid-state aging, Cu_3Sn grows further by consuming Cu_6Sn_5. Since Cu is the dominant diffusing species in this growth of Cu_3Sn, the depletion of Cu takes place at the interface between Cu_3Sn and Cu, forming Kirkendall voids [31]. When electroless Ni is the wetting layer, Ni_3Sn_4 intermetallic compound forms when molten Sn63 solder reacts with electroless Ni. The electroless Ni inherently contains 15 to 20% of P; when the Ni_3Sn_4 forms, the depletion of Ni takes place, leading to the formation of Ni_3P at the interface between the Ni_3Sn_4 and the electroless Ni layer [32]. As reflow time increases, Kirkendall voids form in the Ni_3P layer [33].

In general, microstructure and strength of flip chip solder joints are known to be influenced by multiple reflows [25,34,35,36], and for high reliability applications it must be determined whether the multiple reflows would affect the thermal cycling life of a flip chip package.

3.0 EXPERIMENTAL END RESULTS

3.1 Overview of Design of Experiment

The purpose of the experiment was to investigate synergistic effects between different reliability factors using the Aeroflex daisy chain test assemblies. The current task mainly focused on how a reliability factor would affect the thermal cycling life of the class-Y type packages. Tests conducted in the current task are summarized in the **Table 3-1**.

Table 3-1. Summary of design of experiment.

Test	Test conditions	Test purpose
Thermal cycling	–55°C to +125°C, with two different ramp rates: 214°C/min and 11°C/min	1) Characterize thermal cycling life. 2) Establish baseline reference points for other tests.
Multiple reflow followed by thermal cycling	5 reflows, followed by 214ºC/min and 11°C/min thermal cyclings	To investigate effect of multiple reflow on thermal cycling life
Vacuum thermal aging followed by thermal cycling	Vacuum thermal aging (10^{-7} torr, 135°C, 3 months), followed by 214ºC/min and 11ºC/min thermal cyclings	To investigate effect of long term vacuum exposure on thermal cycling life
Humidity exposure followed by thermal cycling	Humidity exposure (85°C/85% RH, 27 days), followed by 214ºC/min and 11C/min thermal cyclings	To investigate effect of humidity exposure on thermal cycling life
Current stressing baseline characterizations	Current stressing	Baseline experiments to characterize electromigration behavior of samples
	Current stressing followed by die shear test	To characterize the effect of electromigration on the mechanical strength of flip chip solder joints
Current stressing followed by thermal cycling	Current stressing (2×10^4 A/cm^2 at 110°C for 96 hours), followed by 214ºC/min and 11°C/min thermal cyclings	To investigate effect of electromigration on thermal cycling life

Thermal cyclings were performed from –55°C to +125°C with two different ramp rates, 214°C/min and 11°C/min, to characterize the thermal cycling life of the test samples and establish baseline reference points for other tests. To investigate the effect of multiple reflows on the thermal cycling life of the samples, 32 samples were subjected to five multiple reflows and thermal cycled. To investigate the effect of the long-term vacuum exposure on thermal cycling life, 32 samples were subjected to a vacuum thermal aging in 10^{-7} torr at 135°C for 3 months and thermal cycled. 32 samples were exposed to 85°C/85% RH for 27 days and thermal cycled to investigate the effect of the humidity exposure on the thermal cycling life. To investigate the effects of electromigration on thermal cycling life, current stressing experiments were done first to establish baseline electromigration characteristics of the samples. Die shear tests were also done on current-stressed samples without underfill to characterize the effect of electromigration on the mechanical strength of flip chip solder joints. 32 samples were subjected to current stressing of 2×10^4 A/cm^2 density at 110°C for 96 hours and thermal cycled to study the effect of electromigration on thermal cycling life of the package.

3.2 Description of the Aeroflex Samples

As explained in the previous section, the Aeroflex samples were ceramic non-hermetic daisy chained flip chip packages. Two different die sizes were utilized. The bigger die was 15.24 × 15.24 mm size and had 2853 bumps. The smaller die was 5.08 × 5.08 mm size and had 317 bumps. The daisy chain layout of the bigger die was simply a 3 × 3 repetition of the smaller die, as shown in the **Figure 3-1** (c) and (f); the bigger die was designated as a "3 × 3" die, and the smaller die was designated as a "1 × 1" die. It must be noted that the underfill fillet is longer at one edge than other edges of the dies, as shown in **Figure 3-1** (b) and (e). This longer edge represents the underfill dispense edge.

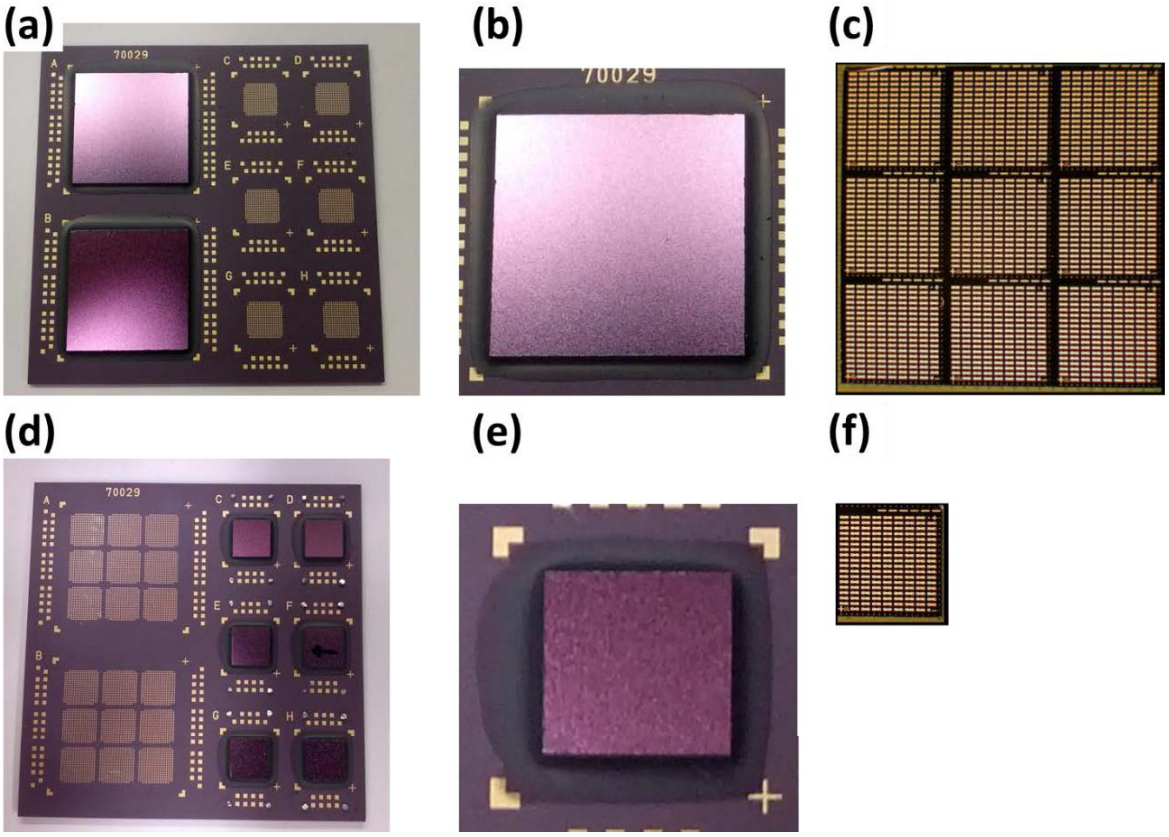

Figure 3-1. Photographs of the Aeroflex samples: (a) a sample with 3 x 3 dies; (b) an enlarged view of a 3 x 3 die(note the longer underfill fillet at the upper edge of the die); (c) the daisy chain layout of the 3 x 3 die; (d) a sample with 1 x 1 dies; and (e) n enlarged view of a 1 x 1 die(note the longer underfill fillet at the left edge of the die); and (f) the daisy chain layout of the 1 x 1 die.

Figure 3-2 (a) shows the schematic configuration of the flip chip solder joints in the Aeroflex sample. The UBM structure is Al/Ni(V)/Cu, which is one of the most commonly used UBM for Sn63Pb37 solder [18]. The substrate side metallization is electroless nickel immersion gold (ENIG). Die side pad size is 102μm diameter, with 80 μm diameter die passivation opening. The bump pitch size is 254μm, and the diameter and the height of the assembled bump are about 150μm and 80μm, respectively.

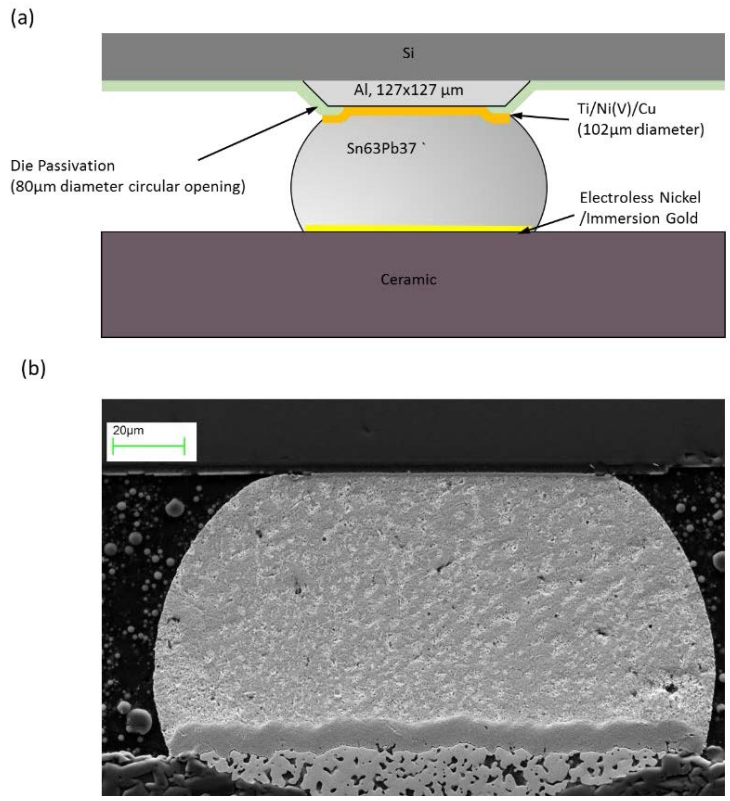

Figure 3-2. Aeroflex flip chip sample solder bump structure view of (a) schematic diagram and (b) cross-sectional SEM.

During FY10, Aeroflex completed thermal cycling tests as part of its internal R&D efforts [18]. Aeroflex performed thermal cycling tests on 3 × 3, 2 × 2, and 1 × 1 die sizes. The 3 × 3 die exhibited the shortest thermal cycling life, due to its larger size. To save schedule, 3 × 3 dies were selected as the primary sample in this study. The 1 × 1 dies were only used when performing die shear tests and baseline electromigration tests.

3.3 Thermal Cycling

Since the overall purpose of the current task was to investigate how reliability risk factors related to the non-hermeticity and the fine feature size would affect thermal cycling life of a class-Y type package, thermal cycling was performed on samples without any pre-conditioning to establish baseline reference points for other experiments. The temperature range was from –55°C to +125°C, with two different ramp rates to study the effect of the ramp rate: 214°C/min and 11°C/min. The 214°C/min test was conducted at Aeroflex, with 15 minutes of dwell time. This profile meets the requirements of MIL-STD-883 Test Method 1010. The temperature profile of the 214°C/min thermal cycling test is shown in **Figure 3-3**. The 11°C/min thermal cycling was conducted at JPL, with 4 minutes of dwell time.

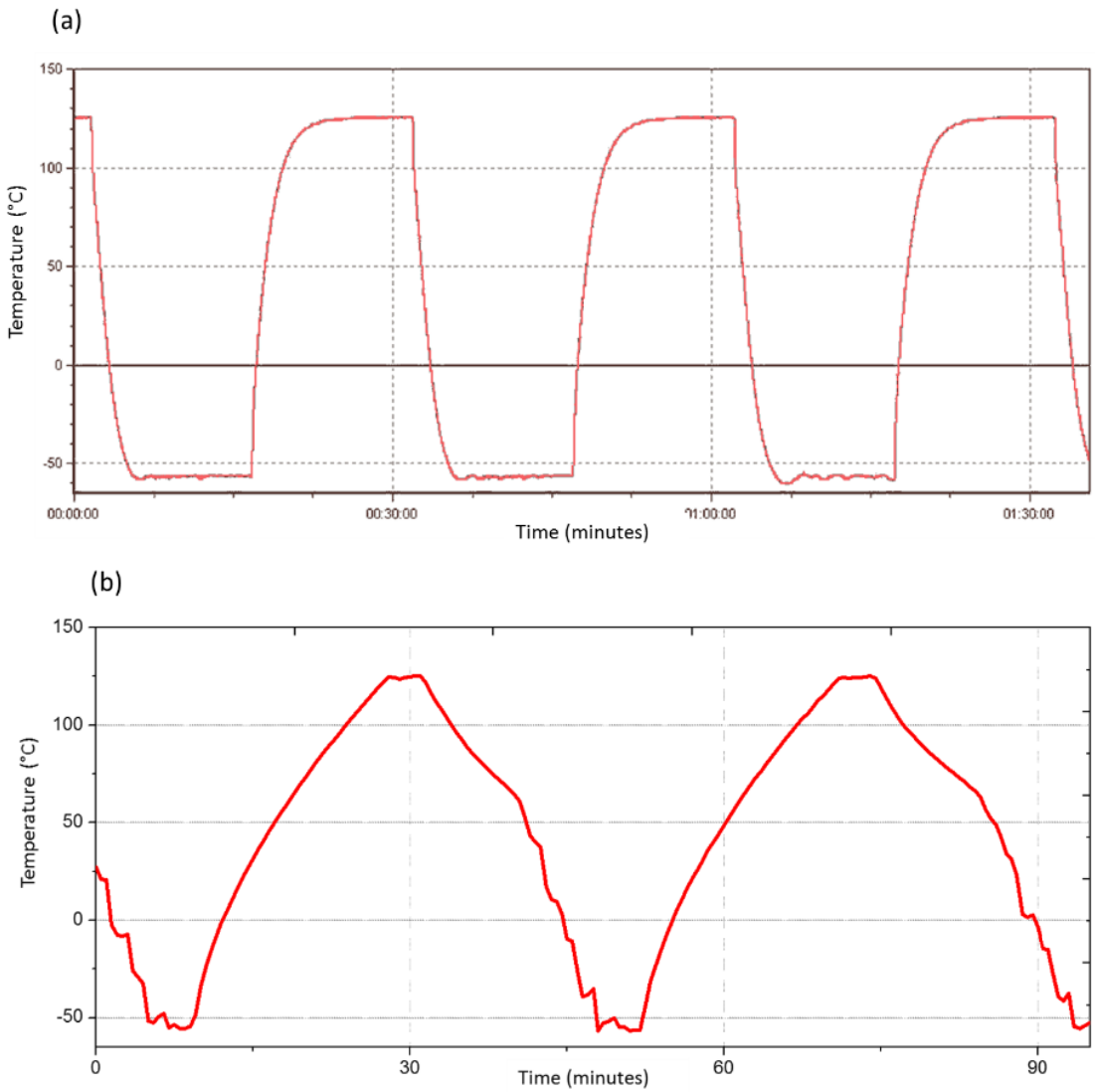

Figure 3-3. Temperature profiles of (a) 214°C/min ramp rate and (b) 11°C/min ramp thermal cycling.

The 214°C/min thermal cycling test on samples without any pre-conditionings was previously completed as part of FY10 Aeroflex internal R&D efforts. Aeroflex has performed thermal cycling tests on 3 × 3, 2 × 2, and 1 × 1 dies. Since the 3 × 3 die exhibited the shortest thermal cycling life due to its large size, 3 × 3 dies were selected as the primary sample to save schedule. The Weibull life of 3 × 3 samples was 3629 cycles. The main failure mechanism was underfill breakdown as Popelar and Thorne described in detail [18]. The underfill breakdown (see **Figure 3-4**) was a direct result of the high thermal cycle ramp rate utilized for these tests. It started with cracks within the underfill fillet that propagated under the die to the die/underfill interface. As the crack propagated at this interface, it drove through a solder interconnect, resulting in a failure in the form of an open. Failures typically occurred at the die corners where stress was the highest. In contrast, the slower ramp rate of 11ºC is anticipated to result in solder fatigue, as it will not necessarily activate underfill breakdown by allowing the underfill material to relax during transitions between hot and cold temperatures.

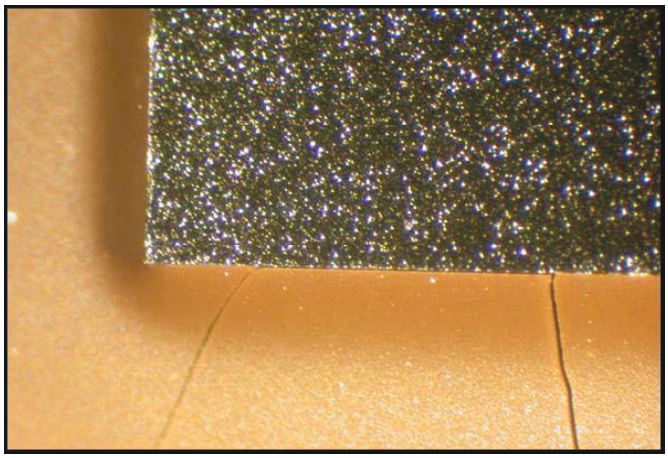

Figure 3-4. Underfill breakdown at the edge of a die with the longer underfill fillet.

3.4 Electromigration

The flip chip solder joint configuration of the Aeroflex sample is Sn63 solder bump paired with Al/Ni(V)/Cu UBM; this is a very commonly used configuration, and its electromigration characteristics have been extensively studied both in the industry and the academia [10,11,37]. Therefore, it was not necessary to perform a detailed study on electromigration failure mechanism of the Aeroflex samples. Instead, the current task mainly focused on how the electromigration would affect thermal cycling life of flip chip packages and performed only a baseline characterization of electromigration behavior. In order to study the effects of electromigration on thermal cycling life, it was necessary to pre-condition the samples by current stressing them for a certain amount of time prior to the thermal cycling tests. There were three variables for the pre-conditioning: current, temperature, and time. Since most of the previous work on electromigration of solder joint was performed with $1\sim2 \times 10^4$ A/cm^2 current density at temperatures around 100ºC, the current stressing was done under similar conditions for this study in order to take advantage of the existing studies, using time as the only pre-conditioning variable.

Typically, an electromigration experiment on flip chip solder bumps is performed on only a few pairs of daisy-chained flip chip solder bumps at an elevated temperature, inside an oven or on a hotplate. In the current task, however, it was necessary to current stress almost all the solder bumps in a die for the subsequent thermal cycling tests. The 3 × 3 die had 2,853 bumps; the large number of bumps caused an excessive amount of the Joule heating when all the bumps were current stressed. In addition, it was difficult to find a constant current source powerful enough to pass 1 A across 2,853 bumps. In order to reduce the Joule heating and lower the required power, only the first 639 bumps from the edge of the die with the long underfill fillet were current stressed, since those bumps would fail first during the thermal cycling. However, the combined resistance of the 639 bumps was still large enough to generate Joule heating large enough to heat the entire sample above the melting temperature of the Sn63 solder when 0.5 to 1 A of current was supplied. The samples had to be attached to air cooled aluminum heat sinks using thermal compound to control their temperature. **Figure 3-5** shows a schematic of the experimental setup. The temperature of the heat sink was monitored with attached thermocouples. It was expected that the temperature of the heat sink would initially rise and reach a steady state during the current stressing; however, the heat sink temperature did not increase noticeably, indicating that the thermal mass and the heat removal rate of the heat sink were large enough to overwhelm the heat generated by the sample.

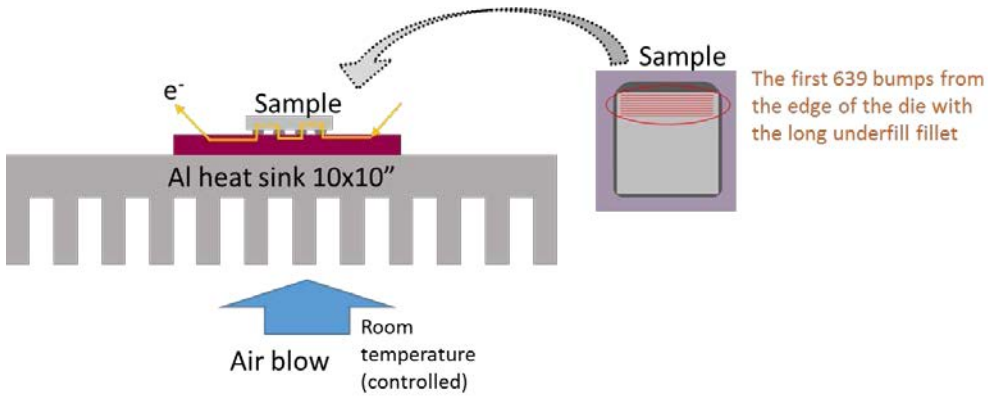

Figure 3-5. Schematic diagram of the electromigration test setup.

In a typical electromigration test where current stressing is done on only a few bumps, the combined electrical resistance of the solder bumps is small enough to assume the Joule heating from the bumps is negligible. In such cases, the temperature of the oven or the hot plate is assumed as the temperature of the solder joints, though actual temperature of the solder joints could be slightly higher or even gradually rise above the melting temperature of the solder because the heat dissipation rate reduces as a void propagates [14]. Since an external heat source, such as an oven or a hotplate, was not used in the current experiment, it was necessary to directly measure the temperature of the solder bumps. Since the total resistance of the solder bumps was large, the change of the resistance with temperature was also large enough to measure with a commonly used resistance meter. Resistance of the samples showed linear dependence when measured in the temperature range from 25 to 150ºC, as shown in the **Figure 3-6**. The temperature of the solder bumps was calculated from the resistance, which was calculated from the voltage and current during the early stage of the current stressing.

Since the die side metallization is the main source of the Joule heating and heat was withdrawn from the substrate, the temperature gradient across the solder joint was thought to be great enough to cause thermomigration; however, thermomigration was not noticeable in the current experiment, which will be discussed later in the this report.

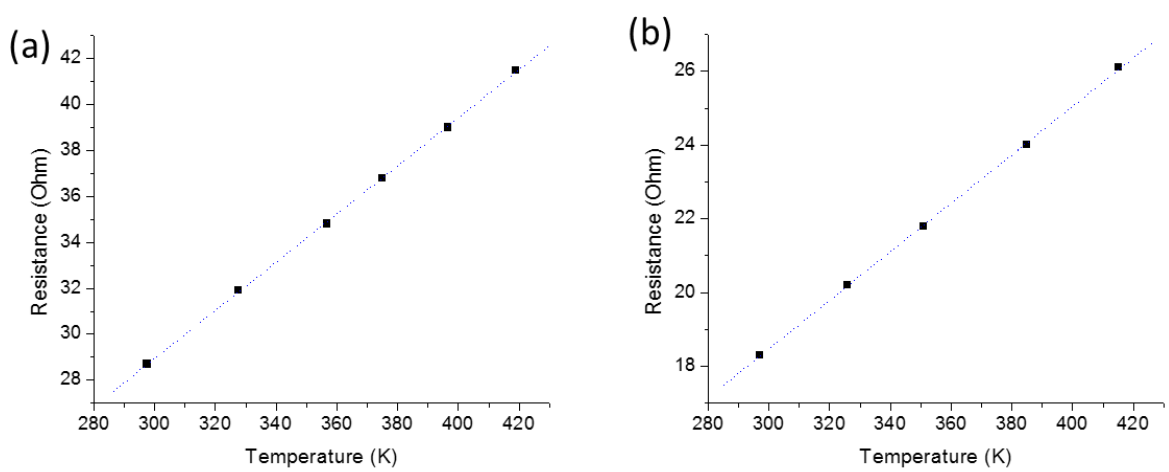

Figure 3-6. Resistance vs. temperature plot of (a) 639 bumps, and (b) 317 bumps.

Typically, electromigration experiments are performed on a few pairs of daisy chained flip chip solder bumps, by measuring the voltage drop across the daisy chain under a constant current. In such experiments, the electric resistance of the die side metallization is far greater than the resistance of the flip chip solder bumps because the solder bumps have much larger dimension. If a void forms and propagates in a solder bump, the contact area between the metallization and the solder bump reduces, increasing the resistance of the solder joint. However, the increased resistance of the solder joint is still much smaller than the resistance of die metallization. Consequently, the resistance change from the void propagation is not easily detectable. As a result, when a voltage drop is measured across the daisy chained flip chip solder bumps during a constant current stressing, the typical voltage vs. time plot looks like the one shown in the **Figure 3-7**; the voltage increase is almost undetectable until right before the complete failure of the solder joint [11]. This is similar to the case when detecting crack propagation within flip chip solder bumps during accelerated thermal cycle tests where only a fracture more than 95% of a joint cross section is detectable by a four-point probe method [38]. For this reason, the Wheatstone bridge method [39] or a sample with a circuit structure specially designed to minimize the resistance effect of the die-side metallization is used for electromigration experiments when a precise characterization on the void formation and propagation is required.

Unlike the conventional electromigration tests where only a few bumps are current stressed, 639 of 2853 bumps in the 3 × 3 dies and all 317 of 317 bumps in the 1 × 1 dies were current stressed in the current task. A voltage vs. time plot of electromigration of 317 solder bumps is shown in **Figure 3-8** (a). Unlike in **Figure 3-7**, the voltage gradually increased with time. This indicates that when current stressing is done on a large number of solder bumps, the combined resistance change from all the bumps is large enough to appear as a gradual increase of the potential. The noise of the curve in the **Figure 3-8** (a) was due to the fluctuation of the room temperature. Temperature of the heat sink was measured in-situ as shown in the **Figure 3-8** (b), which made it possible to subtract the temperature fluctuation effect from the voltage. **Figure 3-8** (c) shows voltage vs time, after subtracting the temperature effect. Every sample had slightly different initial resistance and exhibited variance in initial voltages. To account for the differences in the initial voltage, often percent voltage change was plotted versus time, as shown in the **Figure 3-8** (d).

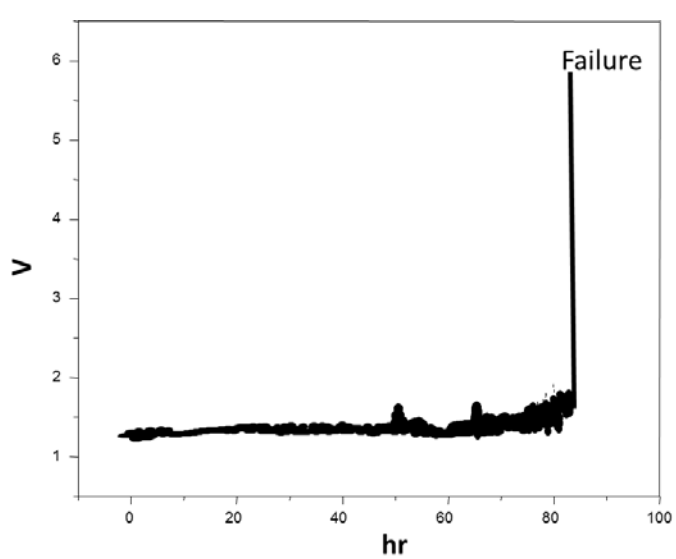

Figure 3-7. (From Choi et al. 2003 [11]) A typical potential vs. time plot of a pair of daisy chained flip chip solder bumps. Voltage increase from void formation, and propagation is virtually undetectable until almost right before the failure.

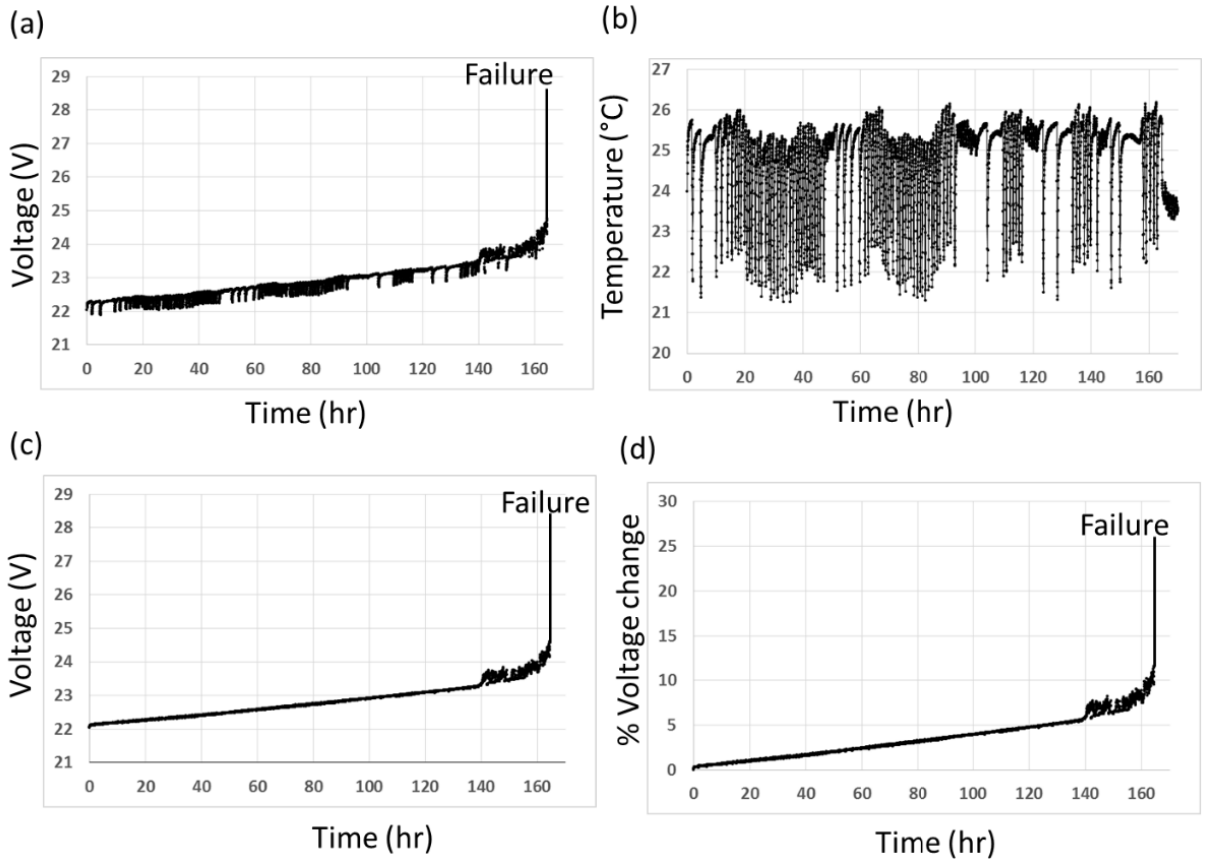

Figure 3-8. Electromigration test data plot of 317 flip chip solder bumps: (a) voltage vs. time, (b) temperature of the heat sink vs. time, (c) voltage vs. time after subtracting the temperature effect, and (d) percent voltage change vs. time after subtracting the temperature effect.

So far, the incubation time for void formation has been considered to take about 90% of the MTTF [11, 20] based on observations that voids do not appear in cross-sectioned solder bumps until right before the failure. However, if the gradual increase of the potential with time was due to the void formation and growth, it would indicate that the void formation takes place earlier than thought. The reason why voids were not observed in other studies could be due to smearing of the solder during the cross-sectioning. The smearing during the conventional cross-sectioning practices can easily hide small voids. For this reason, often a focused ion beam (FIB) is utilized when it is necessary to observe small voids in solder joints [31]. However, this will need further investigation because not all the samples exhibited gradual increase of the voltage with time; as shown in the **Figure 3-9**, the voltage of some samples initially decreased at the early stage of the electromigration experiment, then increased in the later stage.

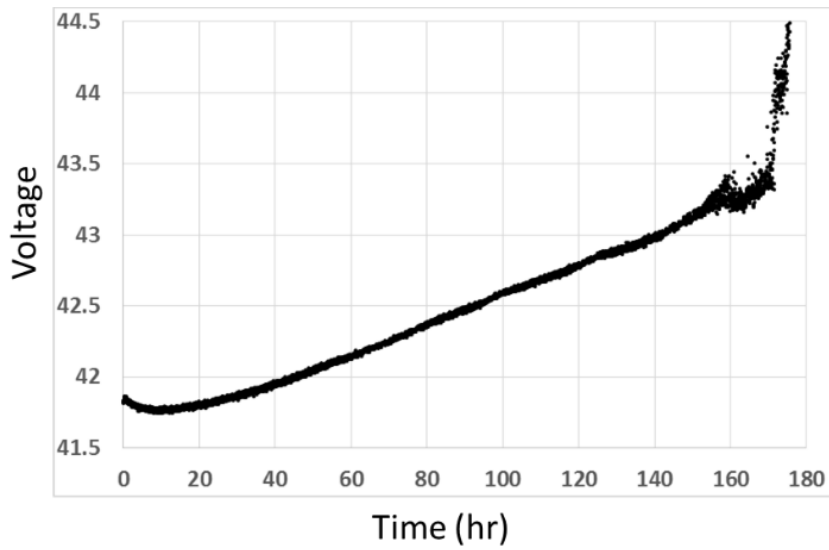

Figure 3-9. Electromigration test data plot of 639 flip chip solder bumps initial decrease in potential.

Figure 3-10 shows cross-sectional SEM micrographs of flip chip solder bump. **Figure 3-10** (a) is a solder bump without current stressing. **Figure 3-10** (b) shows a pair of solder bumps. The direction of the electron flow is depicted as the dotted arrow line. The solder bump with the cathode side at the die side formed voids at the die side. This is the typical failure mode of the SnPb solder with Al/Ni(V)/Cu UBM.

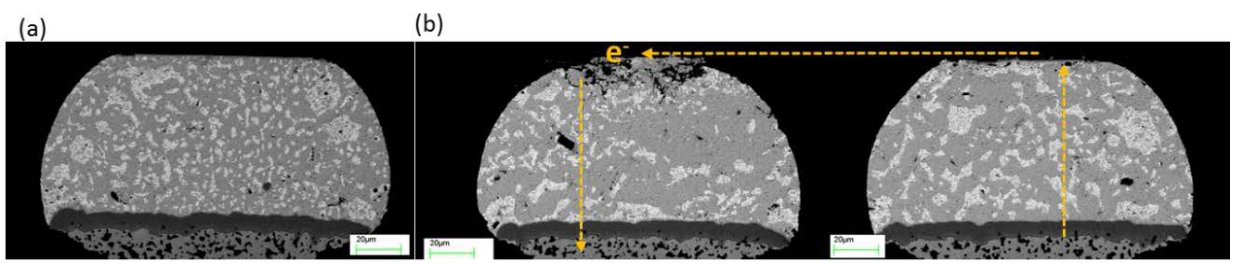

Figure 3-10. SEM images of flip chip solder bumps. showing (a) a solder bump without current stressing and (b) a pair of solder bumps, that failed after 196 hours of current stressing with 2 A/cm2 at 100ºC.

When predicting the electromigration life of a conductor, the equation empirically derived by Black is used,

$$MTTF = Aj^{-n} \exp\frac{E_a}{kT}$$

where A and n are constants, j is the current density, E_a is the activation energy, k is the Boltzmann's constant, and T is the temperature of the interconnection. In the electromigration of aluminum or copper interconnections, the exponent n is regarded as 2. Black originally determined the value of the exponent empirically, and theoretically justified it by explaining that the growth exponent is a product of electron momentum and density [40]. Later Shatzkes and Lloyd explained that the flux divergence at grain boundaries during the grain boundary self-diffusion makes the current exponent 2 [41]. There have been disagreements among the already existing studies about the value of the current exponent in electromigration of solder. In the electromigration of flip chip solder bumps, the situation is different from pure metal lines since solder mainly diffuses through lattice diffusion, and current crowding Joule heating takes place. However, in most of the works done with a statistically meaningful number of

samples, the values of n in flip chip solder bumps were still around 2. **Table 3-2** shows mean time to failure (MTTF) of the samples according to current density and temperature. If one tries to fit the numbers in **Table 3-2** into the Black's equation, one will find that the n could be even larger than 10. The number of samples per condition was only from four to six, which was not large enough to determine a statistically meaningful MTTF. In addition, because 639 solder bumps were serially connected in each test, the time to failure strongly depended on the electromigration life of the "weakest link," creating extremely large scatter of the data. In some samples, a particular bump formed voids much earlier than other bumps and made the entire daisy chain fail prematurely, while in other samples, all the solder bumps showed more or less uniform void formation. Since the experiment was done at room temperature using joule heating as the source of heat, the temperature was not precisely controlled, and there was up to 8ºC of temperature fluctuation/error, which could also have contributed to the scattering of the data. In addition, the electromigration behavior of SnPb solder depends on which one between Sn and Pb is the dominant diffusing species. Sn is known as the dominant diffusing species at room temperature; Sn diffuses faster than Pb at room temperature. At temperatures equal or higher than 100°C, Pb is the dominant diffusing species. However, the exact temperature where the change in the dominant diffusing species takes place was not determined and it is not certain at this moment which one is the dominant diffusing species at 85°C. If Sn is the dominant diffusing species at 85°C, the failure mechanism would be different from tests done at 120 and 125°C, and the test result at 85°C would not fit in to the same Black's equation as 120 and 125°C.

Table 3-2. Mean time to failure and test conditions.

Temperature (°C)	Current density (A/cm²)	MTTF (hr)
85	2	175
120	2	150.3
125	2.2	38.4

It must be also noted that the current experiment did not account for the thermomigration. All the current stressing tests in this task were performed at room temperature. The source of heat was the joule heating of the die-side metallization, and the heat was withdrawn from the substrate. Therefore, the temperature at the die side was far greater than at the substrate side. The temperature gradient across the solder bump could have been large enough to cause thermomigration. As a rough estimate, the temperature drop across the layer with solder bumps and underfill is,

$$\Delta T = R_{fc}P,$$

Where R_{fc} is combined thermal resistance of the flip chip solder bumps and the underfill, and P is the power generated by the die side metallization.

The thermal resistance R is,

$$R = t/KA,$$

Where t is the thickness of the layer, K is the thermal conductivity, and A is the area of the layer. The combined thermal resistance R_{fc} is,

$$\frac{1}{R_{fc}} = \frac{1}{R_{solder}} + \frac{1}{R_{underfill}} = \frac{K_{solder}A_{solder}}{t} + \frac{K_{underfill}A_{underfill}}{t} = \frac{K_{solder}N\pi r^2}{t} + \frac{K_{underfill}(A_{total}-A_{solder})}{t}$$

we can assume that the $K_{underfill}$ = 0.5 W/m·K [42], K_{solder} = 50 W/m·K, N = 639, t = 100μm, r = 50 μm, and A_{total} = 50 mm^2. Then, R_{fc} = 0.367 K/W.

Since the current was 1 A and the resistance was about 30Ω, then P = 30 W.

Therefore, the overall temperature drop across the layer containing the underfill and the solder bumps, ΔT, is 11ºC. Since the thickness of the layer is about 100 μm, the temperature gradient across the layer is,

$$\Delta T/t = 1100^{\circ}C/cm$$

In individual solder bumps, the temperature gradient should be smaller than 1100ºC/cm, since the thermal conductivity of solder bump is much larger than the combined thermal conductivity of the underfill and the solder bumps. Regardless, this amount of temperature gradient is known to cause thermomigration in SnPb solder bumps [43,44,45]. However, because the average temperature of the solder bumps was far lower in the current study than in the existing thermomigration studies, the diffusion of solder was far slower, and the thermomigration was not noticeable from the microstructure of the solder bumps. Nonetheless, based on the high temperature gradient, the thermomigration might have affected the current stressing results, though the measured MTTFs do not largely deviate from the results in the existing studies.

3.4.1 Die Shear Test Results on Current Stressed Flip Chip Dies

Current stressed flip chip solder bumps can fail in a brittle manner when subjected to mechanical force [23, 24]. This indicates that electromigration may reduce thermal cycling life of flip chip solder joints. To conduct the baseline characterization on the effect of electromigration on the mechanical strength of flip chip solder bumps prior to the thermal cycling studies, 1 × 1 flip chip samples without underfill were current stressed and shear tested. All 317 bumps on 1x1 die were current stressed for up to 140 hours with 2×10^4 A/cm^2 of current density at a temperature of about 90°C. It must be noted that the absence of the underfill should slightly alter the electromigration behavior of the flip chip solder bumps. Besides the void formation, stress relaxation behaviors during the electromigration tend to manifest in a more macroscopic level, such as in hillock formation or deformation. The underfill will prevent such mechanisms since it mechanically confines the solder bumps. However, the experiment in this section will still provide a general sense on how the mechanical properties of solder bumps would degrade by electromigration.

Figure 3-11 shows the fractured surfaces of the flip chip bumps after die shear tests. The flip chip solder bumps in (a) were not current stressed, while those in (b) were current stressed for 140 hours. In (b), note that one solder bump in each pair of solder bumps has a darker fractured surface than the other does. This is because all the solder bumps with cathodes at the die side had brittle failures. **Figure 3-11** items (c) and (d) are magnified images of a pair of solder bumps in (a) and (b), respectively. For solder bumps in **Figure 3-11** (c), both solder bumps are equally bright; however, for the solder bumps in **Figure 3-11** (d), the left solder bump appears darker than the other one. The solder bumps with brighter fracture surfaces have distinct shear marks, indicating that their surfaces were ductile fractured. Meanwhile, the darker surface shows the characteristics of a brittle fractured surface. This is more evident in an SEM image; **Figure 3-12**. (a) is an SEM image of a pair of solder bumps. The solder bump at the left clearly shows a typical brittle fractured surface, while the other one shows a typical ductile fractured surface. **Figure 3-12** (b) schematically depicts the electron flow in the two solder bumps. As discussed in the section 2.1.2.1, because of the current crowding, the voids only form at the die sides of the bumps that have cathodes at the die side. The void formation induces embrittlement of the solder bump, resulting in brittle fractures during the die shear tests.

The void formation and propagation also reduces the solder joint strength. **Figure 3-13(a)** shows the relationship between die shear strength and current stressing time. There is an obvious trend showing that the die shear strength reduced as the current stressing time increased. **Figure 3-13 (b)** shows the relationship between voltage increase and the current stressing time. The scatter in the voltage increase was due to the inherent differences between the samples and imprecise temperature control. Hence, the

amount of the voltage increase may better represent the amount of degradation of solder than the current stressing time. **Figure 3-13 (c)** shows the relationship between the voltage increase and the die shear strength. The correlation factor of the data in the **Figure 3-13 (c)** had a slightly higher correlation factor (–0.80) than the data in the **Figure 3-13 (a)** (–0.78). Since the shear stress is inversely proportional to the cross-sectional area, the die shear strength will be inversely proportional to the contact area subtracted by the void area. If one can find the relationship between the current stressing time and the void area, one would be able to improve the correlation between the die shear strength and the current stressing time. If we assume that the void area is proportional to the current stressing time, the contact area without the void will be inversely proportional to the square of the time.

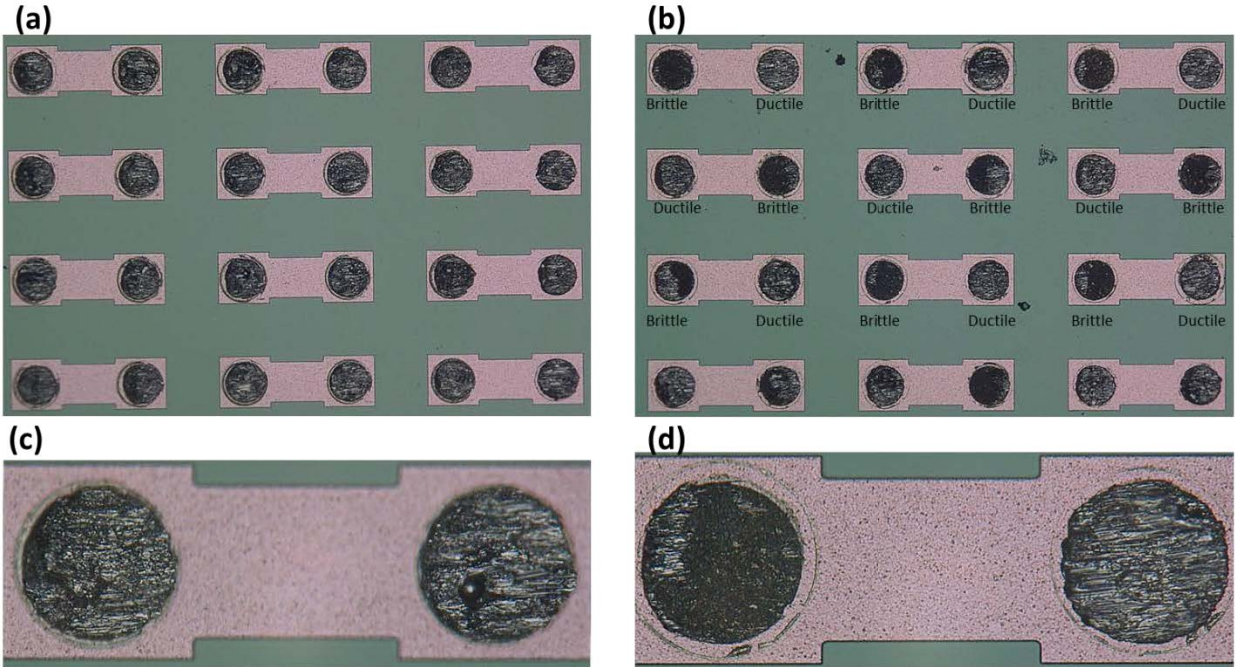

Figure 3-11. Optical microscopic images of surfaces of dies after die shear test: (a) A die without current stressing, (b) 140 hours of current stressing, (c) Magnified image of a pair of bumps in the picture (a), (d) Magnified image of a pair of bumps in the picture (b).

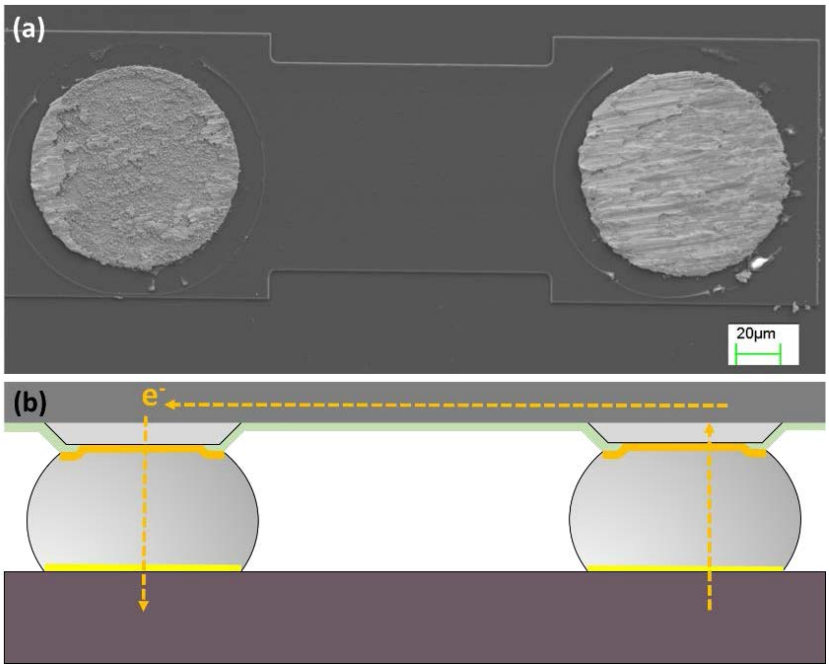

Figure 3-12. Pair of solder bumps showing (a) SEM micrograph after current stressed with 2×10^4 A/cm^2 of current density at 90°C for 140 hours and (b) schematic diagram depicting the flow direction of electrons.

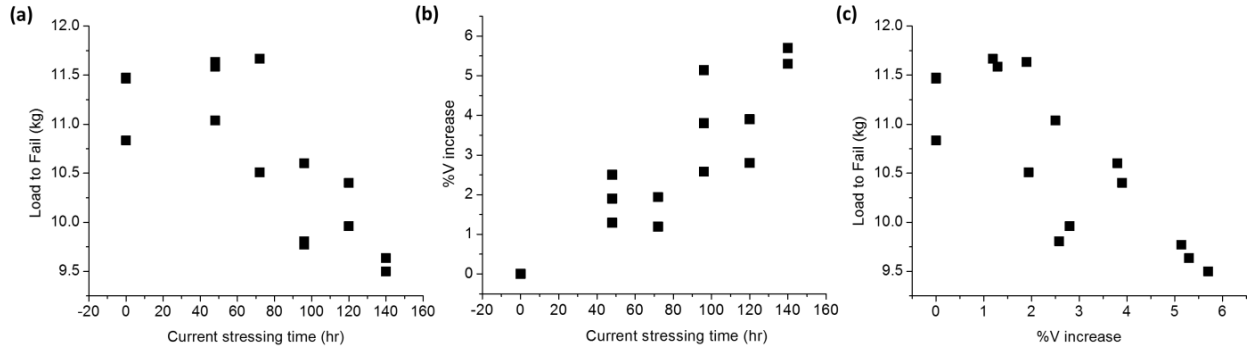

Figure 3-13. Plots showing relationship between die shear strength, current stressing time, and voltage increase: (a) relationship between die shear strength and current stressing time and (b) relationship between the voltage increase and the current stressing time (c) Relationship between die shear strength and percent voltage increase after current stressing.

The void formation and propagation also reduces the solder joint strength. **Figure 3-13** (a) shows the relationship between die shear strength and current stressing time. There is an obvious trend showing that the die shear strength reduced as the current stressing time increased. Figure **3-13** (b) shows the relationship between voltage increase and the current stressing time. The scatter in the voltage increase was due to the inherent differences between the samples and imprecise temperature control. Hence, the amount of the voltage increase may better represent the amount of degradation of solder than the current stressing time. **Figure 3-13** (c) shows the relationship between the voltage increase and the die shear strength. The correlation factor of the data in the **Figure 3-13** (c) had a slightly higher correlation factor (–0.80) than the data in the **Figure 3-13** (a) (–0.78). Since the shear stress is inversely proportional to the cross-sectional area, the die shear strength will be inversely proportional to the contact area subtracted by the void area. If one can find the relationship between the current stressing time and the void area, one would be able to improve the correlation between the die shear strength and the current stressing time. If

we assume that the void area is proportional to the current stressing time, the contact area without the void will be inversely proportional to the square of the time. However, the correlation factor between the die shear strength and the inverse square of the current stressing time did not show noticeable improvement, and this would need further studies at a more academic level. The reduction of the die shear strength was due to the growth of the void. **Figure 3-14** is the fractured surface of a die current stressed for 96 hours. Note that the area of the brittle fractured dark surface is much smaller than the dark surface of the sample current stressed for 140 hours in the **Figure 3-11** (b) and (d). From the **Figure 3-13** (a), the die shear strengths of the 96-hour current stressed dies are about 10% lower than the samples without the current stressing. Since one out of two bumps suffered damage from the electromigration, the amount of the reduction of the shear strength in the damaged solder bumps would be about 20%.

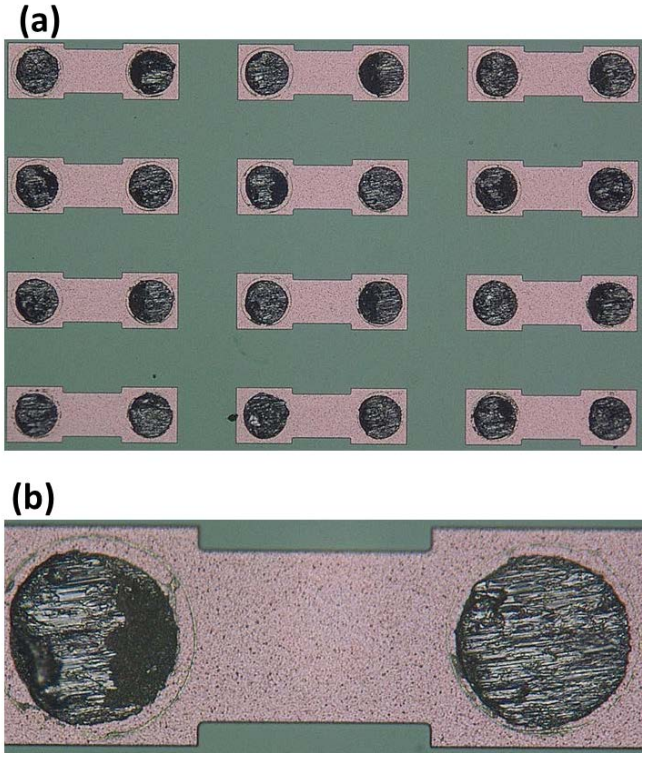

Figure 3-14. The fractured surface of a die after 96 hours of current stressing with 2×10^4 A/cm^2 current density at 90°C showing (a) the macroscopic trend of fractured surfaces and (b) a magnified view of a pair of fractured solder bumps.

3.5 Thermal Cycling Results on Pre-Conditioned Samples

Samples were pre-conditioned and thermal cycled to investigate the synergistic effects of different reliability factors on the thermal cycling life. Thermal cycling was performed from –55°C to +125°C with two different ramp rates: 214°C/min and 11°C/min.

Four different types of pre-conditionings were performed on the samples: vacuum thermal aging, humidity exposure, multiple reflow, and current stressing. 32 samples were used for each type of pre-conditioning. 16 of them were thermal cycled with 214°C/min ramp rate thermal cycling, and the other 16 were thermal cycled with 11°C/min thermal cycling.

The purpose of the vacuum thermal aging and the humidity exposure was to address the aforementioned reliability issues due to the non-hermeticity. As discussed previously, the long-term vacuum exposure, among all the constituents of the LEO environment, was considered as the most realistic potential threat to the class-Y packages. The humidity was another concern related to the non-hermeticity. Since the

package does not have the hermeticity to block the moisture, exposure to the humidity on Earth can affect the reliability of the package in space. In our FY12 NEPP task, humidity was concluded as a major threat to the underfill reliability. For the vacuum thermal aging, samples were vacuum thermal aged in 10^{-7} torr vacuum at 135ºC for 3 months. For the humidity exposure, samples were exposed to 85°C/85% RH for 27 days.

As discussed previously, both the Aeroflex samples and the new Xilinx CN packages use the Sn63 alloy as the flip chip solder bump material. Since the Sn63 solder is also used for the column attachment and the board assembly, the flip chip solder bumps will be reflowed during the subsequent processes. The multiple reflow is known to affect the interfacial structure and the mechanical properties of solder joints. The effect of multiple reflows on thermal cycling life was investigated for the high reliability applications. Samples were subjected to five multiple reflows in the Aeroflex reflow oven and then thermal cycled.

As shown in the section 3.4.1, the electromigration reduces mechanical strength of the flip chip solder bumps. To investigate the effect of the electromigration on thermal cycling life, samples were current stressed with 2×10^4 A/cm^2 current density at 110°C for 96 hours and thermal cycled.

The 214ºC/min ramp thermal cycling results are summarized in **Table 3-3**. As a baseline thermal cycling result, Aeroflex's FY10 thermal cycling results were used. The baseline samples, without any preconditioning, had a Weibull life of 3629 cycles. The thermal cycling lives of the both the vacuum thermal aged and the multiple reflowed samples greatly increased (roughly by 50%). The current-stressed samples had slightly increased thermal cycling life (10%) than the baseline samples, though the Weibull fit had noticeably reduced. In contrast with other samples, the humidity exposed sample showed 33% reduction of thermal cycling life. As for the 11ºC/min ramp rate thermal cycling, the samples were thermal cycled up to 3000 cycles. No samples failed or showed defects.

All the samples failed during the 214ºC/min ramp rate thermal cycling failed by underfill breakdown, described in the section 3.3 and [18]. As noted above, underfill breakdown is a function of the high ramp rate for this thermal profile. As discussed in section 3.4.1, the solder bumps with their cathodes at the die side should experience about 20% reduction in their shear strength. However, the current-stressed samples still did not show a reduced Weibull life. This indicates that the underfill integrity has a greater influence on the thermal cycling life than the solder bump strength. If the failure mechanism were driven to solder fatigue, it is possible that some effect due to current stressing would be observed.

Ultimately, the thermal cycle results at 214ºC/min demonstrate the effect of moisture on the underfill breakdown failure mechanism. The moisture-conditioned samples failed with a Weibull life 33% lower than the baseline. When an underfill material is exposed to heat, moisture removal and additional curing takes place. Both the vacuum thermal-aging samples and the multiple-reflow-conditioned samples were exposed to a large amount of heat. The current stressed sample was pre-conditioned in the ambient temperature, but the underfill adjacent to the current stressed solder bumps was exposed to additional amounts of heat because the Joule heating raised the temperature of the solder bumps to 110ºC. As a result, the vacuum thermal aging and multiple reflow preconditions resulted in a large increase (50%) in Weibull life compared to the baseline. The current-stressed samples also exhibited a 10% increase in the Weibull life due to the exposure to the small amount of heat from the Joule heating. Thermal cycling at 11ºC/min showed no failures after 3000 cycles, suggesting that the effects of preconditioning are mitigated at slow thermal cycle ramp rates. This is an encouraging finding in that use conditions in space are more apt to have slow thermal ramp rates as opposed to fast.

During the FY12 NEPP task at JPL, the LP2 underfill in the Xilinx CF packages was vacuum thermal aged and tested. The LP2 underfill exhibited increased adhesive strength, reduced CTE, and a slightly increased Tg [7]. All these changes indicated that the LP2 underfill should perform better after the vacuum thermal aging. Therefore, the current result on the vacuum-thermal-aged Aeroflex samples is in accordance with the FY12 NEPP task results on the underfill. The multiple reflowed sample also showed

an improved thermal cycling life, which should be also due to property improvement of the underfill. Both the multiple reflowed samples and the vacuum-thermal-aged samples were subjected to additional heat. If an underfill is subjected to heat, an additional cure can take place, as long as the temperature is not excessively high. If the temperature is too high, underfill molecules will scission, and the underfill will go through thermal degradation. The heat will also drive out plasticizers and moisture. All these will improve properties of underfill. Often spacecraft electronics must be subjected to heat after the assembly, for example, during the Planetary Protection process. The current result implies that such thermal exposure will improve the reliability of the class-Y packages. It also implies that the class-Y parts can become more reliable by baking.

The reduced thermal cycling life of the humidity-exposed samples is also in accordance with our FY12 NEPP task results. The properties of the LP2 underfill material changed towards the undesirable direction after the humidity exposure; the LP2 material showed reduced lap shear strength, reduced Tg, and increased CTE. Although the underfill used in the Aeroflex sample is not LP2, the Aeroflex underfill and the LP2 probably degrade in a similar manner. The moisture absorption of an underfill depends on the amount of exposure time and temperature; and therefore, short exposure to water during the assembly and inspection processes, such as cleaning or acoustic microscopy, will not cause noticeable degradation of the underfill. Moisture can be removed from an underfill by baking, but the underfill properties can only be partially recovered once an underfill material suffers property degradation by moisture [6]. Therefore, minimizing exposure of class-Y parts to humidity would be crucial in maintaining a high level of reliability.

Table 3-3. Thermal cycling results for 214ºC/min pre-conditioned samples.

Condition	Weibull Life	Weibull Slope	Weibull Fit R2
Baseline (no precondition)	3629	6.3	0.9613
Vacuum Thermal aging (10^{-7} torr, 135ºC, 3 months)	5474	8.9	0.9402
Humidity exposure 85°C/85%, 27 days)	2438	7.5	0.9717
Multiple reflow (5X reflows)	5237	6.4	0.9348
Current stressing (96 hours, 2 x 10^4 A/cm^2 at 110ºC)	3978	4.9	0.8013

4.0 SUMMARY

To achieve increased functional density and operational frequency, modern space FPGA devices (such as the Xilinx V5 high speed ASIC), the Aeroflex UT1752FC [19], and similar devices, are packaged in a non-hermetic ceramic flip chip form. In order to bring this package type into the QML system, the class-Y category was defined for non-hermetic ceramic flip chip packaging. JPL was tasked by NEPP to investigate the reliability concerns of the class-Y type packages. Aeroflex has been qualifying their processes using their internal R&D class-Y type samples. In early 2012, JPL and Aeroflex initiated a collaboration to study reliability of the Aeroflex flip chip assembly technology. The current task investigated reliability issues related to non-hermeticity, fine feature sizes, and high power characteristics of the class-Y type packages. In the previous NEPP tasks, long-term vacuum exposure and humidity had been identified as the most realistic potential threats to the packaging materials of the class-Y packages. The Aeroflex samples were subjected to vacuum thermal aging or humidity and thermal cycled, to investigate the effect of the environmental exposure to the thermal cycling life. To investigate the reliability issues related to the fine feature size, the Aeroflex samples were subjected to current stressing and thermal cycled. The purpose was to investigate the effect of electromigration on thermal cycling life of the interconnection. In addition, the effect of the multiple reflows on the thermal cycling life was investigated. The Aeroflex samples use Sn63 as the flip chip solder bump material, and the Sn63 bumps will be reflowed during the subsequent assembly processes. It was concluded that the underfill integrity mainly determines the thermal cycling life of the packages for thermal cycle profiles with high ramp rates. Although the current stressing decreased the mechanical strength of the flip chip solder bumps, the thermal cycling life of the packages did not decrease. The packages mainly failed by underfill breakdown. Both vacuum thermal aging and multiple reflows improved the properties of the underfill, improving the thermal cycling life of the package. However, humidity exposure degraded the underfill, and the package exhibited a reduced thermal cycling life. Since exposure to elevated temperatures during the vacuum thermal aging and the multiple reflows had the effect of removing moisture from the underfill, the results demonstrate the effect of moisture on the underfill breakdown failure mechanism.

Thermal cycle results for 11ºC/min showed no failures after 3000 cycles. Hence, the effect of moisture is mitigated for thermal cycle profiles with slow ramp rates. In this case, the predominant failure mechanism was likely solder fatigue. Continued thermal cycling at 11ºC/min will be required to determine if there are any effects of vacuum thermal aging, moisture exposure, multiple reflows, or current stressing on solder fatigue life. To date, however, this is an encouraging result in that use conditions will typically exhibit slow thermal ramp rates as opposed to fast.

The Xilinx CN package also utilizes 63Sn solder for its flip chip interconnects. However, to the extent that the UBM and underfill materials are different from those of the Aeroflex technology, a separate set of reliability assessments will be required to demonstrate a level of reliability comparable to that of the Aeroflex package. As is, the Aeroflex technology has demonstrated a high level of reliability required for qualifying class-Y non-hermetic ceramic flip chip packaging for space applications.

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ACRONYMS AND ABBREVIATIONS

ASIC	application-specific integrated circuit
CTE	coefficient of thermal expansion
DLA	Defense Logistics Agency
ENIG	electroless nickel immersion gold
FIB	focused ion beam
FPGA	field programmable gate array
LEO	low-Earth orbit
LGA	land grid array
MTTF	mean time to failure
NEPP	NASA Electronic Parts and Packaging (Program)
QML	Qualified Manufacturing List
RH	relative humidity
RoHS	(European Union) Restriction of Hazardous Substances
SEM	scanning electron microscope
Tg	glass transition temperature
UBM	under bump metallurgy