Compendium of Test Results of Recent Single Event Effect Tests Conducted by the Jet Propulsion Laboratory

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***Abstract*—This paper reports heavy ion and proton-induced single event effect (SEE) results from recent tests for a variety of microelectronic devices. The compendium covers devices tested over the last two years by the Jet Propulsion Laboratory.**

***Index Terms*—Single event effects, compendium, analog switches, ADC, oscillators, SDRAM, FPGA, drivers, microprocessors, voltage comparator, and voltage regulator.**

I. Introduction

MICROELECTRONICS used in space systems must survive and operate in various radiation environments. To ensure both survival and functionality of these devices for a specific mission, accelerated ground-based testing is required to define their susceptibility to single event effects (SEEs) caused by cosmic rays and heavy ions. The data presented in this paper were acquired by JPL to characterize the susceptibility of potential spacecraft microelectronics to single event latchup (SEL), single event upset (SEU), single event functional interrupt (SEFI), and single event transient (SET). This compendium provides a summary of SEE data acquired within the last two years.

II. Experimental Procedure

A. Test Facilities

A variety of ion facilities are available for SEE testing. The criterion to select a test facility may include scheduling, ion range, and/or programmatic expenses. A high level view of the facilities used is outlined below. The facility websites [1]-[4] provide a detailed view of available ions, energies, and facility capabilities that are beyond the scope of this paper.

1) Heavy Ion Facilities

Heavy ion measurements were performed at the Brookhaven National Laboratory (BNL) and Texas A&M University Cyclotron (TAM) facilities. The BNL facility uses a twin Tandem Van De Graaff accelerator and TAM uses an 88" cyclotron. Both facilities are capable of providing a range of particle beams and energies for radiation effects testing. The longer-range ions at TAM allow most of the irradiations to be performed in air, whereas all testing at BNL took place in vacuum. Intermediate Linear Energy Transfer values (LETs) were acquired either through the use of degrader (TAM only) or by changing the angle of incidence of the ion relative to the device under test (DUT), changing the effective LET.

2) Proton Facilities

Proton tests were performed at the University of California, Davis (UCD) Crocker Nuclear Laboratory (CNL) and at the Indiana University Cyclotron Facility (IUCF). Much of the work associated with recent proton testing has been associated with displacement damage effects, and are included here. The majority of the representative proton data in this compendium is complimentary to heavy ion data, and was acquired to evaluate SEE rates for proton environments.

B. Experimental Methods

Details concerning experimental methodology, including data acquisition, ion selection, biasing conditions, etc., vary from experimenter to experimenter and device to device. In many instances, devices were tested both at room temperature and at elevated temperature; results are shown for both instances. Generally speaking, the procedure used by experimenters followed the procedures documented in the ASTM F1192 or JEDEC JESD57 standards for single-event testing [5], [6]. For details concerning the specifics of a test, please review the associated test report.

III. Data Organization

This compendium is intended to serve as a reference list for tested devices. The data tables contain abbreviated information mainly due to spatial constraints. It is highly recommended that the reader review the referenced article or

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contact the principal investigator (PI) to acquire details concerning the data and test methodologies. Much of the SEE data presented here is dependent on the device's bias and circuit configuration; e.g., SET data depends strongly on their output load; SEFI data are interpretive depending upon what the test defines as a SEFI. Generally speaking, the worst-case results are presented, but it is highly recommended that the reader seek out the test report. Data that has not been previously published but has a formal test report will be released to the JPL parts radiation database [7]. Contact the principal investigator if data is not found on the database.

When possible, LET thresholds were shown to lie between a set of tested energies, otherwise they are simply shown to be at or below a certain value or not seen at the highest tested LET. SEE results have been combined on a single line. For most SEL results, only the LET thresholds have been provided. Saturated cross-sections and thresholds are provided for SEFI, SEU, and SET where available. Unless otherwise noted, all LET values are in MeV•cm^2/mg and all cross-sections in cm^2/device.

Table I lists the abbreviations for the PIs and Table II lists the acronyms, abbreviations, and conventional symbols used in Table III. Table III provides the results of the SEE tests.

TABLE I
LIST OF PRINCIPAL INVESTIGATORS

PRINCIPAL INVESTIGATOR	ABBREVIATION
PHILIPPE ADELL	PA
GREG ALLEN	GA
FAROKH IROM	FI
LEIF SCHEICK	LS

TABLE II
ACRONYMS, ABBREVIATIONS, AND CONVENTIONAL SYMBOLS

ABBREVIATION	DEFINITION
ADC	ANALOG TO DIGITAL CONVERTER
ADI	ANALOG DEVICES, INC.
ASIC	APPLICATION-SPECIFIC INTEGRATED CIRCUIT
CMOS	COMPLEMENTARY METAL OXIDE SEMICONDUCTOR
CPU	CENTRAL PROCESSING UNIT
DRAM	DYNAMIC RANDOM ACCESS MEMORY
DUT	DEVICE UNDER TEST
FPGA	FIELD PROGRAMMABLE GATE ARRAY
H	HEAVY ION TEST
I	INTERNAL DOCUMENT (CONTACT PI FOR SOURCE DATA)
I/O	INPUT/OUTPUT
IBM	INTERNATIONAL BUSINESS MACHINE
LET	LINEAR ENERGY TRANSFER (MEV•CM^2/MG)
LET_{TH}	LINEAR ENERGY TRANSFER THRESHOLD
LTC	LINEAR TECHNOLOGY
MOSFET	METAL OXIDE SEMICONDUCTOR FIELD EFFECT TRANSISTOR
MUX	MULTIPLEXOR
NAND	NOT AND LOGICAL OPERATION
OP AMP	OPERATIONAL AMPLIFIER
PI	PRINCIPAL INVESTIGATOR
σ	CROSS-SECTION
σ_{SAT}	SATURATED CROSS-SECTION
SDRAM	SYNCHRONOUS DYNAMIC RANDOM ACCESS MEMORY
SEE	SINGLE EVENT EFFECT
SEFI	SINGLE EVENT FUNCTIONAL INTERRUPT
SEL	SINGLE EVENT LATCHUP
SET	SINGLE EVENT TRANSIENT
SEU	SINGLE EVENT UPSET
TI	TEXAS INSTRUMENTS

TABLE III
SEE RESULTS

PI	Test Date	Device	Function	Mfg.	Tech-nology	Test Type	Test Site	Test Results	Ref.
ADC, 24-bit									
FI	7/30/2008	AD7760BSVZ	ADC, 24-bit	ADI	BiCMOS	SEL	TAM	LET_{th} < 8.3 @ 85°C	[7]
Analog Switches/MUXs									
GA	10/26/2009	HS9-303ARH-Q	Analog Switch	Intersil	CMOS	SET	TAM	LET_{th} < 84.6, Static Mode	[7]
Logic									
PA	6/9/2008	NL17SZ00	NAND Gate	ON Semi	CMOS	SEL	BNL	LET_{th} > 75 @ 85°C	[7]
PA	6/9/2008	NL17SZ125	Buffer, 3-state	ON Semi	CMOS	SEL	BNL	LET_{th} > 75 @ 85°C	[7]
PA	6/9/2008	NL17SZ74	D Flip Flop	ON Semi	CMOS	SEL	BNL	LET_{th} > 75 @ 85°C	[7]
PA	6/9/2008	NL17SZ14	Inverter	ON Semi	CMOS	SEL	BNL	LET_{th} > 75 @ 85°C	[7]
PA	6/9/2008	IDTQS4A210	MUX/DEMUX	IDT	CMOS	SEL	BNL	LET_{th} > 75 @ 85°C	[7]
Microprocessor									
FI	8/13/2009	IBM PowerPC 750FX	PowerPC Processor	IBM	CMOS	SEU/SEL	TAM	No SEL SEU LET_{th} < 0.8	[8]
FI	10/7/2009	IBM 750FX	PowerPC Processor	IBM	CMOS	SEU/SEL	IUCF/ UCD	No SEL SEU $Energy_{th}$ < 6.9 MeV	[8]
FI	2/11/2009	MC7447A	PowerPC Processor	Freescale	CMOS	SEU/SEL	IUCF/ UCD	No SEL SEU $Energy_{th}$ < 6.6 MeV	[8]

PI	Test Date	Device	Function	Mfg.	Tech-nology	Test Type	Test Site	Test Results	Ref.
FI	9/1/2008	MC7447A	PowerPC Processor	Freescale	CMOS	SEU/SEL	TAM	No SEL SEU $LET_{th} < 1.7$	[8]
Miscellaneous									
FI	7/30/2008	VIRENA	ASIC	SRI	CMOS	SEL	TAM	$LET_{th} > 85$ @ 85°C	[7]
FI	11/11/2008	MV64460	Bridge Chip	Marvell	CMOS	SEU/SEFI	TAM	SEU $LET_{th} < 1.7$ High current SEFIs	[8]
FI	2/11/2009	MV64460	Bridge Chip	Marvell	CMOS	SEU/SEFI	IUCF/ UCD	SEU $Energy_{th} < 21$MeV High current SEFIs	[8]
FI	7/30/2008	AD2S80A	Resolver to Digital Converter	ADI	BiMOS	SEL	TAM	$LET_{th} > 85$ @ 85°C	[7]
FI	8/13/2009	SI9112DY	Switch Mode Controller	Siliconix	CMOS	SEL	TAM	$23 > LET_{th} > 27$ @ 25°C $19 > LET_{th} > 11$ @ 85 C	[7]
FI	7/30/2008	BCM5421KPF	Transceiver, LAN	Broadcom	CMOS	SEL	TAM	Extremely sensitive to heavy ions (contact investigator for further details)	[7]
Non-Volatile Memory									
FI	7/30/2008	S29GL512	NOR Flash	Spansion	CMOS	SEU	TAM	Destructive high current spikes in PROGRAM Mode	[7]
FI	1/12/2009	K9G8G08U0A	8Gb MLC Flash	Samsung	CMOS	SEU/SEL	Finland	SEL $LET_{th} < 35$ @ 25°C SEU $LET_{th} < 4$	[9]
FI	1/12/2009	K9F8G08U0M	8Gb SLC Flash	Samsung	CMOS	SEU/SEL	Finland	SEL $LET_{th} < 35$ @ 25°C SEU $LET_{th} < 4$	[9]
FI	3/29/2009	MT29F8G08U0M	8Gb SLC Flash	Micron	CMOS	SEE	TAM	Destructive high current spikes in PROGRAM Mode	[10]
FI	3/29/2009	K9F8G08U0M	8Gb SLC Flash	Samsung	CMOS	SEE	TAM	Destructive high current spikes in READ and PROGRAM Mode	[10]
FI	5/8/2008	K9G8G08U0A	8Gb MLC Flash	Samsung	CMOS	SEU	BNL	No SEL SEU $LET_{th} < 4$	[10]
FI	9/1/2008	K9G8G08U0A	8Gb MLC Flash	Samsung	CMOS	SEE	TAM	Destructive high current spikes in READ and PROGRAM Mode	[10]
FI	10/29/2008	S29GL512	NOR Flash	Spansion	CMOS	SEU/SEL	BNL	No SEL SEU $LET_{th} < 4$	[7]
FI	2/11/2009	S29GL512	NOR Flash	Spansion	CMOS	SEU/SEL	UCD	No SEL SEU $Energy_{th} < 20$ MeV	[7]
Op Amps									
FI	5/8/2008	LT1498	Quad Op Amp	LTC	Bipolar	SET	BNL	$LET_{th} < 8$	[7]
LS	1/15/2010	AMP01	Precision Op Amp	ADI	Bipolar	SET	BNL	SET > 200 mV @ LET = 15	[7]
LS	10/26/2009	OP470	Quad Op Amp	ADI	Bipolar	SET	TAM	SET > 200 mV @ LET = 5	[7]
LS	12/1/2009	OP470	Quad Op Amp	ADI	Bipolar	SET	BNL	SET > 200 mV @ LET = 5	[7]
FI	8/13/2009	TS951ILT	Low Power Op Amp	STMicro	CMOS	SEL	TAM	$LET_{th} > 85$ @ 85°C	[7]
FI	8/13/2009	MAX4194	Instrumentation Amp	Maxim	CMOS	SEL	TAM	$LET_{th} > 85$ @ 85°C	[7]
Power Conversion									
FI	8/13/2009	UCC2626	DC Motor Driver Controller	TI	Bipolar	SEL	TAM	$LET_{th} > 85$ @ 85°C	[7]
PA	12/17/2007	LS2803R3S/EM	DC/DC Converter	IR	Bipolar/ MOS	SET	TAM	No SEL and SET > 20 mV @ LET = 51.5 for full input voltage range and load	[7]

PI	Test Date	Device	Function	Mfg.	Tech-nology	Test Type	Test Site	Test Results	Ref.
PA	5/8/2008	LS2803R3S	DC/DC Converter	IR	Bipolar/ MOS	SET	BNL	No SEL and SET > 20 mV @ LET = 51.5 for full input voltage range and load	[7]
PA	5/8/2008	LS2805S	DC/DC Converter	IR	Bipolar/ MOS	SET	BNL	No SEL and SET > 20 mV @ LET = 51.5 for full input voltage range and load	[7]
PA	5/8/2008	LS2812D	DC/DC Converter	IR	Bipolar/ MOS	SET	BNL	No SEL and SET > 20 mV @ LET = 51.5 for full input voltage range and load	[7]
GA	10/26/2009	HS-1825ARH	Dual Output PWM	Intersil	BiCMOS	SET/SEL	TAM	SET LET_{th} < 84.6 SEL LET_{th} > 84.6 @ 125°C	[7]
GA	10/26/2009	HS-4423BRH	Power MOSFET Driver	Intersil	BiCMOS	SET/SEL	TAM	SET LET_{th} > 84.6 static SET LET_{th} < 84.6 dynamic	[7]
FI	8/13/2009	HV9112NG	PWM Controller	Supertex	CMOS	SEL	TAM	LET_{th} > 85 @ 85°C	[7]
SDRAM									
PA	7/30/2008	DS5108	SDRAM	Elpida	CMOS	SEL	TAM	LET_{th} > 85 @ 125°C	[7]
FI	10/29/2008	MT46V64M8	SDRAM	Micron	CMOS	SEU	BNL	LET_{th} < 8	[7]
PA	11/11/2008	EDS5104ABTA-75	SDRAM, 512Mbits	Elpida	CMOS	SEU	TAM	LET_{th} > 2.7 $\sigma_{sat} \sim 2\times10^{-1}$/device	[7]
FI	2/11/2009	MT46V64M8	SDRAM 64Mbits	Micron	CMOS	SEU/SEL	IUCF	No SEL @ 50 MeV SEU $Energy_{th}$ < 50 MeV	[7]
PA	9/1/2008	EDS5104ABTA-75	SDRAM, 512Mbits	Elpida	CMOS	SEFI	TAM	SEFI 1: recovered by mode register, LET_{th} > 3.8 and $\sigma_{sat} \sim 1\times10^{-3}$/device SEFI 2: > 1,000 errors in a row, LET_{th} > 5.4 and $\sigma_{sat} \sim 1\times10^{-4}$/device, fixed by rewriting or power cycle	[12]
Voltage Comparator									
LS	12/27/2007	LM139	Quad Comparator	Various	Bipolar	SET	IUCF	SET > 200 mV @ 15 MeV (effective)	[7]
LS	1/15/2010	LM119	Dual Comparator	NSC	Bipolar	SET	BNL	SET > 200 mV @ LET = 60	[7]
LS	10/26/2009	LM139	Quad Comparator	NSC	Bipolar	SET	TAM	SET > 200 mV @ LET = 15	[7]
Voltage Reference									
LS	10/26/2009	LT1009	Voltage Reference	LTC	Bipolar	SET	TAM	SET > 200 mV @ LET = 15	[7]
LS	10/26/2009	IS1009	Voltage Reference	Intersil	BiCMOS	SET	TAM	SET > 200 mV @ LET = 15	[7]
FI	8/13/2009	MAX6050	Voltage Reference	Maxim	CMOS	SEL	TAM	LET_{th} > 85 @ 85°C	[7]
Voltage Regulator									
FI	12/17/2007	RH-117H	Voltage regulator	LTC	Bipolar	SET	TAM	+SET LET_{th} < 2.7 −SET LET_{th} < 15	[11]
FI	12/17/2007	HS-117RH	Voltage regulator	Intersil	Bipolar	SET	TAM	+SET LET_{th} < 4 −SET LET_{th} < 8.3	[11]
FI	1/31/2008	LM2941	Voltage regulator	NSC	Bipolar	SET	BNL	250 mV > SET > 20 mV SET LET_{th} > 1.4	[7]
LS	1/15/2010	LM117HV	Voltage regulator	NSC	Bipolar	SET	BNL	SET > 200 mV @ LET = 60	[7]

IV. Test Results and Discussion

This section contains selected test results and discussions of tests performed on parts not presently published in other works.

A. *Analog Devices AD7760, 24-Bit, ADC*

The AD7760 is a high performance, 24-bit Σ-Δ analog-to-digital converter (ADC). It combines wide input bandwidth and high speed with the benefits of Σ-Δ conversion to achieve a performance of 100 dB signal-to-noise ratio (SNR) at 2.5 MSPS, making it ideal for high speed data acquisition. The reference voltage supplied to the AD7760 determines the analog input range. With a 4V reference, the analog input range is ±3.2 V differential biased around a common mode of 2V. The AD7760 ADC was tested for SEL at TAM. The LETs of the ions used ranged from 8 to 86 MeV-cm^2/mg. All the measurements were done in the normal incident configuration. The beam flux ranged from 10^4 to 10^5 ions/ (cm^{2}sec). Beam fluence of 10^7 ions/cm^2 was used to determine each cross-section point. Tests were done in the air with a normal incident beam. An evaluation board, EVAL-AD7760, the companion Blackfin ADSP-BF537, and evaluation software, all available from Analog Devices were used for the test. The three components provided a means of monitoring device functionality while the device was tested for SEL.

The AD7760 was tested at room temperature and at an elevated temperature of 85°C. The sample size was two. Latchup events were observed at both cases. The latchup events were observed at an LET as low as 8.3 MeV-cm^2/mg. The latchup threshold therefore is below LET of 8.3 MeV-cm^2/mg. Fig. 1 compares the results of the room temperature and elevated temperature measurements. These data indicate AD7760 is highly sensitive to latchup, and has an LET threshold below LET of 8.3 MeV-cm^2/mg. Furthermore, the cross section is relatively large, and gradually rising to approximately 5×10^{-4} at high LETs (saturation cross section).

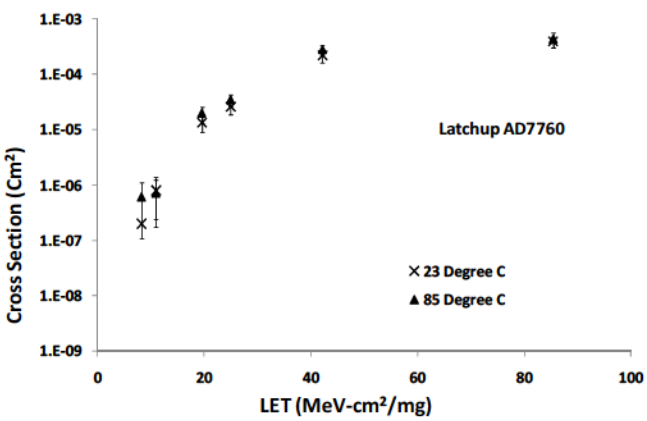

Fig. 1. AD7760 single-event latchup cross section at room and elevated temperature.

B. *Intersil HS-4423BRH Pulse Width Modulator*

The HS-4423BRH is a radiation-hardened inverting, dual, monolithic high-speed, metal-oxide-semiconductor field effect transistor (MOSFET) driver designed to convert TTL level signals into high current outputs at voltages up to 18 V. This device was tested at TAM. Devices were subjected to a total fluence of 10^7 ions/cm^2 with 15 MeV/amu Au (effective LET 84.6 MeV-cm^2/mg) at elevated temperature. The device under test (DUT) was configured to allow two or four (as in the application circuit) of the outputs to be tied together and sent to the scope. Devices were tested with static inputs of 0V and 5 V, as well as 5 V 1 kHz 50% duty cycle square wave. No SEL/SEB events were observed. No SET was observed for input conditions of 0 V and 5 V. SET were observed for the 5 V, 1 kHz stimulus. The average SET width was 23 µs and on the positive portion of the square wave (a negative going transient). No positive SET was observed on the zero potential portion of the square wave.

C. *On Semiconductor NL17SZ14 Inverter Schmitt Trigger*

The NL17SZ14 is a single inverter with Schmitt trigger that operates at low voltage. This device, among several others of the device family, was tested at BNL for latchup. Three devices were subjected to an effective LET of approximately 81 MeV-cm^2/mg while device inputs were toggled from 0 to 5 V at 1 kHz and the temperature was maintained at 85°C. Beam fluence was 10^7 ions/cm^2 with beam flux ranging from 2×10^4 to 4×10^4 ions/ (cm^{2}sec). No latchup events were detected during this test.

V. Summary

This paper presents recent data from SEE testing performed on a variety of semiconductor devices at the Jet Propulsion Laboratory. These data can be used in support of the selection of devices for use in space systems. It is the authors' recommendation that these data be used with caution as actual device performance can vary with application and from lot to lot.

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