Area Array Package Trends & Assembly Reliability/Failures for Tin-lead and Lead-free Solder

by

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JPL Space Missions

July 2009

Formulation (5)

Outer Planets (2016)

Exo-Planet (2015)

DESDynI (2017)

SIM (201X)

Soil Moisture (2012)

Pipeline

Implementation (6)

Juno (2011)

GRAIL (2011)

NuSTAR (2011)

MSL (2011)

WISE (2010)

Aquarius (2009)

Operations (19)

Dawn (2007)

Deep Impact (2005)

EPOXI

Stardust (1999)

Stardust Next

Cassini (1997)

MRO (2005)

Spirit (2003)

Opportunity (2003)

Odyssey (2001)

Kepler (2009)

Spitzer (2003)

Galex (2003)

Voyager 1 (1977)

Voyager 2 (1977)

OSTM (2008)

CloudSat (2006)

GRACE (2002)

Jason-1 (2001)

QuikScat (1999)

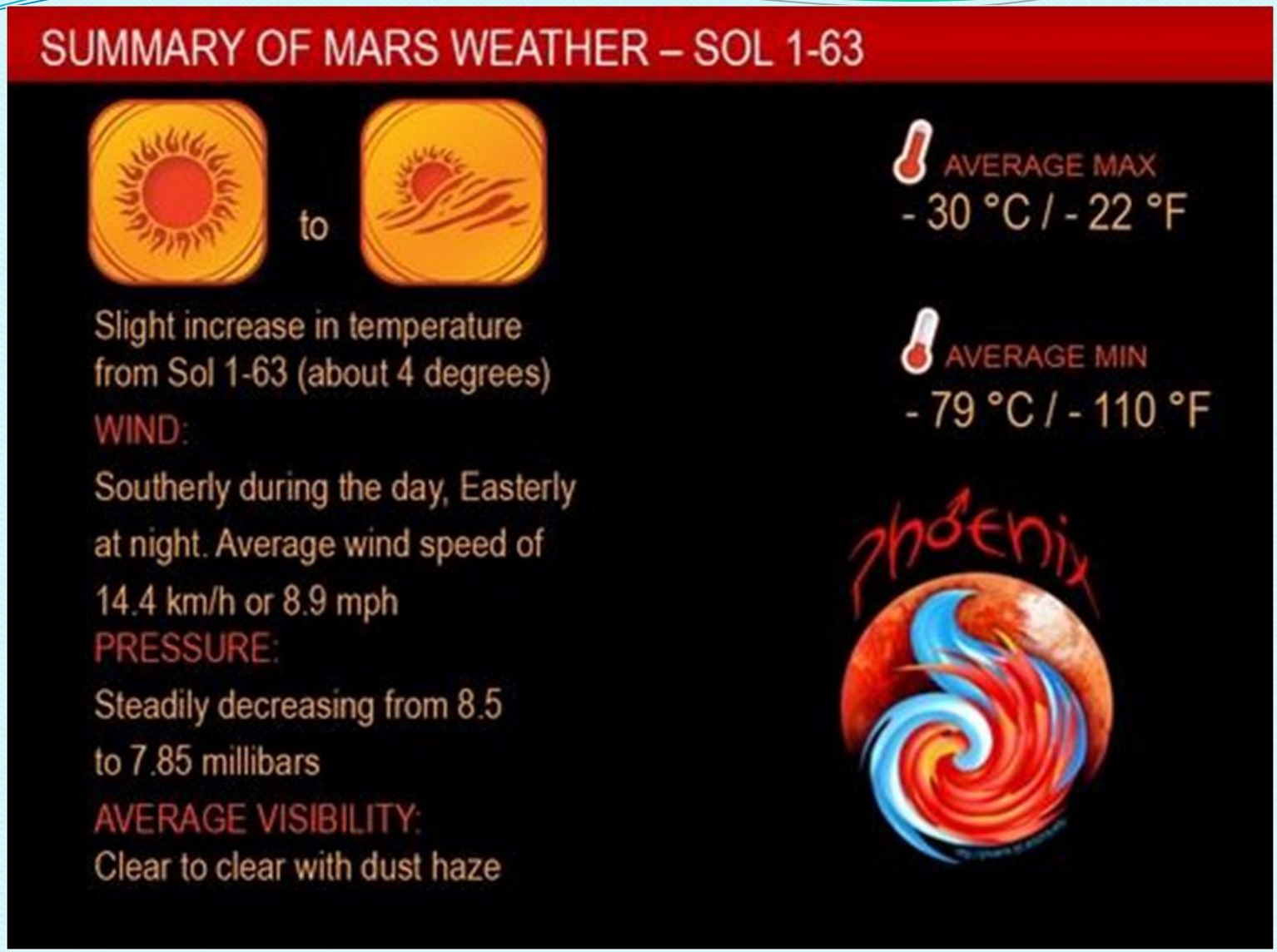
AcrimSat (1999)

Planetary/Mars Astrophysics Earth Science Planetary/Mars Astrophysics Earth Science Planetary/Mars Astrophysics

Mars Science Laboratory (MSL)- Curiosity Rover

- Determine whether Life ever arose on Mars
- Characterize the Climate of Mars
- Characterize the Geology of Mars
- Prepare for Human Exploration

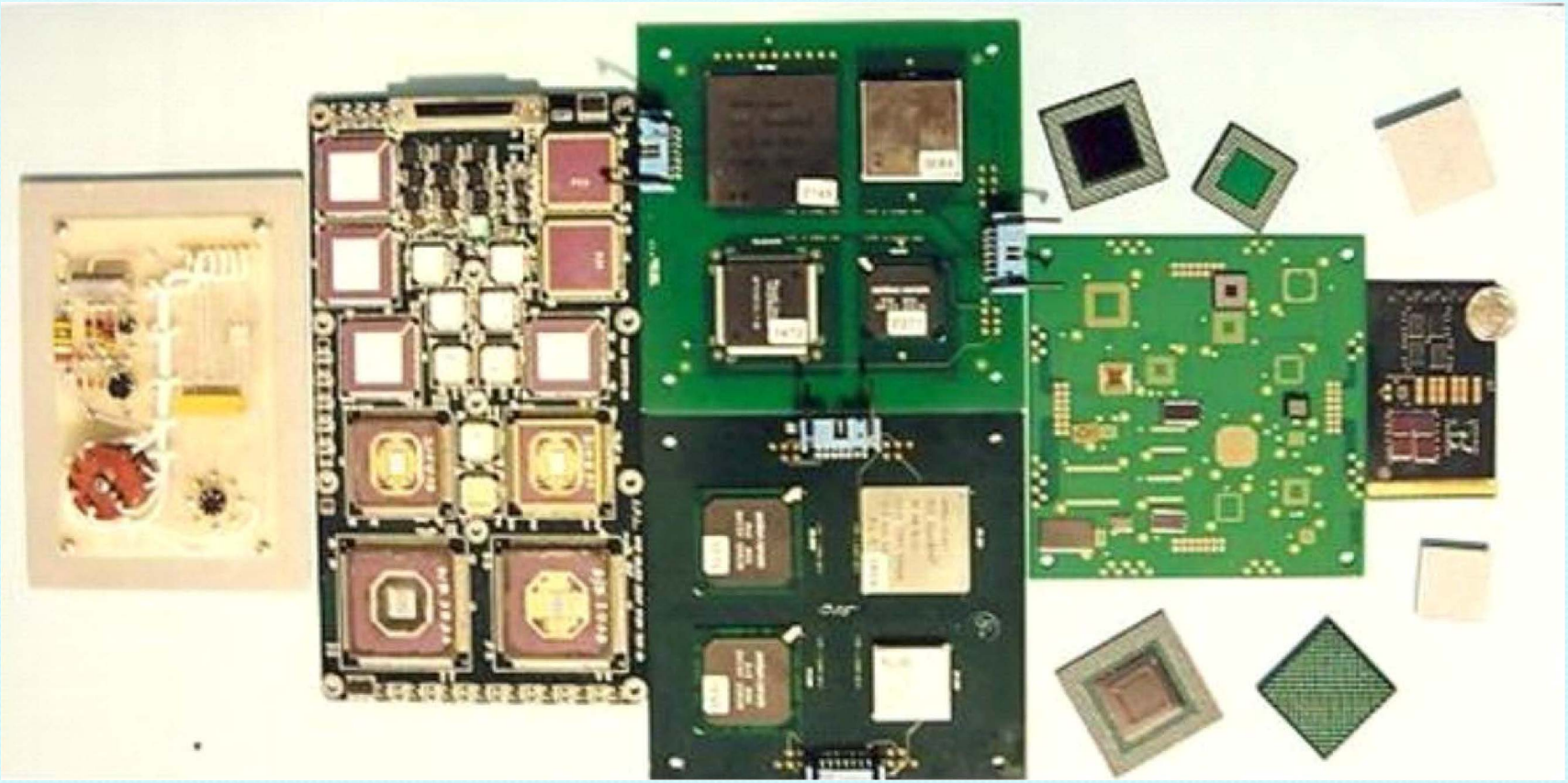
Mars is Cold- Tin Pest/Lead-free?



Outline

- Package Trends
  - Packaging trends thru historical test vehicles
  - Package concept and PBGA/CGA trends
  - Key parameter affecting assembly reliability PBGA/CGA
  - Reliability comparison /projections for CCGAs
  - Lead-free issues and reliability comparison
- High I/O BGA & CSP & SMC Packages
  - Assembly characterization/Key manufacturing defects
  - Reliability: Thermal cycle harsh/extreme cold
  - X-ray and optical and failure analysis after TCs/drops
- Summary & Future Activities

Package trends: Through Hole to Area Arrays



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High I/O BGA 1mm Pitch & 3D Stack Packages

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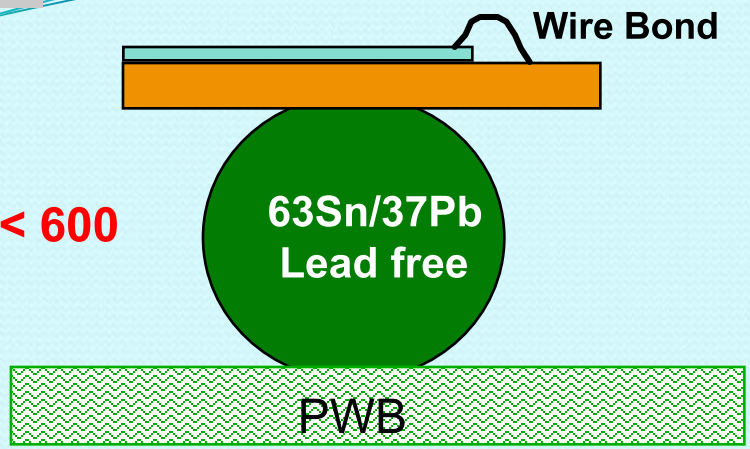
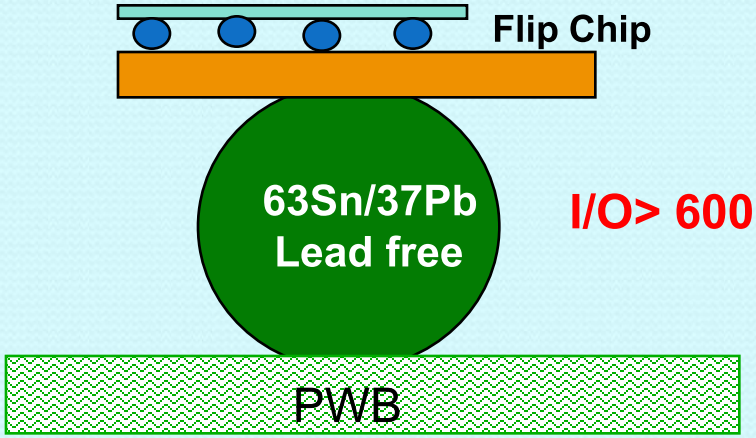
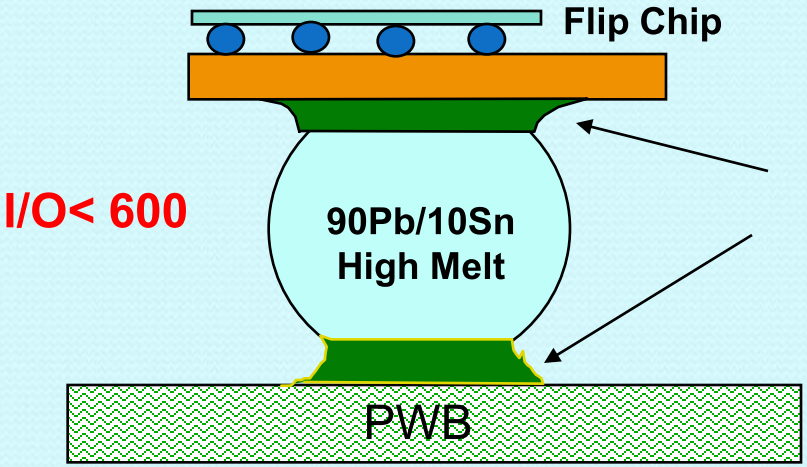
BGA Package Types



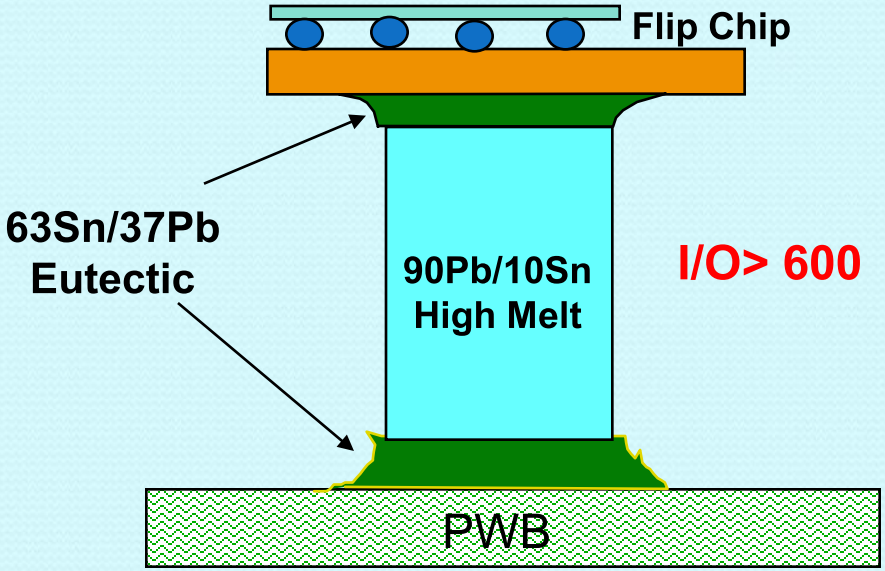
Plastic BGA (PBGA)



Flip Chip BGA (FCBGA)



Ceramic BGA (CBGA)



Column CGA (CCGA)

Area Array Package (BGA/CCGA) vs QFP

- Advantages
  - Capable of high pin counts
  - Manufacturing robustness
  - Higher package densities
  - Faster circuitry speed than QFP
  - Better heat dissipation

- Challenges
  - **Inspection**
  - Multiple processes and double sided assemblies
  - Routing for high pin count
  - Rework, especially individual balls

Package Trend- PBGA/CGA

- Plastic Ball Grid Arrays (PBGAs)
  - Peripheral to full array
  - From 1.27mm (50 mil) pitch to 1 mm (40 mil) pitch/lower
  - Wire-bond die (<1000 I/Os) to flip-chip die (>1000 I/Os)
  - Pb-Sn to **Pb-free**
- Ceramic Packages- Hi-Rel
  - CQFP to area array packages
  - CBGA to CCGA/CGA (>500 I/Os?) and LGA
  - Wire-bond to flip-chip die within package
  - Hermetic to non-hermetic package (>1000 I/Os?)
  - Pure column to column with Cu wrap (Six Sigma)
  - Pb-Sn to **Pb-free** (Cu column??)
  - Land grid with conductive interconnect rather **Pb-free** solder

Screen /Qualification New FPGAs

- Hermetic CGA packages
  - Wire bond/standard wire bond process/Pull test
  - Life time isothermal age/wire bond pull meet Spec
  - Three tier or more/fine pitch space/Vibration issue
  - Post column attach/inspection visual/x-ray/coplanarity/ pull test
- Non-hermetic CCGA/Flip chip die
  - Flip chip ball integrity is difficult: Ball shear & CSAM
  - Underfill materials: Outgas and adhesion integrity
  - Burn in test and subsequent tests: Column pull/Centrifuge
  - Post column attach/inspection/x-ray/coplanarity/bend/pull
- Passives in package

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Literature Data: Cycles-to-Failures for PBGAs

Case Number	Package (I/O, Pitch)	Pkg Size (die size) mm	Thermal Cycle Condition (ramp, dwell, Cycle/hr)	First Failure	Mean Life ($N_{63.2\%}$)	Comments
1	PBGA-119-1.27	27x27 ?(17.8x17.8 x0.3)	0°C/100°C (10 min, 5 min,2)	6260 (1% failure)	12215	27 Pkg Ref Mawer [12]
2	PBGA-256-1.27	27x27 (10x10)	0°C/100°C (10 min, 5 min,2)	No Failure to 9000 cycles	No failure to 9000 cycles	PWB 1.6 mm Thk Ref. Amkor [13]
3	FCBGA-1849-1.27	??	0°C/100°C	3095 (1% failure	4710	Ref Shiah[16]
4	PBGA-256-1.0	17x17 (8.80x7.9)	0°C/100°C (10 min, 5 min,2)	3687(1% failure)	NA	Full Array PWB, 2.3 mm Thk Ref Altera [14]
5	PBGA-676-1.0	27x27 (17.8x17.8x 0.3)	0°C/100°C (10 min, 5 min,2)	4686	6012	30/30 Fail, PWB, PWB 2.36 mm Thk Ref Xilinx[15]
6	PBGA-900-1.0	31x31.5 (17x17x0.3)	0°C/100°C (10 min, 5 min,2)	4405	5344	28/28 fail PWB 2.36 mmThk. Ref Xilinx [15]
7	FCBGA-1020-1.0	33x33 (22.6x19.9)	0°C/100°C (2 cycles/hr)	5670 (1% failure)	NA	PWB Thk 2.3mm 6 layer build up BT Ref. Altera [14]
8	FCBGA-1020-1.0	33x33 (17.9x16.7)	0°C/100°C (2 cycles/hr)	2770 (1% failure)	NA	PWB Thk 2.3mm 6 layer build up BT+ Cu heat sink Ref. Altera [14]
9	PBGA-313-1.27	35x35 (13x13)	-30°C to 100°C (25 min, 15 min, .75)	3310 (1% failure)	4000	13 Pkg, PWB 1.6 mm Thk Ref Evans/Ghaffarian [17]
10	PBGA-256-1.27	27x27 (10x10)	-40°C-125°C (15 min, 15min, 1)	~2000 (1% failure)	(3164)	PWB 1.6 mm Thk Ref Amkor
11	PBGA-676-1.0	27x27 (17.8x17.8x 0.3)	-40°C-125°C (15 min, 15min,	1341	1830	27/32 Fail, PWB 1.6 mm Thk

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Key Parameters for PBGA Assembly Reliability

- **Thermal Cycle range, ramp rate, dwell times**
  - PBGA 256, 0-100°C, CF 1%F is 3200 cycles
  - PBGA 256, -40-125°C, CF 1%F is 2000 cycles
- **Package size, thickness, configuration, and I/Os**
  - PBGA 256, 0-100°C, CF 1%F is 3200 cycles
  - PBGA 1849, 0-100°C CF1%F is 3095 cycles
- **Die size and its relation to the package size and ball configuration**
  - Was not apparent for data given in table, show opposite effect possibly due to heat sink
- **PWB thickness, definition of pad, surface finish**
  - IPC 9701 defined 2.3 mm, a 676 I/O showed higher thermal resistance than 256 I/O, possibly using thinner board
- **Single or double sides, relative effect of package on top and bottom**
  - Double sided, mirror image had lower resistance to thermal cycle

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Literature Data: Cycles-to-Failures for CCGAs

#	Package I/O- Pitch	Pkg Size (die size, mm)	Thermal Cycle Condition (ramp, dwell, cycle/hr)	First Failure	Mean Life (63.2%)	Comments
1	CCGA 472-1.27 Cu spiral column	Not specified	-55°C to 105°C (30 min dwell, 5°C /min)	500 cycles (crack/no failure)		Package size not given Failure definition not IPC 9701 standard Ref [10]
2	CCGA 624-1.27 Cu spiral column 90/10 Pb/Sn	32.5x32.5x2.25	-55°C to 105°C (30 min dwell, 5°C /min)	~ 2300 ~1200	NA	Spiral column showed significantly better TC resistance Ref [11]
3	CCGA 1152 & 1272- 1 mm Cu spiral column 90/10 Pb/Sn	35x35x2.77 & 37.5x37.5x2.77	-55°C to 105°C (30 min dwell, 5°C /min)	~ 1200 & 1500 ~ 850 & 1100		Spiral showed improved resistance Ref [11]
4	CBGA937-1.0	32x32x1.5 (substrate) 32x32x2.4	0°C to 100°C (2 cycles/hr)	NA	1860 ($N_{50\%}$) 1310 ($N_{50\%}$)	Ref [12]
5	CCGA 1144-1.0 90/10 Pb/Sn column	35x35x1.59	0°C to 100°C (2 cycles/hr)	No Failure to 5000 cycles	NA	Ref [13]
6	CCGA1657-1.0 90/10 Pb/Sn	42x42x1.5 42x42x2.55 42x42x3.7	0°C to 100°C (2 cycles/hr)	NA	1530 ($N_{50\%}$) 990 620	Ref [14]
7	CCGA 1657-1.0 Cu column	42.5x42.5x 2.55	0°C to 100°C (2 cycles/hr)	1660 (1st failure)	2410 ($N_{50\%}$)	Cu column, solder paste 96.5 Sn3.5Ag Ref [15]

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Key Parameters for CCGA 2nd Level Reliability

- **Thermal Cycle range, ramp rate, dwell time**
  - CBGA 361, 0/100°C, CF 50%F is 4535 cycles
  - CBGA 361, -55/110°C, CF 50%F is 1190 cycles
- **Package size, thickness, configuration, and I/Os**
  - CBGA 361- 0.8 mm thick 0/100°C, CF 50%F is 4535 cycles
  - CBGA 361-1.2 mm thick 0/100°C, CF 50%F is 2700 cycles
  - CBGA 361-2.9 mm thick 0/100°C, CF 50%F is 1600 cycles

  - CBGA 361-.8 mm thick, 0/100°C, CF 50%F is 4535 cycles
  - CBGA 625-.8 mm thick, 0/100°C, CF 50%F is 2462 cycles

  - CBGA 361, -55/110°C, CF 50%F is 1,190 cycles
  - CBGA 361, -55/110°C, CF 50%F is 2,160 cycles- HITCE Substrate

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Key Parameters for CCGA 2nd Level Reliability

- **Die Size and its relation to the package size and ball configuration**
  - Die size/Package type (full vs peripheral) on TC reliability
    - Less important for ceramic
- **PWB thickness, definition of pad, surface finish**
  - IPC 9701 defines 2.3 mm, thinner board improve reliability
  - Effect of board thickness
    - Not established for ceramic package
  - Effect is less critical for CCGA
- **Single- or double- sides, relative effect of package on top and bottom**
  - PBGA: Double-sided, mirror image had lower reliability
  - Ceramic: No data

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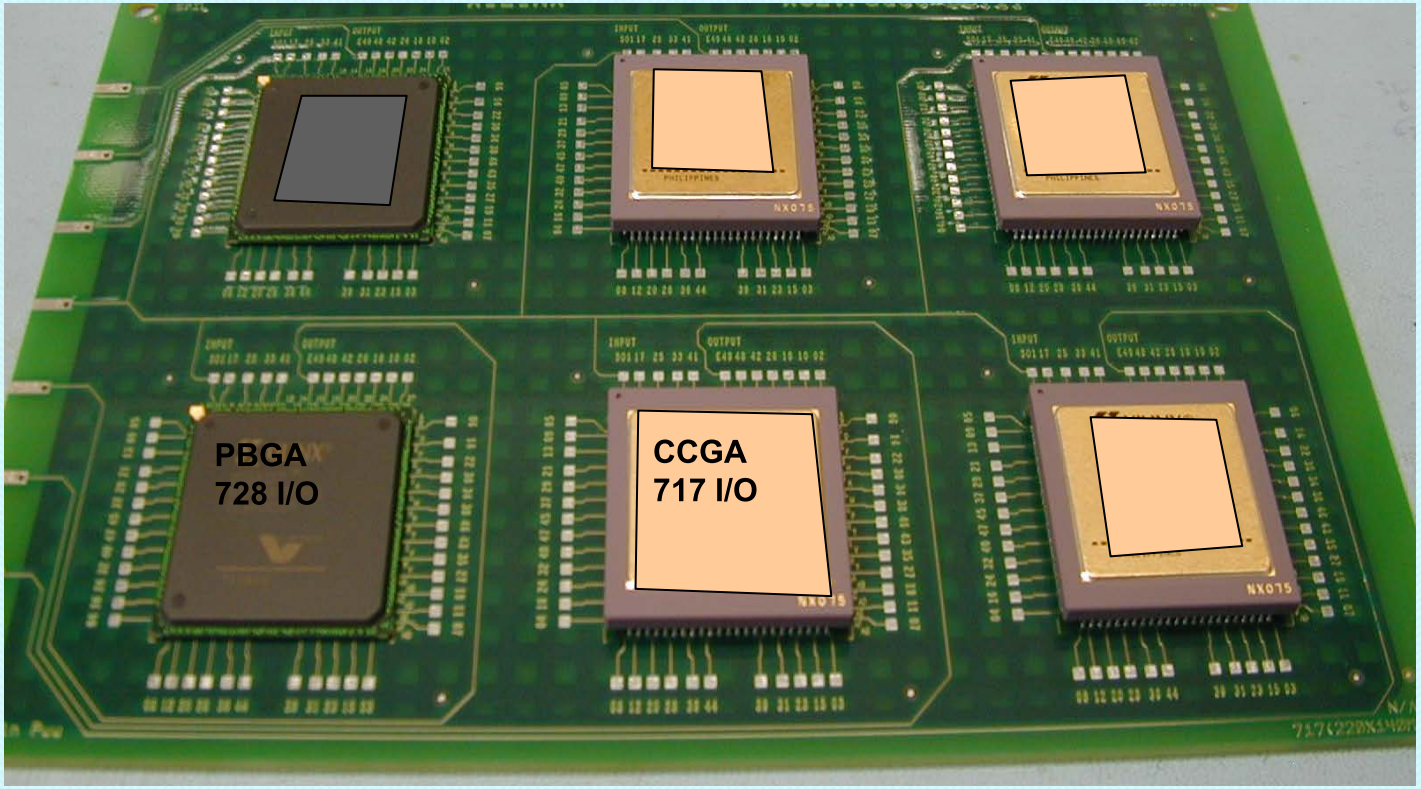
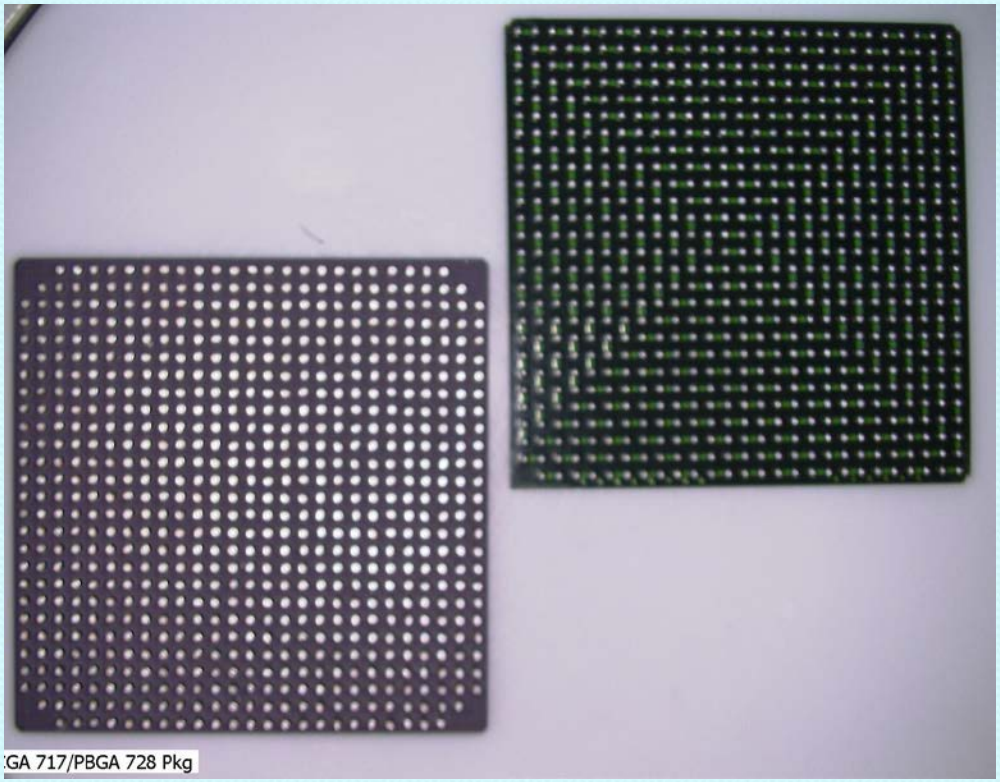
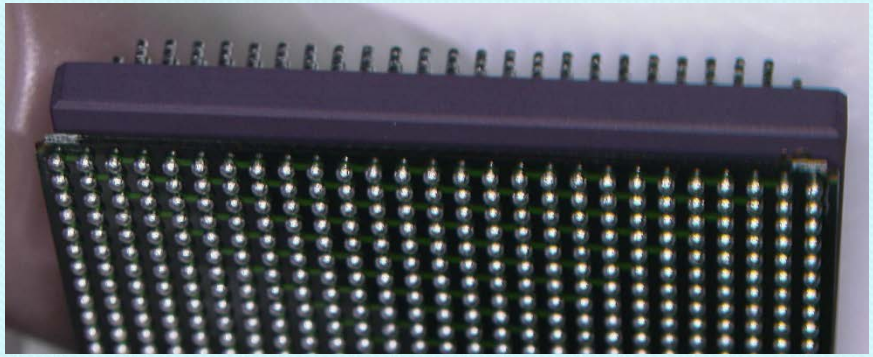
CCGA 717 & PBGA 728 I/Os TV

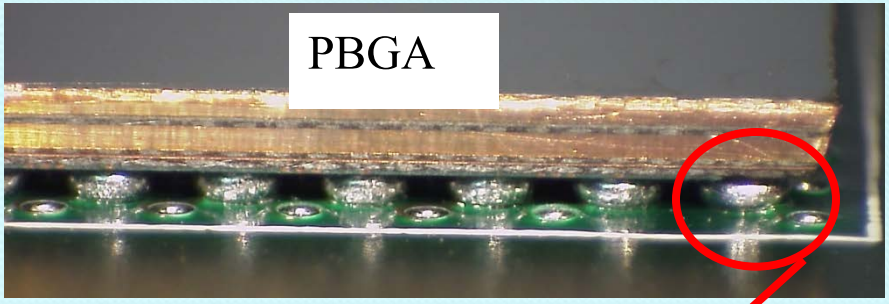


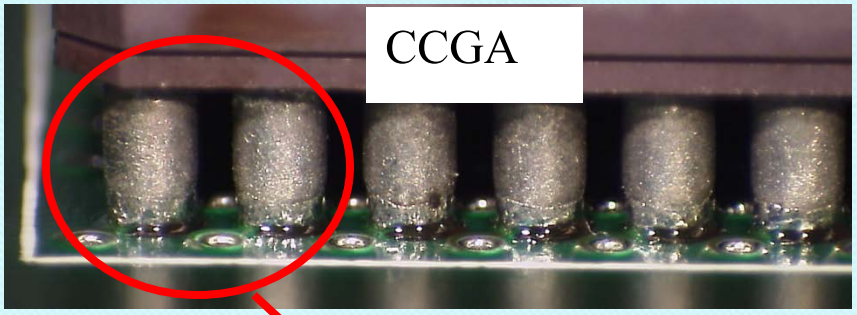
CCGA 717 & PBGA 728 I/Os

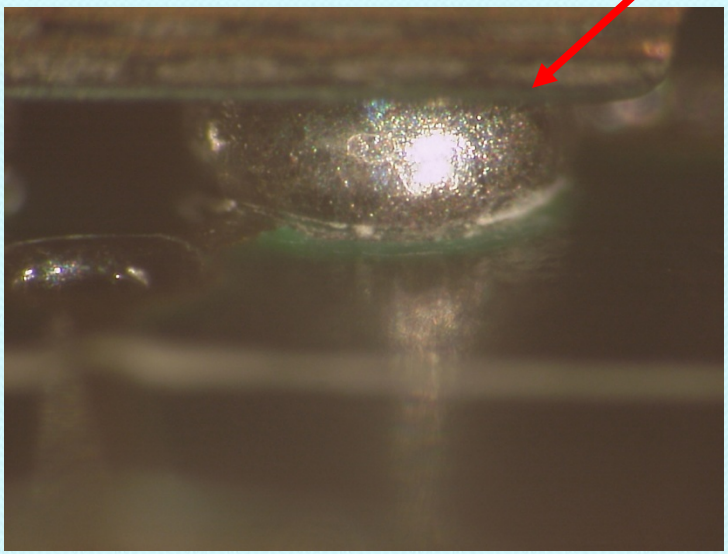


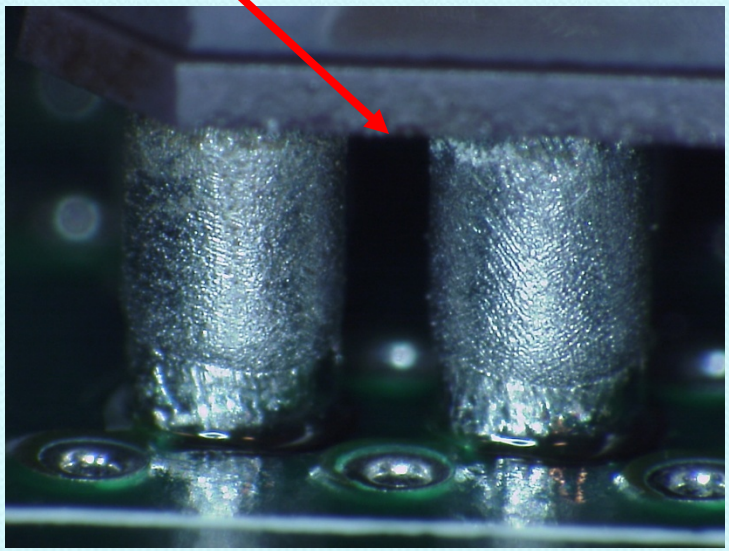


CCGA & PBGA Package Interconnections



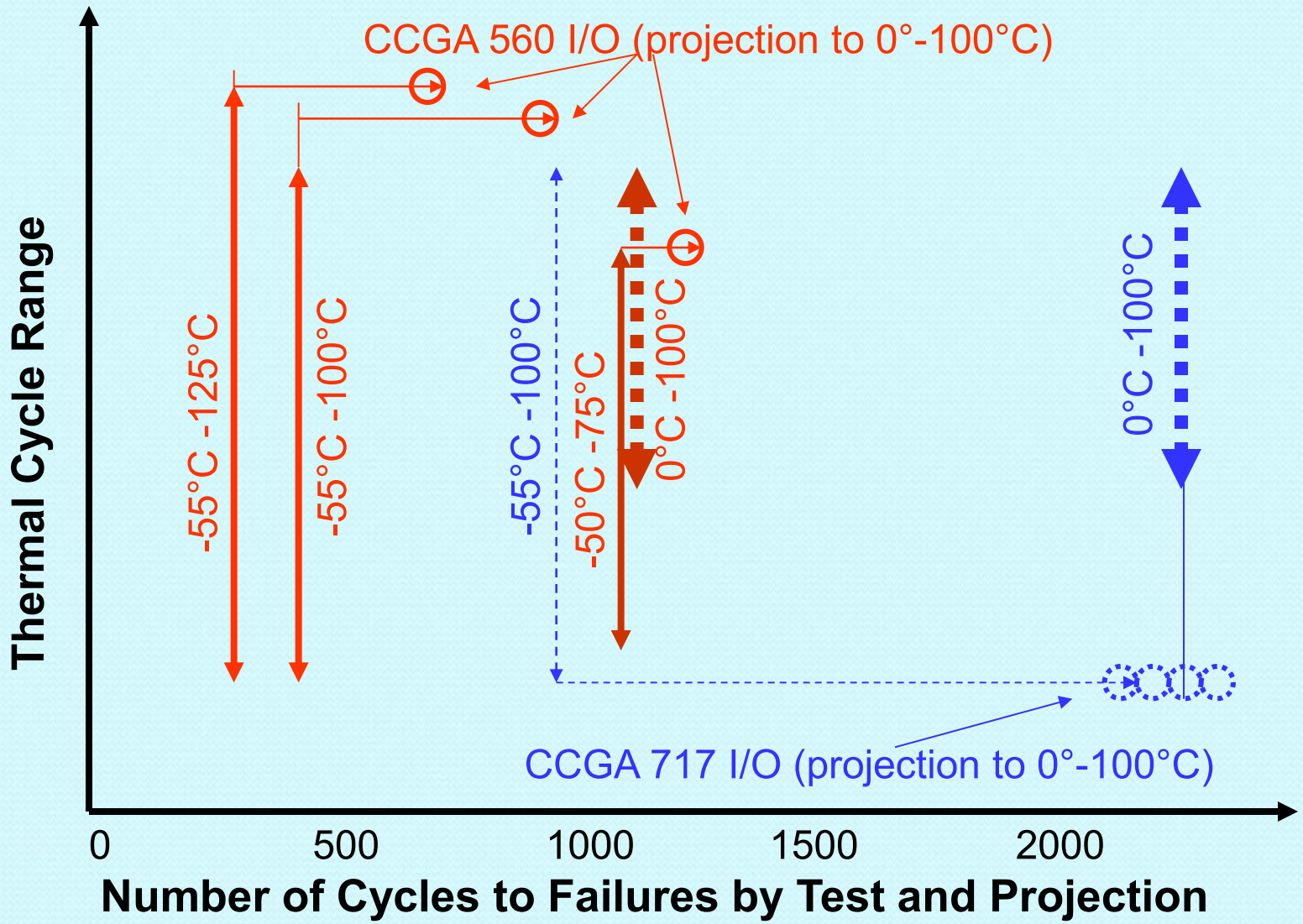






950 Thermal Cycles (-55°/100°C)

Projection using Coffin-Manson Relationship



Effect of TC Range/Dwell Time

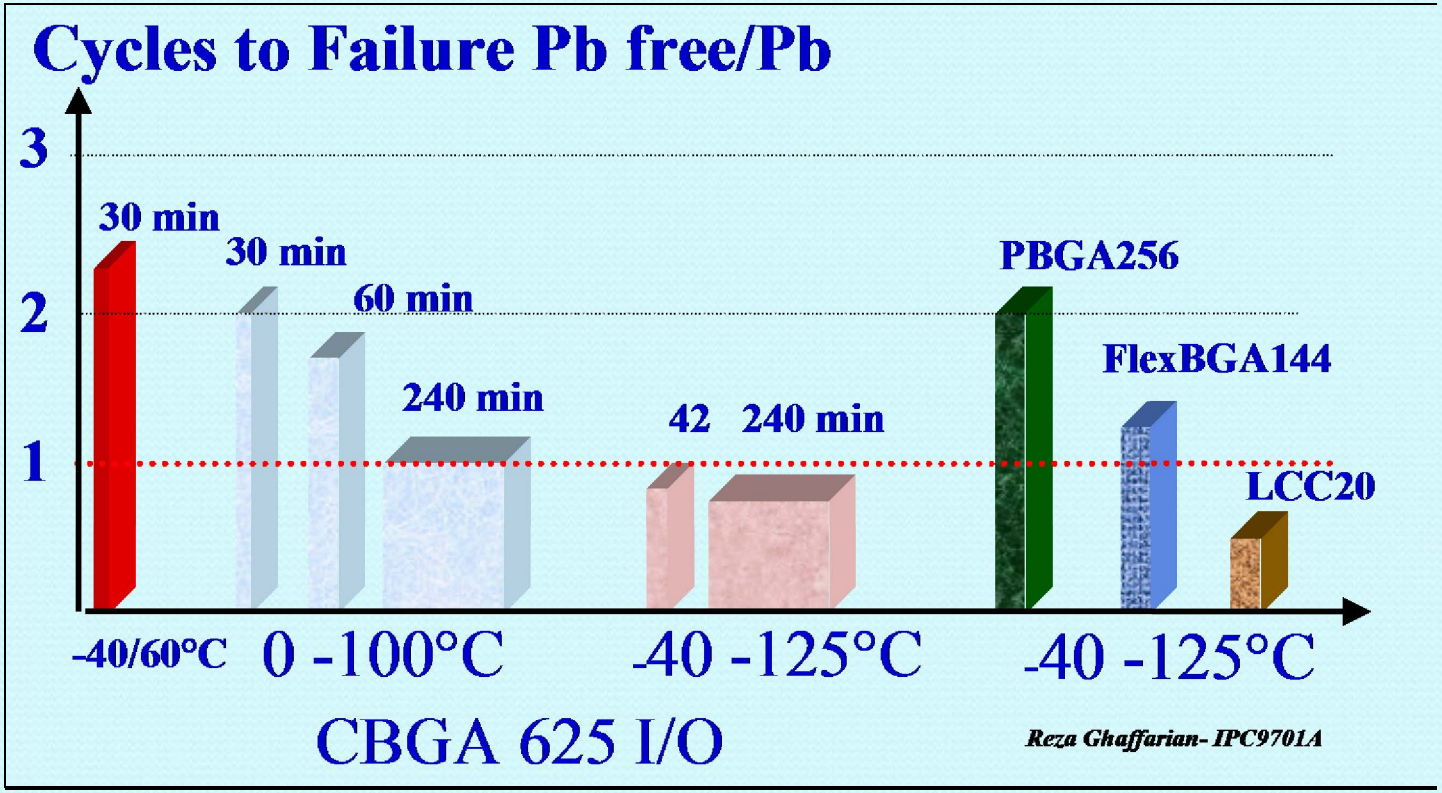
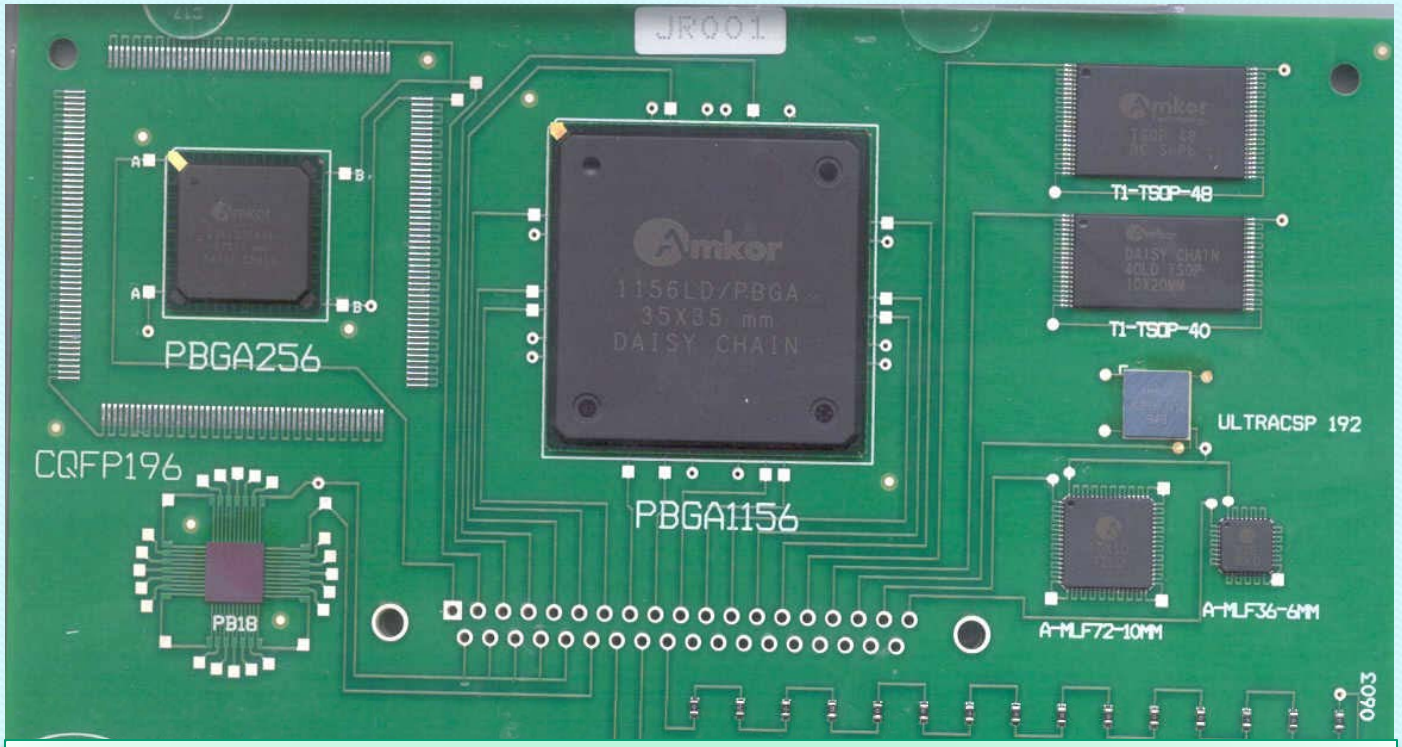


Figure B1 Cycles-to-failures for SAC (Sn-Ag-Cu) solder attachment depend on thermal cycle range and state of stress/strain (Courtesy Reza Ghaffarian, NASA-JPL, CIT), different source of data including [11].

Note: When comparing cycles-to-failure data for lead-free and lead-based solders, it should be noted that such comparison may not be valid since failures depend not only on the temperature cycle profile but also on the type of package and assembly configuration.

High I/O BGA & CSP/Flipchip/TSOP Packages



Detail Discussion on a Recent Test Vehicle

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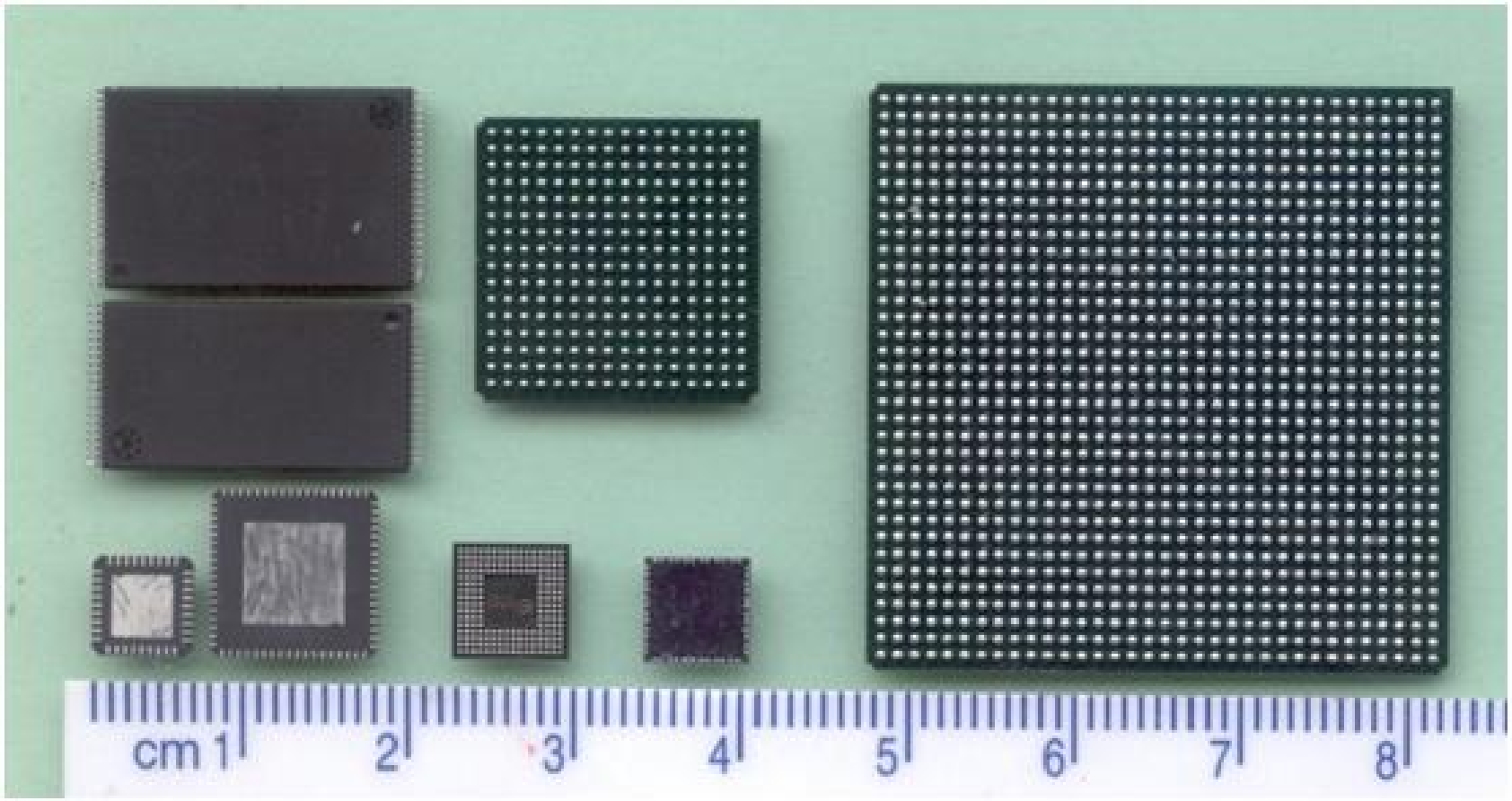
PBGA 1156 I/O 1mm /CSP/FC/MLF



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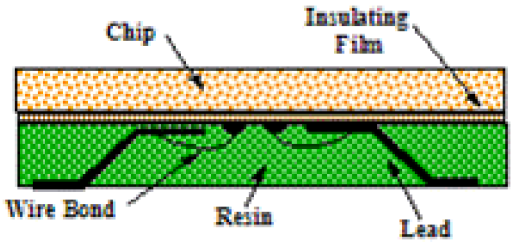
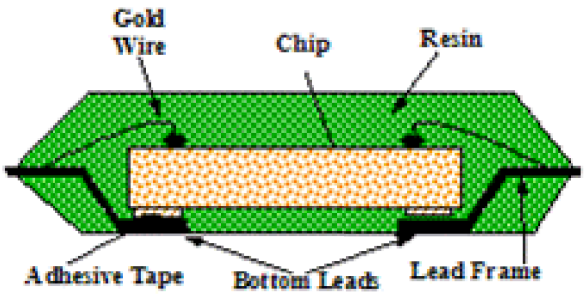
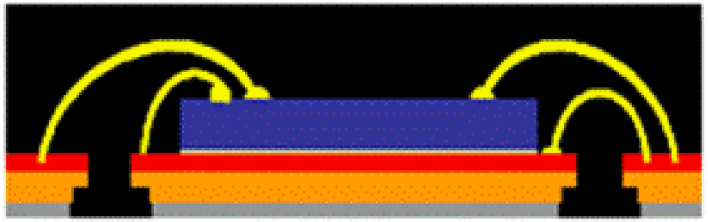
Leadless Package & MLF 36/72 I/Os



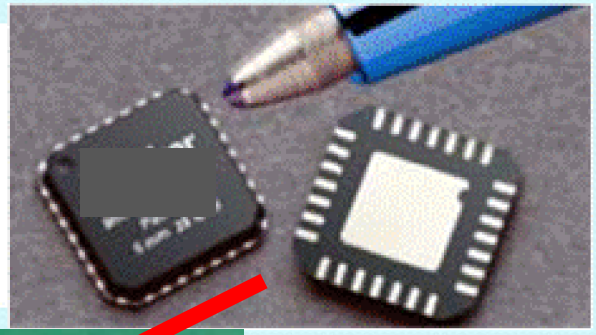
Lead On Chip
LOC

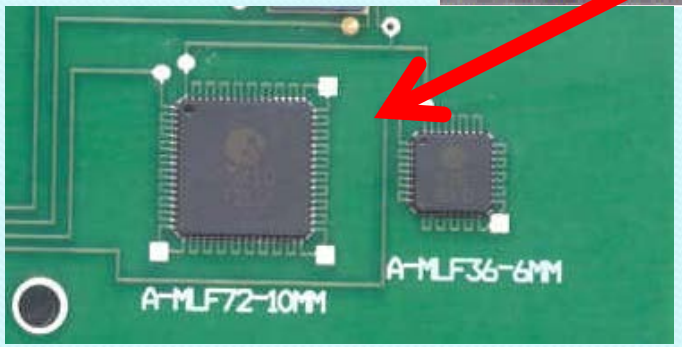


Ultra-Thin-Small-Outline
USON



MicroLead Frame®





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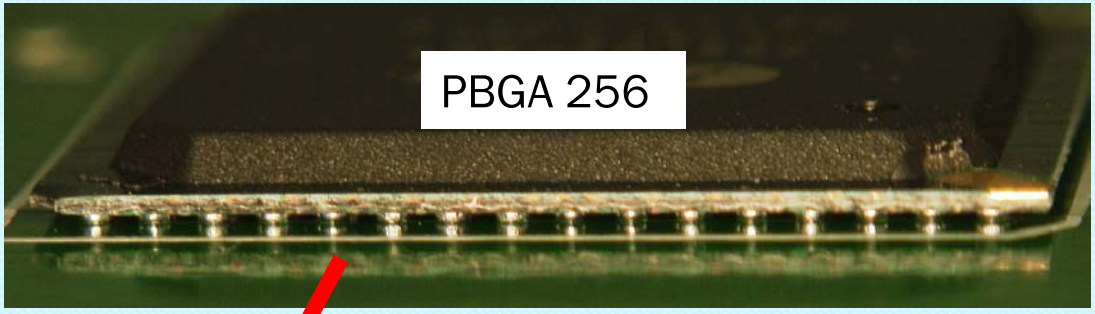
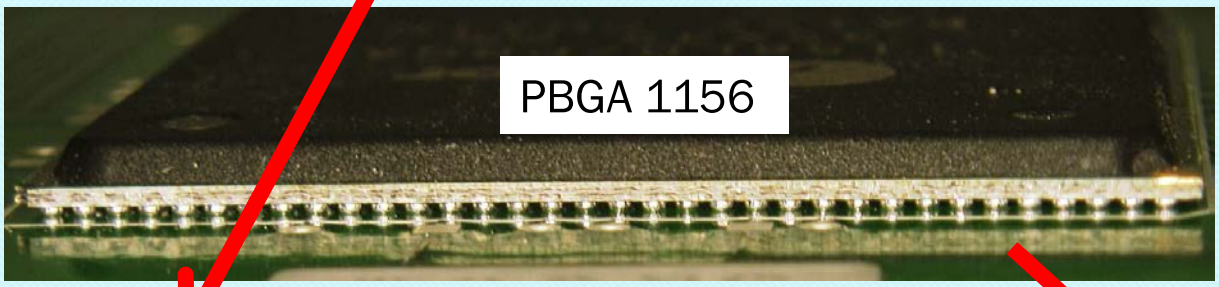
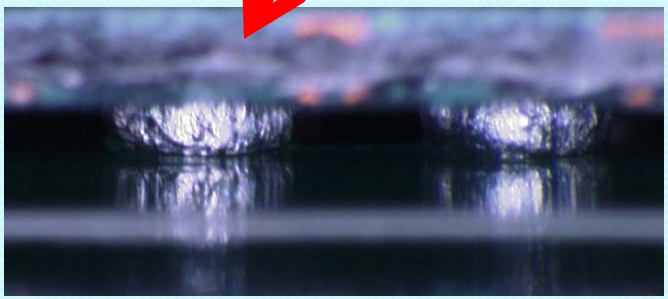
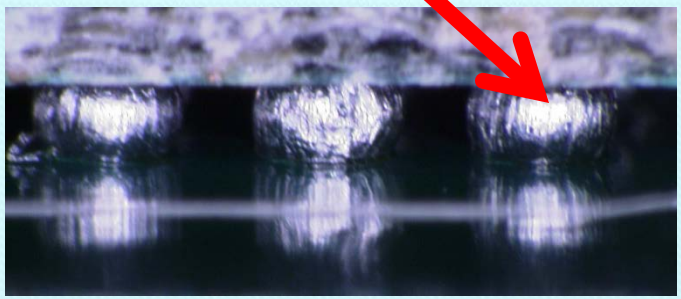
Optical Photos of PBGA 1156 & 254 I/O Assemblies









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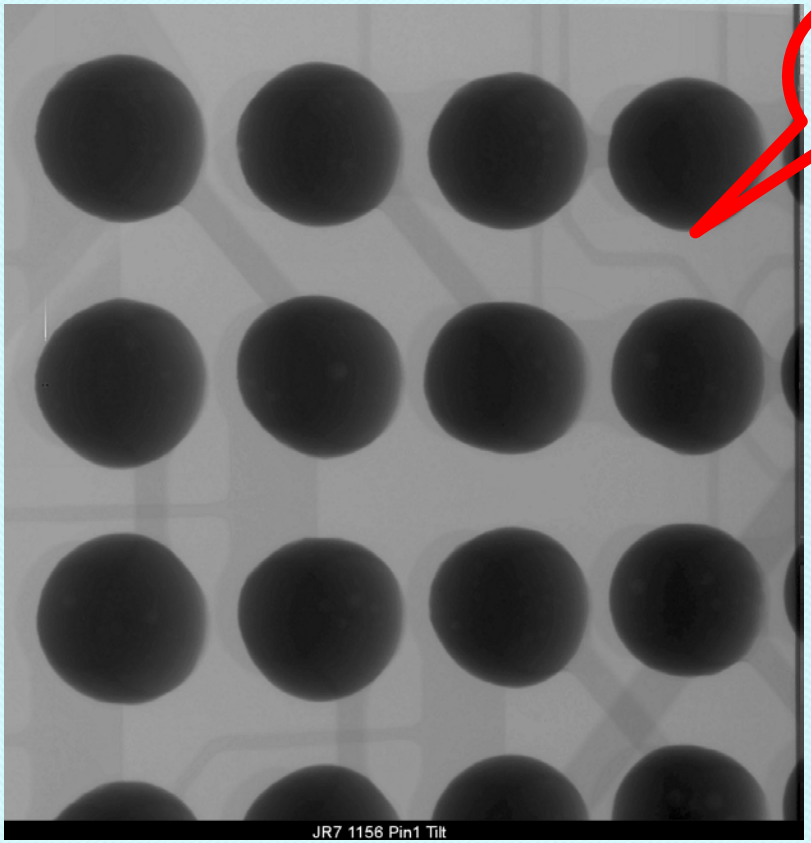
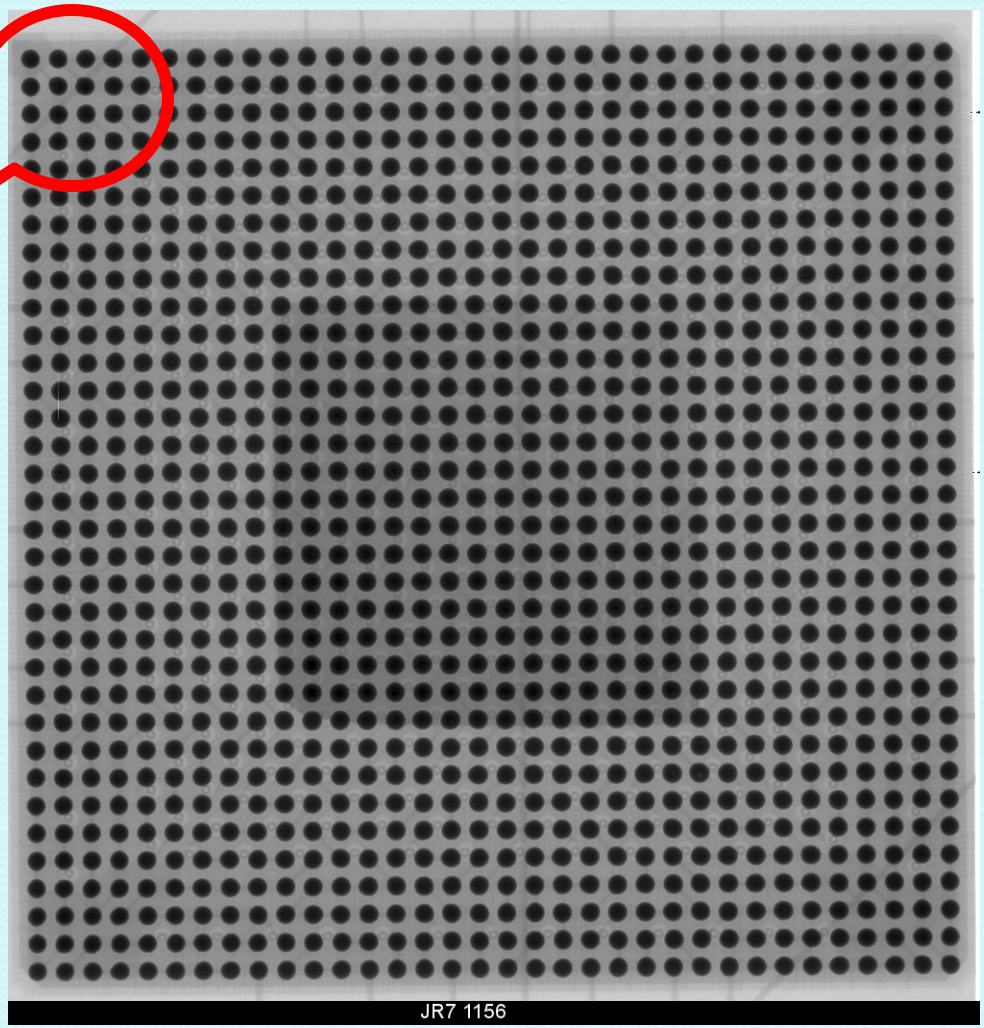
X-ray of PBGA 1154 I/O 1mm Pitch Assembly





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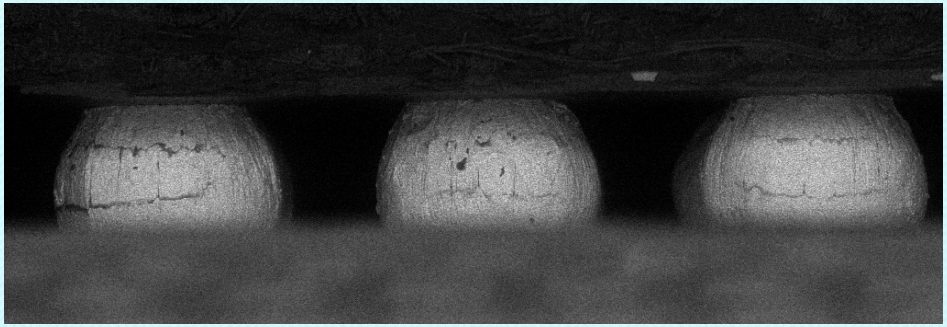
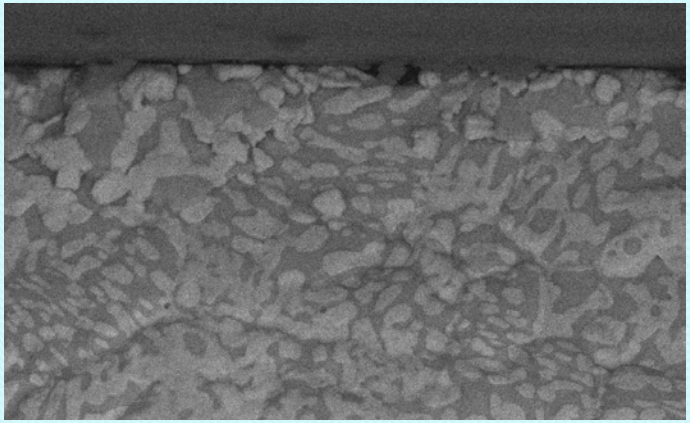
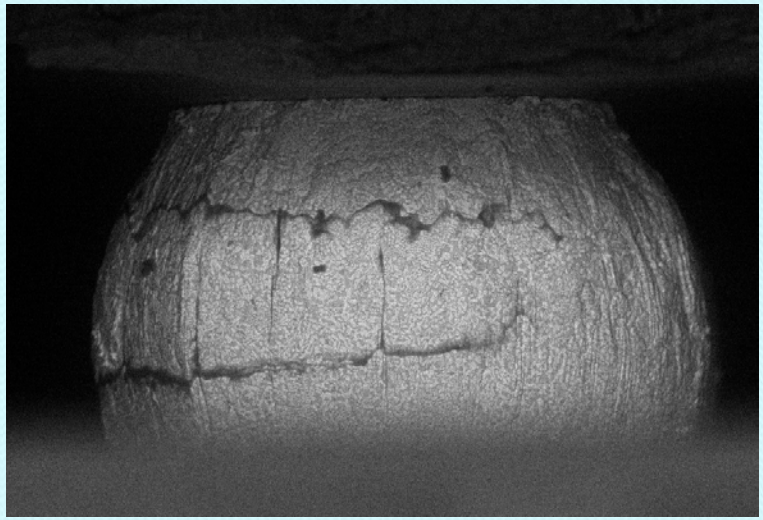
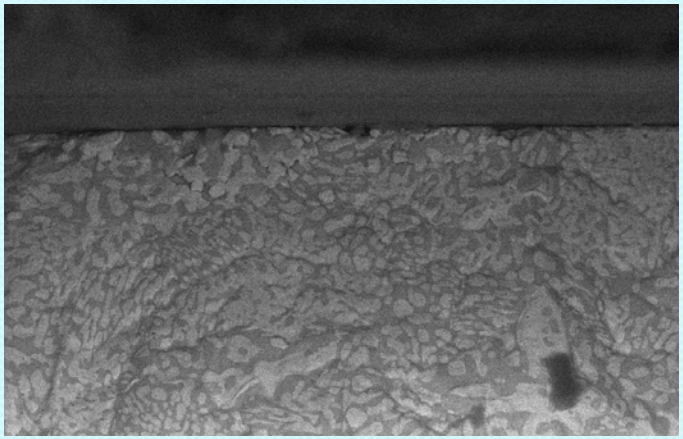
SEM Images of Thermally Cycled PBGA 1156 I/O Assemblies









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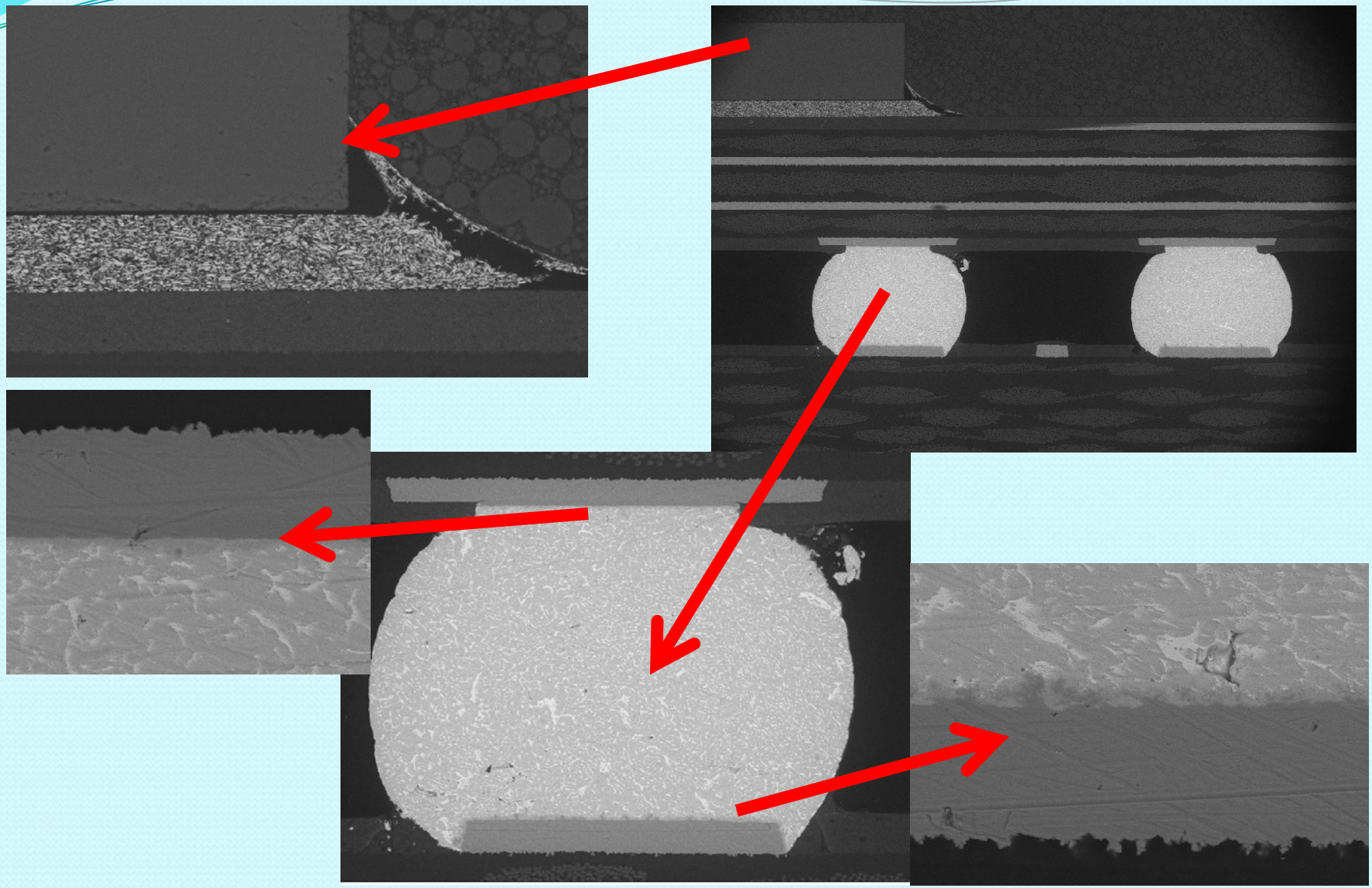
X-section Images of Thermally Cycled PBGA 1156 I/O Assemblies



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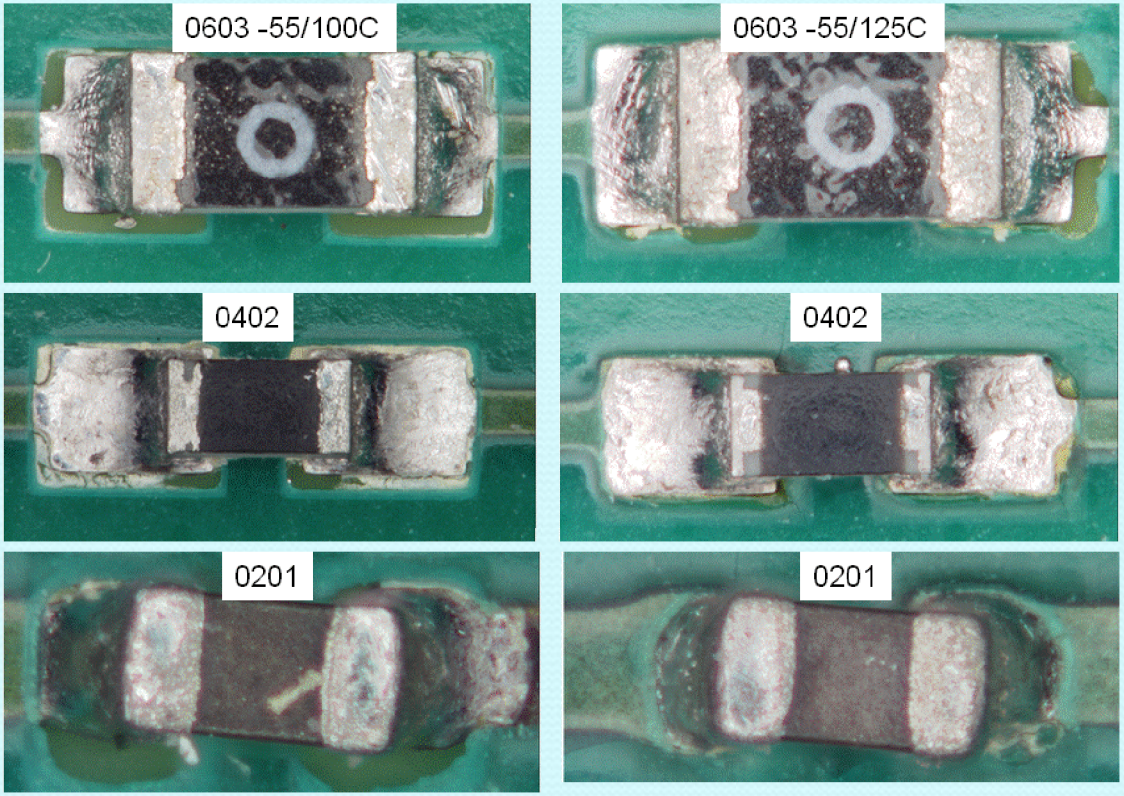
Damage of 0201 and 0402 Resistors under two TCs, -55/100C & -55/125C with the same time intervals



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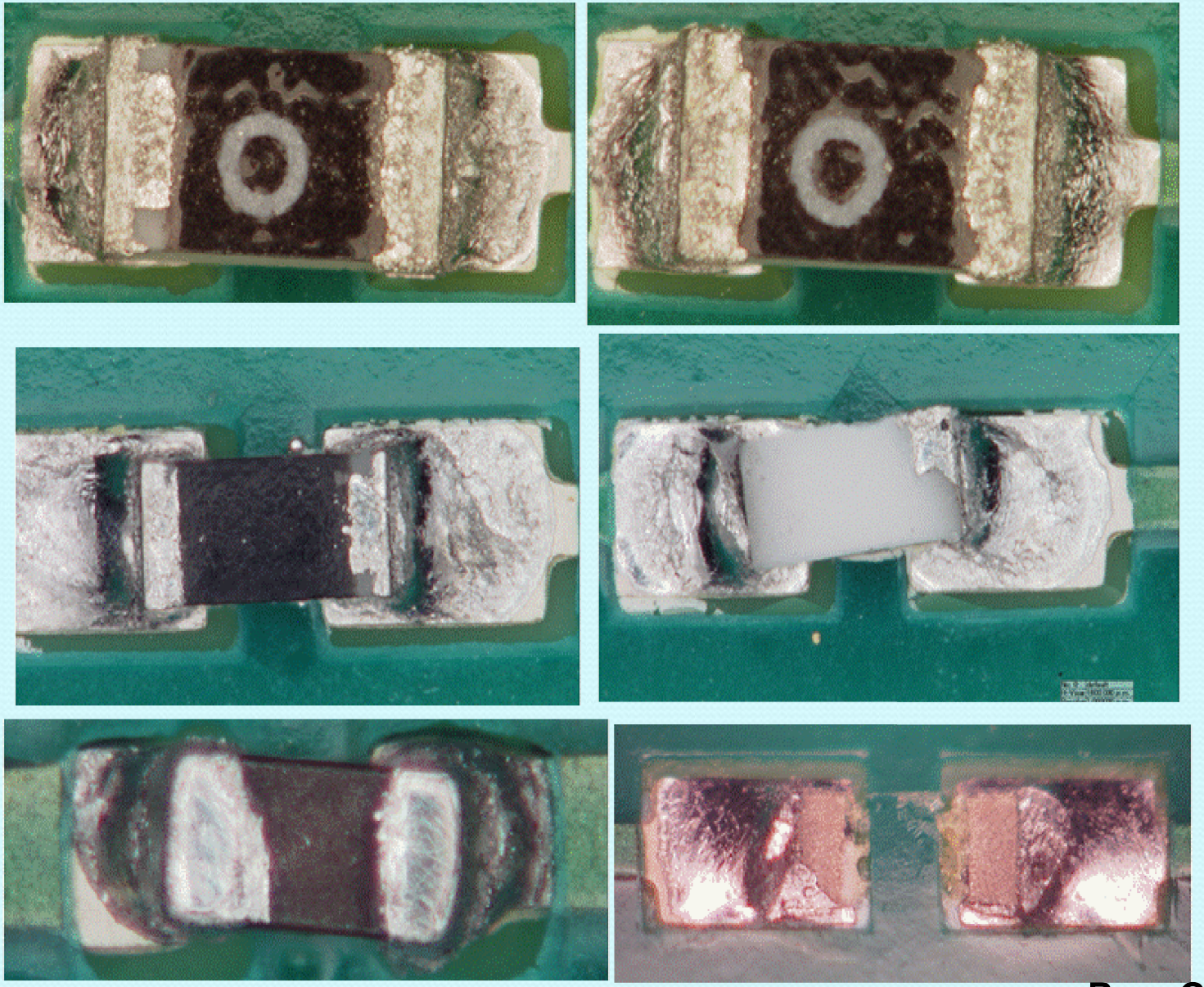
Damage of 0201 and 0402 Resistors under Extreme Thermal Cycle -120/85C



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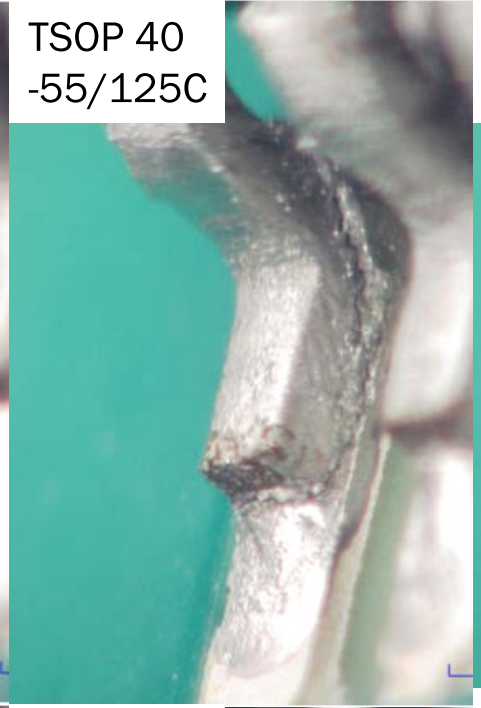

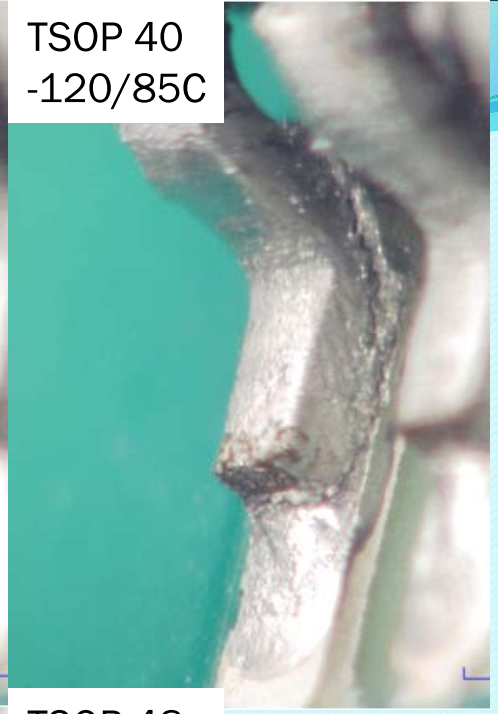

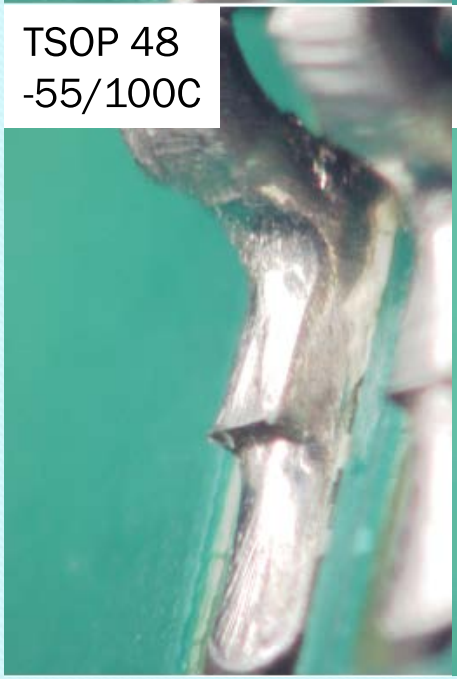

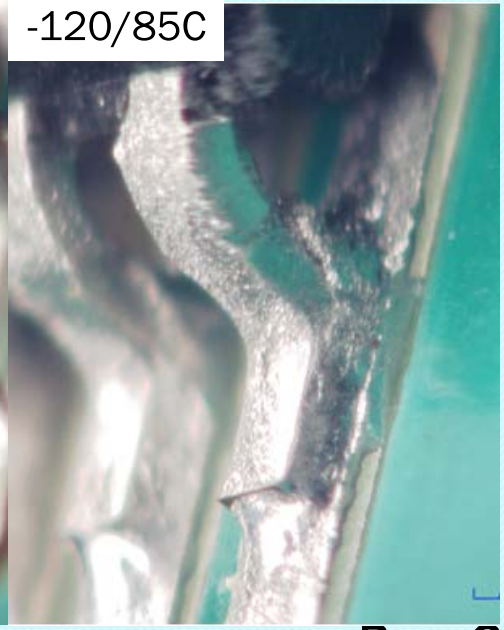

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Lead-free & High Reliability

- Why?
  - "Green" Marketability/Reputation Advantage
  - WEE & REACH! Other Legislation (Waste from Electrical & Electronic Equipment)
  - Implemented – Commercial worldwide /**High Reliability lags**
- Lead-free SAC
  - SAC near eutectic , INEMI/IDEALS/JEIDA
  - Requires reflow temp 235°C (melt 217°C)> Tin-lead 210°C (183°C)
  - Issues with exiting package/assembly – mostly resolved
  - Now, alloy proliferation! – **High Reliability?**
- Package Finish (Tin Whisker)
  - Matte tin (low organic content, grain>1 μm) – **High Reliability?**
- Assembly Reliability
  - Extensive data for commercial/Minimum data & scatter for **High Reliability**
  - Inspection criteria redefinition – Minor for **High Reliability**
  - Mixed Pb-free & Pb – Critical for **High Reliability**
  - Assembly/Rework – Critical for **High Reliability**

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Lead-free Activities& High Reliability

- **Limited study for High Reliability**
  - NASA NEPP initiated some activity
  - NASA-JPL joint study with RIT on backward/lead-free TC/Drop
  - NASA strong policy for mitigation of Tin Whisker
- **NASA- DOD on Lead-free**
  - Completed comprehensive study, thermal cycle/vibration/shock
  - Continuation on rework- Data being gathered/e.g., presentation at AIMS/SMTA 09
- **Aerospace GEIA Guidelines**
- **Implementation for high-end commercial**
  - Extensive presentations @ SMTA/AIMS/ECTC 2007/2008
  - IBM lesson learned SMTA Oct 2009
- Issues for Hash Environment
  - Reliability, especially mechanical, quality controls/specifications
  - Lead-free alloy proliferation- Chaos!

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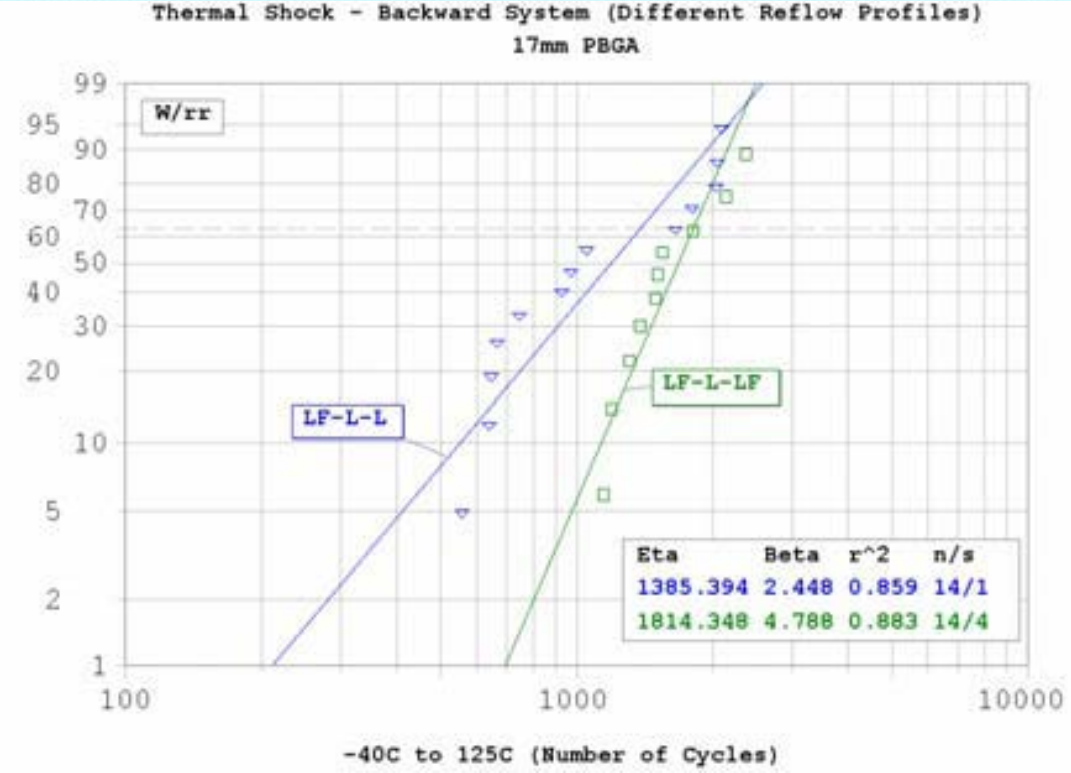
Lead-free Interim Solution for High Reliability

- **Use lead-free balls and tin-lead paste**
  - NASA-JPL & also joint study with RIT on backward/lead-free TC/Drop
  - NASA-DoD on lead free, industry, universities
  - CAVE Auburn University: PBGA 17mm, 208 I/O 1mm pitch



Tao Zhang, John Evans, Charles Mitchell, Zhao Zhi Li, Erika Crandall, Joshua Ridenour and Fei Xie

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Lead-free Interim Solution for High Reliability

- **Reball lead-free balls with tin-lead paste**
  - NASA-JPL investigated recolumn
  - Industry investigation
  - CALCE, University of Maryland

Assembly Type	Sample Size (failure/total)	Slope (β)	Characteristic Life (η)	Cycles to 10% Failure (B_{10})
676 I/O Reballed LTWS+PF	20/20	7.10	2336	1702
676 I/O Reballed SW+PF	24/24	7.98	2123	1601
676 I/O Lead-free (230°C)	23/24	7.33	4273	3143
676 I/O Lead-free (240°C)	23/24	5.72	4276	2885
676 I/O Mixed	20/24	3.92	4498	2533
256 I/O Reballed LTWS+PF	23/23	9.14	2419	1891
256 I/O Reballed LTWS+BD	23/23	8.33	2561	1955
256 I/O Lead-free	21/24	5.20	4624	3000
256 I/O Mixed	11/24	4.18	5929	3461

Table 3. Cycles to failure data of 676 I/O and 256 I/O BGA Assemblies

Lei Nie, Michael Osterman, and Michael Pecht , Center for Advanced Life Cycle Engineering (CALCE)
SMTA 09

Drop tests for as-assembled and after 2 TCs

Thermal cycles

-55/100°C

-55/125°C

Various cycles

Drop test parameters

Parameter	Setting
Average peak load	485 G
Time period	3 ms
Height of drop	36 inches
Maximum drop cycles	30
Stand-off height	2 inches

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Number of Drops to Failure for Different Solder ball/Paste Conditions

Package Type	As Fab Pb/Pb	As Fab SAC ball /Pb Paste	As Fab SAC/SAC
PBGA 1156	2	1	1
PBGA 256	14	16	5
Thickness	0.093	0.063	0.093

TSOPs: No Failure to 30 drops

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Summary: Tin-Lead Solder: High I/O BGA & CSP/SMC

- **Assemble BGA/CSP/FC/MLF/TSOP/0201-0603**
  - Vapor phase reflow process
  - High I/O BGA 1156 I/O 1mm pitch – No issue
  - CSP- Issue with paste print consistency
  - MLF- Design need to be changed for consistent paste print
  - Often opens for 0201 due to tombstone defects
- **Inspection after cycling**
  - Optical inspection difficult for area array, flip chip , and MLF
  - X-ray, generally difficult to narrow damage level
  - X-ray revealed larger size for TSOP 40 rather TSOP 46

Summary: Tin-Lead Solder: High I/O BGA & CSP/SMC

- **Thermal cycles (-55/100C), (-55/125C), (-120/85C)**
  - Compared damage on TSOP under three conditions
  - Compared for 0201 chip resistor
  - Optical/SEM /X-section of BGA 1156 I/O
- **Drop test @ ~ 500 g**
  - Critical: Package location, type, and size
  - PBGA 1156 at the center failed after one drops for As Fab
  - PBGA 256 away from center, better results for comparison
- **Current/Future Activities**
  - More comprehensive study on TC/Drop with RIT University gathered/presented
  - New test vehicles with >1500 I/Os and fine pitch

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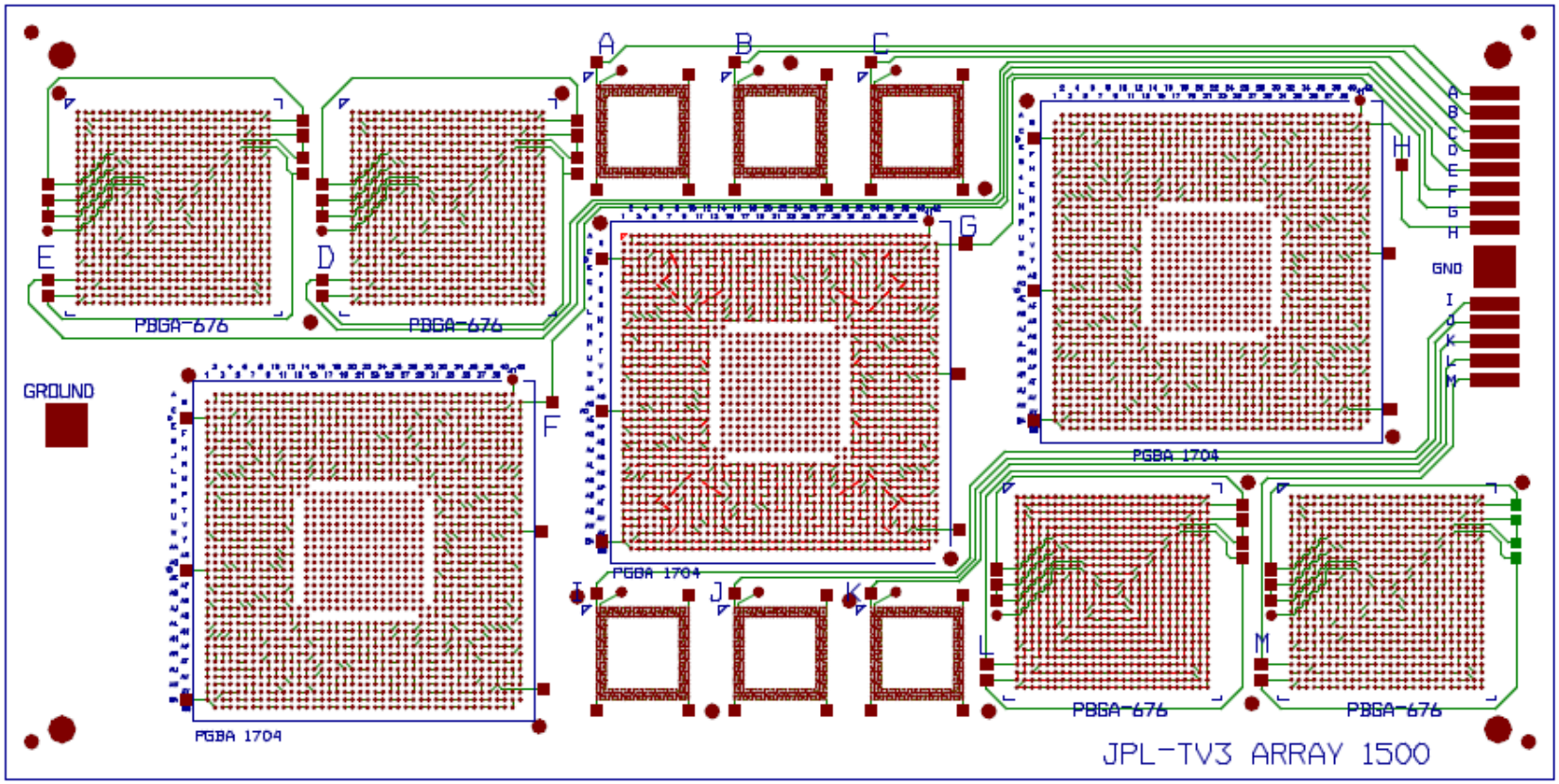
New Test Vehicle with >1500 I/O FCBGA & fine pitch CSPs



ALL LAYERS VIEWED FROM TOP SIDE (LAYER 1)

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References

http://NEPP.nasa.gov