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# **BOK—Printed Electronics**

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## **Objectives and Products**

The use of printed electronics technologies (PETs), 2D or 3D printing approaches either by conventional electronic fabrication or by rapid graphic printing of organic or nonorganic electronic devices on various small or large rigid or flexible substrates, is projected to grow exponentially in commercial industry. This has provided an opportunity to determine whether or not PETs could be applicable for low volume and high-reliability applications.

This report presents a summary of literature surveyed and provides a body of knowledge (BOK) gathered on the current status of organic and printed electronics technologies. It reviews three key industry roadmaps- on this subject—OE-A, ITRS, and iNEMI—each with a different name identification for this emerging technology. This followed by a brief review of the status of the industry on standard development for this technology, including IEEE and IPC specifications. The report concludes with key technologies and applications and provides a technology hierarchy similar to those of conventional microelectronics for electronics packaging. Understanding key technology roadmaps, parameters, and applications is important when judiciously selecting and narrowing the follow-up of new and emerging applicable technologies for evaluation, as well as the low risk insertion of organic, large area, and printed electronics.

**Key Words:** printed electronics, organic electronics, large area electronics, packaging hierarchy

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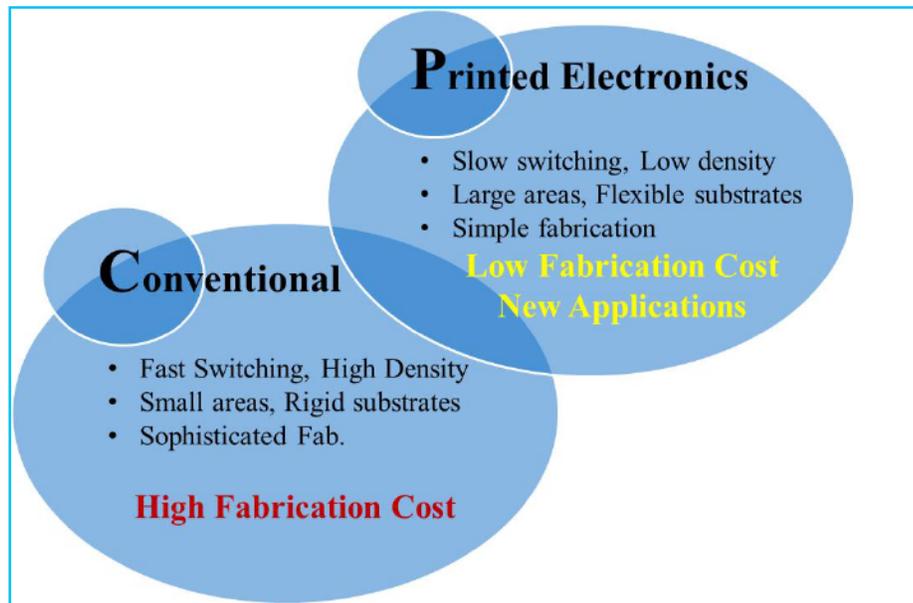
# 1. Printed Electronics Technology Trends

Printed electronics technologies (PETs) are emerging technologies that add significant advantages compared to the use of costly and inflexible conventional electronic systems. PETs can also be edible, biocompatible, and conformable/stretchable. For example, NASA recently (May 2013) awarded a contract to a company to make food “on-demand” from ingredients [1]—allowing for storage of ingredients instead of perishable prepared food—meeting the demand for food on long distance travel, such as humans going to Mars by 2030. Other projects pursued by NASA include nanotechnology ink and identifying ways PET can be effectively implemented into various aspects of spacecraft. One recent concept funded by NASA [2] utilizes the commercial technology of printed electronics to design and fabricate an entire end-to-end functional spacecraft—a significant technical challenge. The novel concept of applying PET in a multi-functional platform drives the current state of the art for functionality, as well as introducing design and manufacturing compatibility challenges among the functional subsystems. Current industry growth and commercial investment is expected to advance the functionality of available basic building blocks and components synergistically with NASA’s needs.

PET is complementary to silicon chip technology, which industry continues to find special applications for, with significant cost per area and throughput benefits. PET’s key advantages and disadvantages relative to conventional microelectronics are summarized in Figure 1. Even though PETs have significant drawbacks on speed due to longer switch time and device density, advantages include large area applications, use of flexible substrate, ease of fabrication, and much lower cost (which provides incentive for industry to continuously seek new applications). In summary, conventional electronics have continuously reduced cost per function (Moore’s Law); whereas PET reduces cost per area. Cost per function is still cheaper for silicon technology because of the significant miniaturization of integrated circuits (ICs) since their inception. In addition, to date, the performance of PETs in terms of actual function and reliability is less than that of conventional electronics.

Forecasters have gone as far as to predict that the market for PET will eventually outpace the silicon chip market; which itself grew from nothing to 200 billion dollars in about thirty years. The beginning of PET’s exponential growth starts now. For low-volume and high-precision applications, sheet-based techniques such as inkjet and screen printing, rather than roll-to-roll (R2R) printing, are best. For high-volume productions, such as solar cells, gravure, offset, and flexographic, printing methodologies are more common.

In addition to printability, other technology and process improvements are critical for the implementation of PET. These include optimization approaches for electrical functionality, functionality adjustment, and mechanical flexibility. For example, Figure 2 summarizes details of key technology challenges from performance improvement to killer application.



**Figure 1.** Comparison of key characteristics of conventional and printed electronics as complementary technologies.

- **Performance improvement**
  - Electrical performance
  - Material stability
  - Ease of processing
- **Feature size**
  - Resolution, registration, uniformity
  - Stability of the patterning processes
- **Materials**
  - Improvement of low-cost encapsulation, especially flexible transparent barriers
- **Standards**
  - Lack of standards/regulations for organic and printed electronics
- **Killer application**
  - No Moore’s Law yet
    - Charge carrier mobility, feature size, circuit complexity

**Figure 2.** Areas of technology challenges for printed electronics from performance improvement to finding a killer (large volume) application.

Irrespective of definition, the progress of PET has led to a multitude of possibilities in conception, design, fabrication, packaging, and application of devices and circuits. A few key aspects of PET discussed in this report are summarized in Figure 4. The report first focuses on roadmaps to provide a general survey of the technology, with emphasis on ultralow volume applications. Detailed roadmaps

of current status and future growth trends from three key roadmap industry societies—the organic electronics association (OE-A) [3], the international technology research society (ITRS)[4], and the international manufacturing initiative (iNEMI)[5] are presented. Then, specification-related activities by IEEE on generating specification for organic devices, by IPC addressing key design and assembly, and by other societies are discussed.

Finally, technology levels (hierarchy) are presented side-by-side, both for surface mount technology (SMT) and PET, in order to link the well-known established levels, e.g., device/package/system, in microelectronics with those potential levels for organic or printed electronics. This direct comparison better defines technology opportunities that are in-line with the author's experience, especially at the packaging level.

## 2. PET Roadmaps

### 2.1 PET Roadmap Organizations

Industry roadmap organizations have been created to address technology trends and to answer simple questions, such as what fields of technology do printed electronics encompass? Some examples are an interactive business card with a flexible display or a board game with a printed battery and flashing OLEDs. As shown, the scope and fields of applications for PET are highly diverse. A few years ago, an industry organization was created in Europe to categorize this diversity and to provide some guidance. One of these was the OE-A, whose focus was creating communications and developing interfaces for the various fields of research. The OE-A, with over 180 members worldwide, represents the entire value chain of organic electronics, from the materials, equipment, and product manufacturer to the end user and all applications. While many OE-A-generated concepts are still in the development phase, a series of applications are already in production. The OE-A recently published the fourth edition of the roadmap on organic and printed electronics.

The ITRS is the key industry roadmap provider for the conventional microelectronics field, and it is sponsored by the world's five leading chip manufacturers. The objective of the ITRS is to ensure cost-effective advancements in the performance of the integrated circuit and the products that employ such devices; thereby supporting the health and success of this industry. Recently, in 2013, ITRS team members gathered to discuss trends in printed electronics and associated technology developments.

iNEMI, a consortium of approximately 100 leading electronics manufacturers, suppliers, associations, government agencies and universities, is another industry roadmap provider. iNEMI roadmaps cover the future technology requirements of the global electronics industry by identifying and prioritizing gaps in technology and infrastructure. With the support of participant companies, iNEMI generates timely, high-impact deployment projects to address or eliminate those gaps. On the PET roadmap, the 2013 iNEMI roadmap has a chapter on Large Area, Flexible Electronics that provides a comprehensive update to its first edition, released in 2011, and is based on a number of announcements made by industry. The roadmaps for printed electronics provided by OE-A, ITRS, and iNEMI are further discussed in the following sections.

### 2.2 OE-A Roadmap

The OE-A, a working group within VDMA, was organized a few years ago to create a communication and development interface for various fields of research. It represents the entire value chain of organic electronics, from the materials supplier and equipment and product manufacturer through to the user. The OE-A's goal is to issue roadmaps that serve as a guide to the multitude of technical developments and help to define possible applications. While many of the developments of OE-A members are still in the test phase in the lab, a whole series of practical applications are already in use. The OE-A has published four roadmaps. An adapted summary version of the 4<sup>th</sup> map, which projects near-term to long-term growth and applications, is schematically shown in **Figure 3**. Here, the technology related to lighting and display are bundle together rather shown separately.

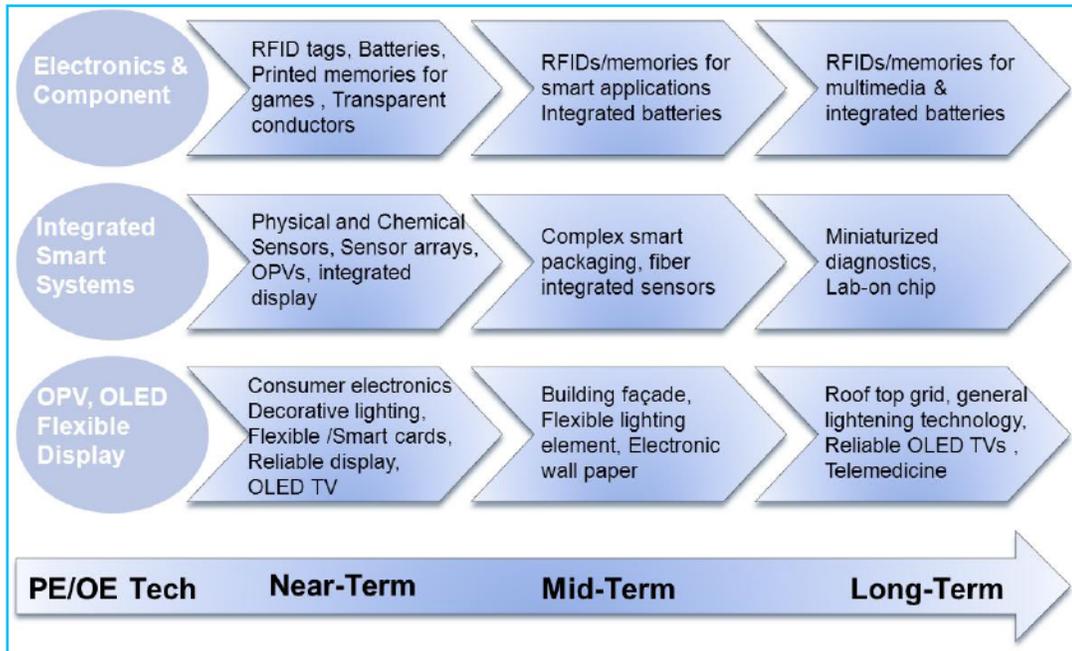


Figure 3. Adapted OE-A roadmap showing near-, mid-, and long-term key technology projections for printed electronics.

The three key areas defined are:

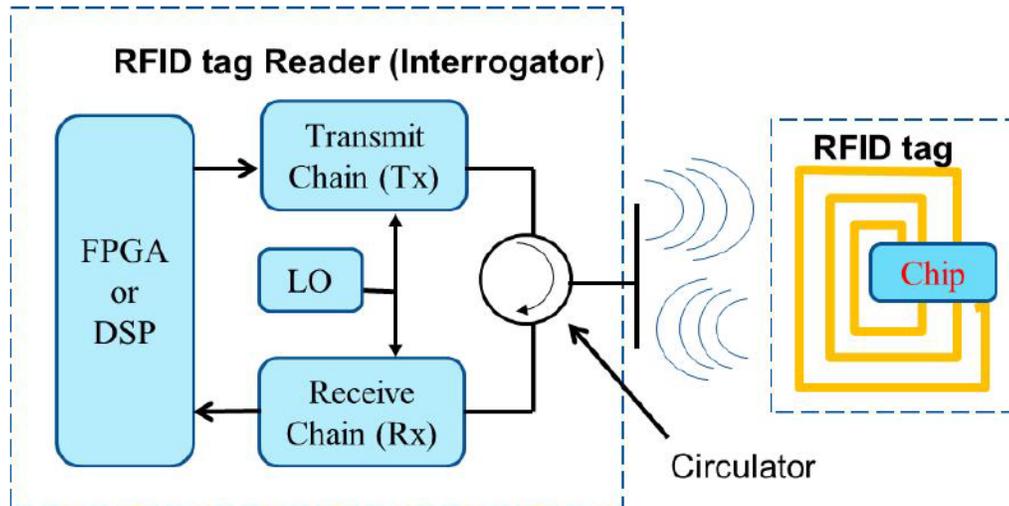
1. Electronics and components covering radio frequency identification, batteries, printed memory for games, and transparent conductors
2. Integrated smart systems including physical and chemical sensors, sensor arrays, and integrated displays
3. Organic photovoltaic (OPV), organic light emitting diode (OLED), and flexible displays, which encompass a large number of applications in consumer electronics, lighting, and flexible/smart cards.

Because of the diversity of technology in this report, only the first two categories will be discussed further as potential applications for microelectronics systems in low-volume applications. In the first category (electronics and components), printed RFID, memories, and flexible batteries have shown significant progress with new applications. Other application areas added recently within this category are printed conductors and passive components, printed antennas, printed circuits, and transparent conductive films. The second category (integrated smart systems) brings together multi-function devices to perform complex automated tasks without the need for external electronic hardware. Such system applications become more challenging, especially as technology progresses for organic and printed electronics. A typical printed electronic system may have a power sector (batteries, miniaturized fuel cells), input devices (physical, chemical and biological sensors), and output devices (displays, visual, audible or haptic interfaces and wireless communications)—all sections are integrated together using sophisticated logic and memory.

### 2.3 Printed RFID Roadmap

RFIDs enables the electronic labeling and wireless identification of objects using radio frequency communications. Because of low-cost fabrication and ease of remote identification, RFID technology is rapidly growing and is currently being used for various applications. An RFID system consists of a tag reader (also called the interrogator) and a tag. All communication between the tag and reader occurs completely through a wireless link that is sometimes called an air interface. Through a

sequence of commands sent and received between both devices (called the inventory round), an RFID reader can identify the electronic product code (EPC) of an RFID tag. **Figure 4** shows a basic block diagram of the tag/reader system. For passive tags, the basic idea is that the interrogator initiates an interrogation round with a query command. The query command essentially “wakes up” the tag, which responds with the appropriate information.



**Figure 4.** Block diagram of a typical RFID tag/reader system.

Printed RFID with limited functionality is a major solution for meeting the growing market demand for low cost and high-volume (see **Figure 5**). The logic circuit with the memory is printed on the basis of either organic or printed electronics platform technology. The antenna can be either standard, like today (e.g., etched copper or aluminum), be printed with conductive inks, or by other additive processes. Besides the low cost of printed tags they also have advantages due to their smaller thickness, flexibility, and better ecological properties compared to standard tags. Increases in frequency of data rate and memory are expected to become mature in a few years for full printed UHF RFID (at 800 to 900MHZ). Communication is another aspect that is continually improving.

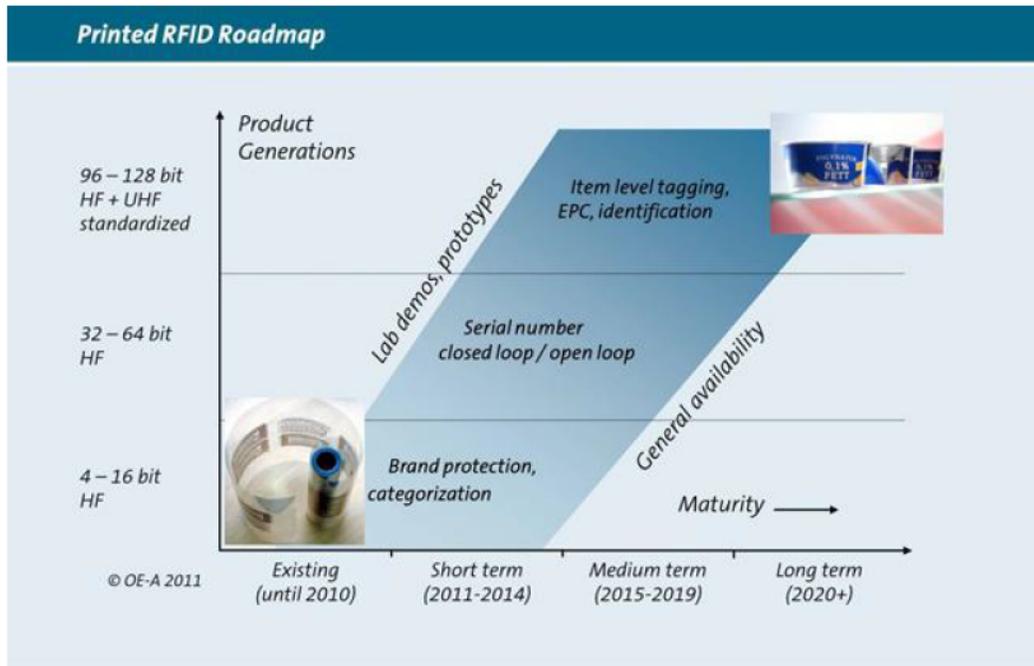
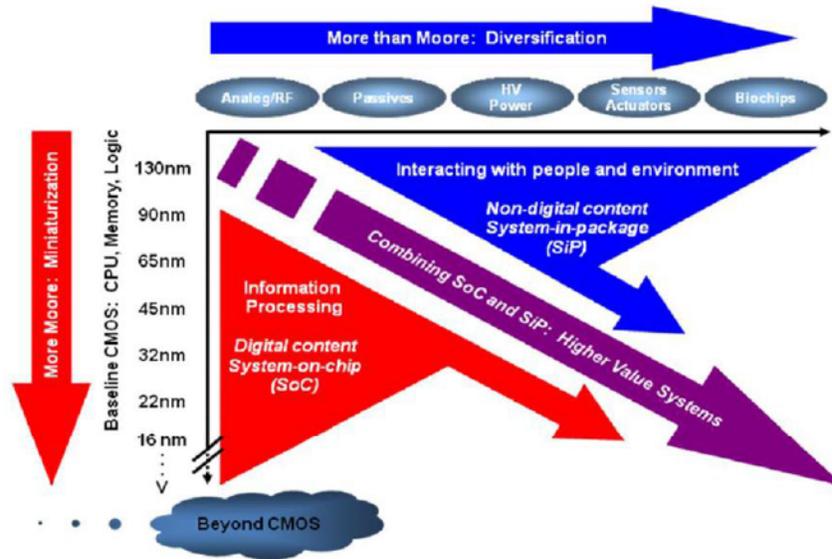


Figure 5. Roadmap for printed RFID projection (OE-A, fourth edition[3]).

## 2.4 ITRS PET Roadmap

For five decades, the semiconductor industry has distinguished itself by the rapid pace of improvement in its products-based miniaturization level. This is usually expressed as Moore's Law, but is also sometime called scaling. The most significant trend is the decreasing cost-per-function, which has led to substantial improvements in economic productivity and overall quality of life through proliferation of computers, communication, and other industrial and consumer electronics. To help guide these R&D programs in scaling, the Semiconductor Industry Association (SIA) met with corresponding industry associations in Europe, Japan, Korea, and Taiwan to participate in a 1998 update of its roadmap and to begin work toward the first ITRS, published in 1999. Since then, the ITRS has been updated in even years and fully revised in between years. The latest 2012 update is available on the ITRS website [4]. Figure 6 shows the ITRS roadmap for printed CMOS Moore's Law, and beyond which is later called "More than Moore" or its abbreviation, MtM.



**Figure 6.** ITRS Roadmap for printed CMOS Moore's Law and beyond, MtM.

The ITRS projects that by 2020–2025, many physical dimensions are expected to be crossing the 10 nm threshold. It is expected that as dimensions approach the 5–7 nm range it will be difficult to operate any transistor structure that is utilizing CMOS physics as its basic principle of operation. It is also expected that new devices, like the very promising tunnel transistors, will allow a smooth transition from traditional CMOS to this new class of devices to reach these new levels of miniaturization. However, it is becoming clear that fundamental geometrical limits will be reached in the above timeframe. By fully utilizing the vertical dimension, it will be possible to stack layers of transistors on top of each other. This 3D approach will continue to increase the number of components per  $\text{mm}^2$  even when horizontal physical dimensions will no longer be amenable to any further reduction.

ITRS recognized the limitations of Moore's law (i.e., linear scaling) and proposed a methodology to identify those MtM technologies for which a roadmapping effort is feasible and desirable. The semiconductor community needs to depart from the traditional scaling "technology push" approach and involve new constituencies in its activities. ITRS materialized this new approach in 2011, when it added a MEMS chapter to the roadmap, and also aligned it with iNEMI roadmap. The MEMS chapter aligns its effort towards those MEMS technologies associated with "mobile internet devices," a driving application broad enough to incorporate many existing and emerging MEMS technologies.

Even though there is no information in the current ITRS roadmap on printed electronics, a few ITRS team members recently met twice in conjunction with the IEEE Advanced Packaging Materials Symposium (IEEE APM, March 2013) to discuss key trends, current status, and potential applications for nanomaterials technology and display. Draft documents of the trend in these technologies were generated and distributed to participant team members; these are yet to be released. Key discussion topics on printed electronics included conductors, semiconductors, and opaque technologies. Trends in semiconductors presented in the following are intended for discussion purpose only.

## Semiconductors

### 1. 1D/2D Carbon (Carbon nanotubes, graphene)

- ✓ Cost
  - Low-defect graphene

- Low-cost single wall CNTs
- ✓ Purity
  - Chirality control in production or purification at low cost
- ✓ Interconnect of Transistors
  - Ohmic contacts to nanotubes for power delivery
- ✓ Durability of Doping
  - Long-term spatial distribution stability of dopants
- 2. *Polymers*
  - ✓ High resistance => Slow Transistors
  - ✓ Low processing temp.
  - ✓ Temp. dependence, photonic, degradation ..... durability
- 3. *1D/2D Si*
  - a. Too early for us to forecast: We don't know enough today

## 2.5 iNEMI PET Roadmap

The 2013 iNEMI's Large Area, Flexible Electronics Roadmap Chapter is building upon the 2011 first edition [5]. It added a comprehensive update based on a number of announcements made by industry since the previous publication. In addition, the iNEMI team identified paradigm shifts, enablers, and show stoppers (see [Figure 7](#)). One key paradigm is the transition from the beginning of the 21<sup>st</sup> century vision for completely printed electronic products to 'hybrid' products, where traditional electronic components are used in combination with printed components. Other paradigm shifts include cost per area of functionality versus cost per function for silicon chip and integration of electronics in non-traditional objects and locations – ubiquitous electronics. A few gaps and show stoppers are also identified and presented. For example, it states that rate of commercialization of materials and manufacturing/processing equipment is occurring too slowly to meet the cost/performance/utility demands to enable near-term product launches. Additionally, the rate of development of systems must accelerate—otherwise a window of opportunity may be lost for a disruptor to commercialize a new competitive product.

- **Paradigm Shifts**
  - All PE to “hybrid” products
  - Cost per area rather than cost for function
  - Non-traditional integration- Ubiquitous electronics
  - Scalable and high volume production
  - Novel form factor and low-cost electronics
- **Enablers**
  - Establish best-in-class manufacturing
  - Develop low temp interconnect materials
  - Improve materials/processes
  - Develop high performance/stable organic/inorganic/hybrid
  - Advance design and layout products

**Figure 7.** iNEMI 2013 roadmap identification of paradigm shifts and enablers.

Seven areas of opportunity were identified by an industry survey performed by the iNEMI team. Those surveyed further predicted that the near-term commercialization opportunities will continue to be lighting, power (battery), and sensors (biological, chemical, and touch) followed later by the introduction of RF devices (anti-tampering and authentication), photovoltaics, and displays. As with silicon-based component/subsystem technologies, it is envisioned that the technology and applications will mature over time, offering additional opportunities for integration into product emulators. As an example, as these technologies become more robust, it is possible that memory products may be developed for the Aerospace and Defense industries. **Table 1** identifies potential opportunities for integration as performance improves over the next 10 years.

**Table 1.** iNEMI 2013 product emulators and potential application opportunities.

| <b>Industry</b>   | <b>Display Modules</b> | <b>Lighting Systems</b> | <b>Memory Components</b> | <b>Power</b> | <b>RF Devices</b> | <b>Sensors</b> |
|-------------------|------------------------|-------------------------|--------------------------|--------------|-------------------|----------------|
| Aerospace/Defense | X                      | X                       |                          | X            |                   | X              |
| Automotive        | X                      | X                       |                          |              |                   | X              |
| Consumer/Portable | X                      | X                       | X                        | X            | X                 | X              |
| High End Systems  |                        |                         |                          |              |                   | X              |
| Medical           | X                      | X                       | X                        |              | X                 | X              |
| Office Systems    | X                      | X                       |                          |              |                   | X              |

Near-term opportunities are classified as either 1) non-hybrid—an application that is comprised of only the emerging technology or 2) hybrid—an application that is manufactured using traditional electronics and devices, circuits, or components based on the new technology, e.g., a product with a printed display module and a silicon IC RF front-end. For non-hybrid application, one technical

barrier concerns the development of in-line manufacturing quality control equipment. To benefit from the economies of scale that R2R and printing offers, systems must be developed and qualified for testing of the fabricated devices, circuits, and components.

Conversely, hybrid flexible electronics systems comprised of printed electronics-based components (sensors, power, indicators, signage) integrated with traditional electronics (surface mount technology for passive devices and silicon based ICs) continue to receive greater attention for near-term commercialization opportunities. In order to achieve further commercialization, a dedicated, hybrid manufacturing platform must be developed. iNEMI envisions that an R2R manufacturing platform combining several printing technologies (e.g., flexography, gravure, and micro dispensing) is required to enable realization of the market potential.

## 3. Specifications for PET

### 3.1 Key Specifications

IEEE was among the first to recognize the importance of generating standards for PE devices and new emerging technologies, such as nanotechnology materials [6]. Recently, IPC-JPCA (IPC—Association Connecting Electronics Industries® and JPCA—Japan Electronics Packaging and Circuits Association) released a joint specification, the first operational-level standard on printed electronics [7]. Other industry societies are joining this trend; representatives are listed in **Figure 8**. This Figure includes the IEEE P1620™ for nanomaterials, an element of PE technology.

- **IEEE**
  - 1620.1™ -Test Methods for the Characterization of Organic Transistors and Materials
  - P1620™ -Organic Field Effect Technology- Standard Test Methods for the Characterization of Organic and Molecular Transistors and Material
- **IPC**
  - IPC/JPCA 2291 – Design Guidelines for Printed Electronics, Draft Jan 2013
- **ASTM**
  - ASTM F1662-10... , Standard Test Method for Verifying Specified dielectric Withstand Voltage and Determining the Dielectric Breakdown Voltage of a Membrane Switch
- **IEC** (International Electrotechnical Commission)
  - TC 119 Printed Electronics

**Figure 8.** Key specifications for printed electronics technology by industry societies.

### 3.2 IEEE Specifications

It is interesting to note that during development of nanotechnology specification, the term “anticipator standards” was used because the technology was not yet mature. The definition and benefits of the IEEE anticipator standards are:

1. Creation of standards in anticipation of the manufacturing of value added products,
2. Provide an approach to help drive early commercialization in emerging fields and to promote acceptance among producers, users and the public, and
3. Creation of a standing group, which provides a forum to consider new standards projects.

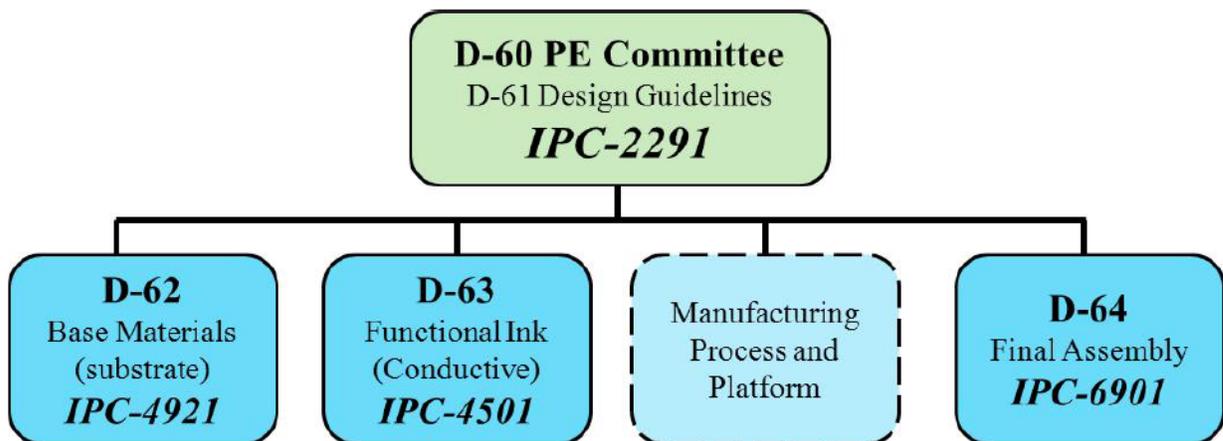
The anticipator standards also guide the development of white papers into standards and revise existing standards, e.g., the IEEE 802™ committee, which deals with both wired and wireless networking standards. This committee decided to start with the family of anticipatory nanotechnology standards, IEEE P1650™ in particular. to focus first on material characterization methods and

equipment. Then, standards followed that concern device and component fabrication and testing, followed by systems architecture and interoperability.

IEEE 1620-2008—Standard for Test Methods for the Characterization of Organic Transistors and Materials. This standard recommends methods and standardized reporting practices for electrical characterization of printed and organic transistors. Due to the nature of printed and organic electronics, significant measurement errors can be introduced if the electrical characterization design-of-experiment is not properly addressed. It describes the most common sources of measurement error, particularly for the high-impedance electrical measurements commonly required for printed and organic transistors. It also suggests recommended practices in order to minimize and/or characterize the effect of measurement artifacts and other sources of error encountered while measuring printed and organic transistors.

### 3.3 IPC Specifications

A few years ago, IPC stakeholders began to identify printed electronics as a potential game changer and suggested that the field should be closely monitored. The exploratory standards working group meeting held in late 2010 became the foundation for the present IPC Printed Electronics Standards Portfolio development effort (see Figure 9). A dynamic strategy was adopted by the IPC Printed Electronics Standards Committee (D60) to respond quickly based on industry trends and market dynamics with the formation of subcommittees (D61-D64) to effectively generate specifications on PE. The status of these specifications are as follows.



**Figure 9.** IPC committee and subcommittee for printed electronic technology specification development and current specifications identification.

IPC-2291: Design Guidelines for Printed Electronics provides an overview of the design process flow for printed electronics based devices, modules and units, and final products. The intent of this generic specification is to establish a design process flow that will facilitate and improve the practice of PE design. It is “generic” because it specifies only information that forms the basis for further specific declarations. It is therefore intended to be used in conjunction with other documents, as needed.

IPC-4921, released June 2012: Requirements for Printed Electronics Based Materials, a key structural material for the field of PE covering five substrate categories. These categories capture the broad families of substrate materials. As new substrate materials are introduced into the field of PE they will be added to the list appearing in IPC-4921. The IPC-4921 document has been referred to as

fundamental for the field of printed electronics. Moreover, it is considered by many to be one of the most critical drivers of manufacturing innovation. The paradigm shift that flexible substrates offers for transitioning from batch to roll-fed and roll-to-roll manufacturing is considered paramount for realization of vibrant new areas of manufacturing growth. In its release announcement, IPC states that “IPC/JPCA-4921 provides a starting point for IPC’s Printed Electronics Initiative to establish a critical segment of the infrastructure that will help the industry expand more quickly”. The IPC committee started to work on Revision A of this specification in late 2013.

IPC/JCA 4591, released Dec. 2012: Requirement for Printed Electronics Functional Conductive Materials provides data to help users more easily determine material performance, capabilities, and compatibility of functional conductive materials for the manufacture of printed electronics. It includes: 1) classification schemes based on composition, conductor type, and post-processing structure; 2) functional conductive material specification sheets to present properties for the different conductive material types; and 3) the most current classification system, qualification and quality conformance requirements, including those raw material properties of particular interest to the printed electronics designer, fabricator, or other user. The IPC committee started to work on Revision A of this specification in late 2013. The word “Conductive” was dropped from the title to accommodate new printed materials.

IPC 6901, yet to be released: Performance Requirements for Printed Electronics Assemblies. Final Assembly Subcommittee met in 2012 and drafted the table of contents for this specification as stated in the IPC updated document. The subcommittee identified documents from ISO defining RFID structures and ASTM defining membrane switches as possible reference documents.

## 4. Technologies and Hierarchy

### 4.1 Surface Mount Technology Hierarchy

For Surface Mount Technology (SMT), packaging hierarchy has been expanded to define different manufacturing and system levels. A similar adoption by industry for printed electronics elements and system level definitions (e.g., defining interconnects between system levels) allows value chain participants to capture value and enable innovation. Furthermore, the acceptance of definitions allows value chain members to develop materials and technologies optimized for use within specific system levels. The JISSO International Council (JIC), comprised of Asian, European and North American members, is aimed at promoting a strategic partnership among organizations interested in the total solution for electronics interconnecting, assembling, packaging, mounting, and integrating system design. Figure 10 shows a recent proposal by JISSO for expanding packaging hierarchy [8].

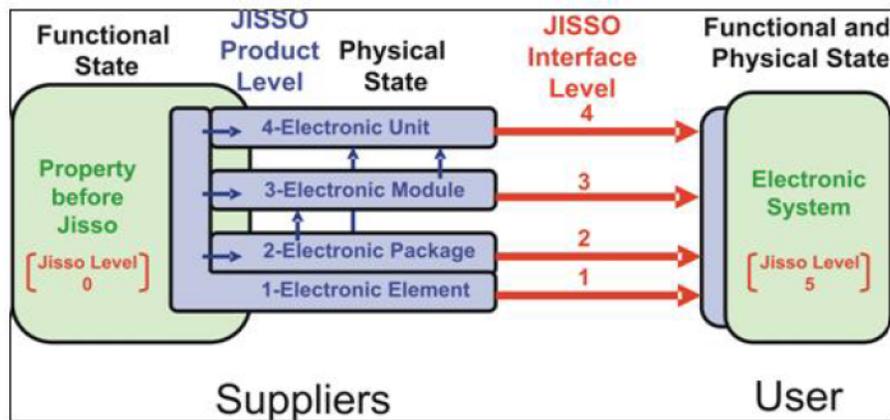


Figure 10. SMT packaging hierarchy presented by JISSO [8].

The definition of interconnection hierarchy includes the following [5,8,9].

**Level 0 - Electronic Element:** The intellectual property of an item pertains to the idea or intelligence imported or described in a formal document (protocol, standards and/or specifications), design entity or patent disclosure. The information may be in hard or soft copy and can include computer code or data format as a part of the descriptive analysis. The characteristics are described as to their physical, chemical, electrical, mechanical, electromechanical, environmental, and/or hazardous properties.

**Level 1 - Electronic Element:** Uncased bare die or discrete components (e.g., resistor, capacitor, diode, transistor, inductor, fuse), with metallization or termination ready for mounting. This can be an IC or a discrete electrical, optical, or MEMS element. Individual elements cannot be further reduced without destroying their stated function.

**Level 2 - Electronic Package:** A container for an individual electronic element or elements that protects the contents and provides terminals for making connections to the rest of the circuit. The package outline is generally standardized or meets guideline standards. The package may function as electronic, optoelectronic, or MEMS, or System in Package (SiP), and may in the future include bio-electronic sensors.

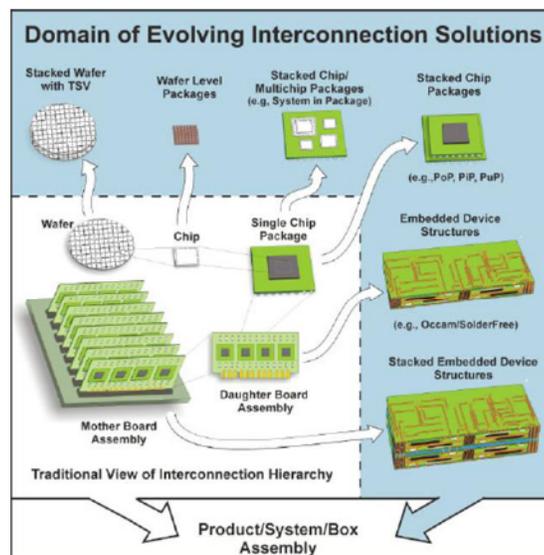
**Level 3 - Electronic Module:** A electronic sub-assembly with functional blocks, which is comprised of individual electronic elements and/or component packages. An individual module having an application-specific purpose including electronic (including SiP), optoelectronic, or mechanical (MEMS). The module generally provides protection of its elements and packages, depending on the

application to assure the required level of reliability. The module may be a company standard (catalog item) or custom (OEM-specific). Note: there will likely be some subdivisions of Level 2 and Level 3 descriptions to increase the granularity and clarity relative to what is included within each of these levels.

**Level 4 - Electronic Unit:** Any group of functional blocks that have been designed to provide a single or complex function needed by a system in order for the system to serve a specific purpose. The electronic unit may be comprised of electronic elements, component packages and/or application - specific modules. The function of the electronic unit may be electronic, optoelectronic, electromechanical, or mechanical or any combination thereof. The function may in the future include bio-electronic applications.

**Level 5 - Electronic System:** A completed, market ready unit dedicated to combining and interconnecting functional blocks. The functional blocks are generally comprised of electronic units, but may also include electronic modules, electronic packages, or electronic elements. The electronic system product can include the cabinetry, a backplane or motherboard into which the assemblies, modules, packages, or elements are inserted and the cabling (electrical, optical, or mechanical) needed to interconnect the total functional block(s) into a configured system. The electronic system can vary in complexity from very simple to highly complex.

The interconnect hierarchy has evolved since the introduction of the transistor in 1960 [9]. **Figure 11** compares the traditional view of the hierarchy (lower left) to the emerging microelectronic technologies with growing ambiguity in interconnection level definition. In the early days, the divisions of levels for the various tasks involved in the creation of an electronic system were well defined. The semiconductor manufacturer created the integrated circuits(IC); the IC chips were packaged for protection; a printed circuit facility build a substrate according to a design. Next, the package was assembled onto board using soldering process and used as “daughter card” for the next assembly of motherboard. The completed assembly would then be packaged in a suitable format, whether a computer, telephone switch, internet router, or any other product. Now, there are new interconnections, such as a wafer-level packages and 3D stacks; some lack a clear category or definition. The blue area in the Figure shows added new interconnections with lack of clear category; therefore, there is a need to find a way to embrace the emerging technologies that are already being deployed to create next generation products.

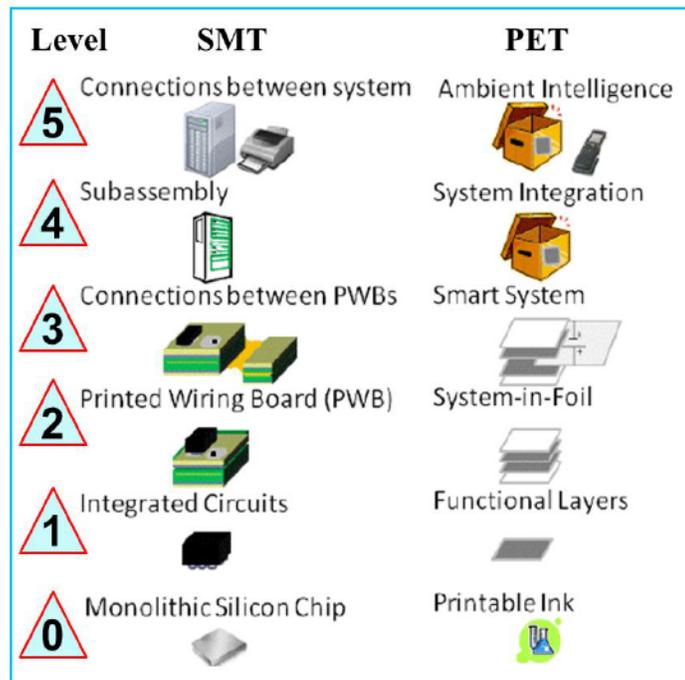


**Figure 11.** Expansion of SMT packaging hierarchy with inclusion of new developments in packaging, including wafer levels and 3D stacks[9].

## 4.2 Printed Electronics Technology Hierarchy

For the purpose of comparison to printed electronic technology, key system levels of SMT can be simply defined as follows: a) Level 0 - silicon IC, b) Level 1- IC packaging, c) Level 2 - printed wiring board (PWB) manufacturing and board assembly, d) Level 3 - interconnections between different PWB's, e) Level 4 - assembly of the PWB into racks, housings of product, etc., and f) Level 5 - connection of several individual products or systems.

For printed electronics technology, levels of hierarchy can be defined similar to those of silicon, driving the SMT hierarchy as shown in **Figure 12**.



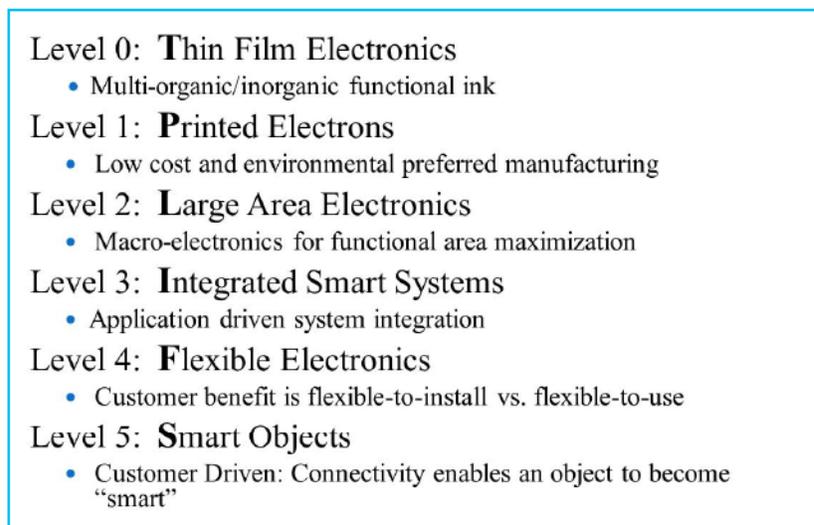
**Figure 12.** Comparison of SMT and PET device/package/system hierarchy.

The PET hierarchy can be simply defined as follows [10]:

- Level 0, basic material elements for PET system operations such as organic and inorganic functional inks. Functional inks have intrinsic properties such as – emitting light in OLEDs devices, energy harvesting in OPV cells, piezo / pyro effects in sensors, and conductivity in traces and antennas.
- Level 1, packaging level or functional layers for PET. The functional layers can be fabricated on a coated paper, plastic or metal foil. It can be a single layer such as in the case of a conductor (e.g., an antenna), printed electronics, or it can be combination of multiple layers. For sensors, three or more (structured) layers can be used, while for OLEDs and OPVs the number of layers can be much higher.
- Level 2, the system-in-foil level, is defined as the combining of stacks of functional layers, e.g., the integration of a first stack having an antenna with a second stack having logic. Another example is the front and back planes that form a display. The stacks may be based on different technologies and could include embedded or mounted ICs or SMT components

- (resistors, capacitors, inductors, etc.). Also, stacks that form Level 2 can be individually tested.
- Level 3, the smart-system level, represents the hierarchical level where multiple system-in-foils are integrated or linked together. The individual system-in-foils are pretested and sorted to ensure high yield of the smart system. Typical examples include batteries and displays connected with other system-in-foils to provide power and visual content to an existing printed system design.
  - Level 4, the system integration level, defines the level at which smart systems are integrated into or mounted onto a structural housing, frame, package, etc. This level is enabled due to the novel feature provided by this technology – flexible design for integration, e.g. laminate, attach.
  - Level 5, the ambient intelligence level, is the highest level and is characterized when the system has a “touch-point” to the rest of the world - hierarchy level when the functional product is integrated with its surroundings. As an example, this is the level at which OPV or OLED systems are connected to the power grid or lighting infrastructure. A variety of connection methods can be used, such as RF or optical hardware.

**Figure 13** summarizes the hierarchy for large area smart systems. The range encompasses large area smart systems, with level 0 as thin film electronics build by multi-organic/inorganic functional ink to level 5, which covers connectivity that enables an object to become “smart”.



**Figure 13.** Hierarchy device/packaging/systems levels for large area printed electronic sensors.

### 4.3 Printed Electronics Technology Performance

The technology performance parameters discussed in this section are more “fundamental” and describe fundamental material, device or process properties rather than specific requirement for each application. Here, only a small number of the key technology parameters identified for the various applications are listed, emphasizing those that are relevant to a number of applications[9].

- Mobility/electrical performance (threshold voltage, on/off current): the performance (operating frequency, current driving capacity) of the circuits depends on the carrier mobility of the semiconductor, the conductivity of the conductor and the dielectrical behavior of the dielectric materials.

- Resolution/registration: the performance (operating frequency, current driving capacity) and reliability of the circuits depends on the lateral distance of the electrodes (resolution) within the devices (e.g. transistors) and the overlay accuracy (registration) between different patterned layers.
- Barrier properties/environmental stability: the lifetime depends on a combination of the sensitivity of the materials and devices to oxygen and moisture, as well as the barrier properties of protective layers, substrates and sealants against oxygen and moisture. The necessary barrier properties vary for the different applications over several orders of magnitude.
- Flexibility/bending radius: thin form factors and flexibility of the devices are key advantages of organic and printed electronics. In order to achieve reliable flexibility and even rollable devices materials, design and process have to be chosen carefully.
- Fit of process parameters (speed, temperature, solvents, ambient conditions, vacuum, inert gas atmosphere): in order to have a sufficient working system, it is important to adjust the parameters of the different materials and devices used to build organic and printed electronics.
- Yield: low cost electronics in high volumes are only possible when the processes allow production at high yields. This includes safe processes, adjusted materials and circuit designs as well as an in-line quality control.

## 5. Additive Manufacturing/3D Printing

### 5.1 Introduction

Additive manufacturing (AM) or 3D printing is a process for building up a three-dimensional solid object, layer-by-layer, from a 3D digital model. It is an additive process, contrary to traditional machining, which is a subtractive process. Innovation in AM technology is critical for wider applications. On May 9, 2013, the US government announced a competition to create three new manufacturing innovation institutes across five agencies. NASA has been fully engaged with the partners in the National Additive Manufacturing Innovation Institute (NAMII, a.k.a, America Makes); it recognizes that on Earth and potentially in space, additive manufacturing can be game-changing for new mission opportunities. The additive manufacturing technologies expected to significantly reduce production time and cost by 'printing' tools, engine parts or even entire spacecraft. The 3-D printing manufacturing offers opportunities to optimize the fit, form, and delivery systems of materials that will enable space missions while directly benefiting American businesses here on Earth.

### 5.2 Key AM for Metallic Materials

Applying additive manufacturing to aerospace has been emphasized by the development of high-value materials such as Ti-based alloys and Ni-based superalloys [12-15]. Ti-based alloys, specifically Ti-6Al-4V, are commonly used in space applications—there are over 1000 Ti-6Al-4V parts in one spacecraft including parts with complex geometry. This category of parts is expensive and time consuming to fabricate using conventional manufacturing because titanium is generally difficult to process and to machine. These challenges make Ti-6Al-4V parts an ideal target for using additive processes.

The most common AM approaches for the manufacturing of metal parts are : (1) the powder bed fusion processes such as electron beam melting (EBM), (2) selective laser melting (SLM), and (3) direct energy deposition such as laser engineered near shaping (LENS). Presently, the EBM appears to be the most mature methodology for building up fabrication of Ti-6Al-4V parts since there also exists some materials property database; a number of aerospace parts are already fabricated. A large number of aerospace companies have developed, produced, characterized and approved some EBM-processed Ti-6Al-4V parts.

The AM version of Ti-6Al-4V can compete with its wrought version. In a recent study [12], it was shown that the static and dynamic mechanical properties of Ti-6Al-4V, which was electron beam melted plus hot isostatic pressed (HIP), become comparable to or exceed their classical wrought annealed properties. The author recommended to accelerate the infusion of 3D printing for spaceflight applications by developing the statistical property database for effectively using the additive manufacturing technologies.

Key advantages and disadvantages of using AM materials are:.

*Advantages of additive manufacturing:*

- Reduction in cost of manufacturing (e.g., about 50% less for Ti-6Al-4V)
- Production of parts is significantly faster (e.g., twice as fast for Ti-6Al-4V)
- Manufacturing of complex geometries and designs are possible, which cannot be done by traditional processes
- A higher manufacturing flexibility. Parts can be quickly replaced if needed
- A greener manufacturing process since it produces much lower waste scrap compared with subtractive material process with significant scraps (e.g., more than 75% less scrap for Ti-6Al-4V)
- Creation of new, tailored materials is possible

- The development of gradient alloy is possible [12]
- Improvement in properties of some material is possible
- Reduction in cost/time in building prototypes
- Multiple iterations of a prototype can be easily made
- Reduction in time for design reviews and manufacturing steps
- Detection of discrepancies in designs and fast revision during the early stages of the project

*Disadvantages of additive manufacturing:*

- Better suited for production of smaller runs only. AM techniques tend to be more expensive for large production runs
- Better suited for production of smaller part sizes only. Presently, low build speeds and technical limitations tend to limit AM to shapes where relatively smaller parts (such as one cubic foot) are needed.
- Lack of database for materials properties. Currently, publically available data is inadequate for designing of flight-quality AM parts.

### **5.3 AM Materials and Challenges**

Additive manufacturing offers an ideal platform for developing new products and applications. It creates the material (i.e. the metallurgy) locally in the laser or electron beam focus during the production of the part. This gives unprecedented possibilities to create new, tailored materials and/or material gradients, including materials that cannot be manufactured by other means. Due to the additive build-up of the parts, it is also possible to vary the geometry and the internal structure of the material by numerous methods, which offers possibilities for designing and optimizing part properties and behavior by geometrical layering, in addition to chemical bonding. The result is an expanded range of possibilities for designing parts to be produced by AM in the future.

Recently, the additive manufacturing industry has grown significantly with markets including prototyping, tooling, direct part manufacturing, and maintenance and repair. The introduction of aerospace materials for AM has been successful in increasing acceptance, and has already led to many requests for additional materials. Since a very broad range of metal materials can be processed by this technique, it is to be expected that the number and range of aerospace and commercially available materials will continue to grow.

Additive manufacturing was the subject of the NASA administrator's message when he was summarizing the development of technology for the future [16]. Briefly stating a number of innovations, it cited the joint effort with Aerojet Rocketdyne that hot-fire tested a "3D printed rocket engine injector", enabling a first step in using AM to support wider space applications. The citation is a reference to a previous official announcement [17] that two rocket engine injectors made with a 3D printer performed as well as traditionally constructed parts during the hot-fire tests, which exposed them to temperatures approaching 6,000°F (3,316°C) and extreme pressures.

Despite significant progress in the AM field, a number of technical challenges related to materials, equipment, and applications remain. Issues such as material characterization and development of statistical property database, material development, process control, process understanding in modeling, machine qualification and modularity among others have been identified by industry as areas for improvement. Though many issues are being examined by researcher teams in academia, industry, and government, it is perceived that coherent efforts among these teams with appropriate funding will enable resolutions of technical challenges and faster implementation of the additive manufacturing technology.

## 6. Summary

Printed electronics takes over where silicon chips cannot cope. For example, PE can provide simple electronic circuits at one tenth of the cost of those in a simple silicon chip, but it can also be edible, stretchable, conformal (fitting over uneven surfaces), even transparent, though not simultaneously. NASA recently funded JPL and industry partners for using this technology to address its effective implementation into various aspects of spacecraft. The concept is “to apply printed electronics in multi-functional platform by implementing every subsystem that a spacecraft might need from the scientific sensor through the data downlink and have it survive and function in a space environment.” If to include other aspects of this technology such as nanotechnology and additive manufacturing, then, NASA is heavily involved in advancing the printed electronics and 3D technologies forward.

While a “killer application” for printed electronics technology has yet to be identified allowing industry to focus on the development of key technologies and supply chains; nevertheless, there are numerous unique applications emerging that will change the direction of electronics. A few key points on PET discussed in this report are summarized below:

- It is forecasted that the PET market will outpace silicon chip electronics because of its ubiquity.
- For ultralow volume and precision applications, sheet based techniques such as inkjet and screen printing with ink or other materials are more suitable.
- It is advisable to continuously reviewing roadmaps generated from key industry including OE-A, ITRS, and iNEMI to define the pulse of development and potential areas for application and further investigation.
- Review and adopt or adapt applicability of industry specifications, including those by IEEE and IPC.
- To meet the current needs of microelectronics applications, a hybrid approach combining the advantages of both silicon chip and printed electronics may be considered.
- Understanding the hierarchy of device/package/systems enables users to better define key implementation and reliability challenges for effective use of PETs.
- Briefly discussed key technology performance parameters for various applications. These included electrical performance, resolution, environmental stability, level of flexibility, process parameters, and yield.
- Briefly discussed additive manufacturing, a.k.a, three-dimensional (3D) printing, approaches; their advantages and disadvantages for use of high value metallic materials such as Ti-6Al-4V. Also, briefly discussed future needs and technical challenges for effective implementation of the AM technology.

Understanding key technology development and the characteristics of printed electronics technologies and additive manufacturing—advantages and disadvantages—are important in judiciously selecting and narrowing the follow-up applicable technology, and quality assurance and reliability test methods in preparation for low-risk insertion into electronic or non-electronics systems for NASA use.

## 7. Acronyms and Abbreviations

|        |   |
|--------|---|
| AM     | additive manufacturing  |
| ASTM   | american society for testing and materials  |
| BOK    | body of knowledge   |
| CMOS   | complementary metal oxide semiconductor   |
| EPC    | electronics product code  |
| IC     | integrated circuit  |
| IEEE   | institute of electrical and electronics engineers   |
| iNEMI  | international electronics manufacturing initiative  |
| IPC    | association connecting electronics industries   |
| ISO    | international organization for standardization  |
| ITRS   | international technology research society   |
| JIC    | JISSO international council   |
| JISSO  | Japanese acronym for a total solution for interconnecting, assembling, packaging, mounting, and integrating system design |
| JPCA   | Japan electronics packaging and circuits association  |
| JPL    | Jet Propulsion Laboratory   |
| LCD    | liquid crystal display  |
| LED    | light emitting diode  |
| MEMS   | micro-electro-mechanical systems  |
| MOSFET | metal oxide field effect transistor   |
| MtM    | more than Moore   |
| OE-A   | organic electronics association   |
| OLED   | organic light emitting diode  |
| OLED   | organic light emitting diode  |
| OPV    | organic photovoltaic  |
| OTFT   | organic thin film transistor  |
| PET    | printed electronics technology  |
| PWB    | printed wiring board  |
| R2R    | roll to roll  |
| RF     | radio frequency   |
| RFID   | radio frequency identification  |
| SIA    | semiconductor industry association  |
| SMT    | surface mount technology  |
| TFT    | thin film transistor  |
| OTFT   | organic thin film transistor  |
| VDMA   | verband deutscher maschinen- und anlagenbau (German engineering federation)   |

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