National Aeronautics
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SOC SEE Test Guideline Development

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Outline

- Motivation and Structure
- Needed Radiation Data
- Test and Test Device Preparation
- Testing
- Reporting
- Sample Results
- Conclusion

Motivation

- Many space programs are using or designing around modern SOCs – i.e. Freescale P2020
- Space part manufacturers are providing RHBD SOCs – i.e. Aeroflex UT699, BAE e5500-based microprocessors
- JPL microprocessor SEE guideline (Irom, 2008) needs update for modern devices.

- Want to provide here:
  - Taste of what's in the guideline – highlighting some key information
  - General overview of what to expect

Interest in SOCs

- SOCs gain popularity and will likely fly soon
  - UT699 is a controller on MISSE-7
  - Several programs interested in flying Maestro
  - SpaceMicro building Proton400k-L with Freescale P2020
- Single Event Effects Test methods unclear
  - Very complex devices
  - Multiple elements – do all need to be tested?
  - Hardware simulation of SEEs?
  - Manufacturing processes impact test methods
    - RHBD
    - Fault Tolerance
    - Multicore

Structure of SOC SEE Guideline

- Covers key areas of test planning, development, and performance:
  - Determining the type of radiation testing needed or possible
  - Development of hardware, software, and test procedures
  - Performance of testing and analysis of data
- Provides relevant examples
  - Freescale P2020 & P5020, Boeing Maestro ITC, Aeroflex UT699
- Provides specific recommendations for various elements of SEE testing of SOCs.

Focus Areas for Guideline

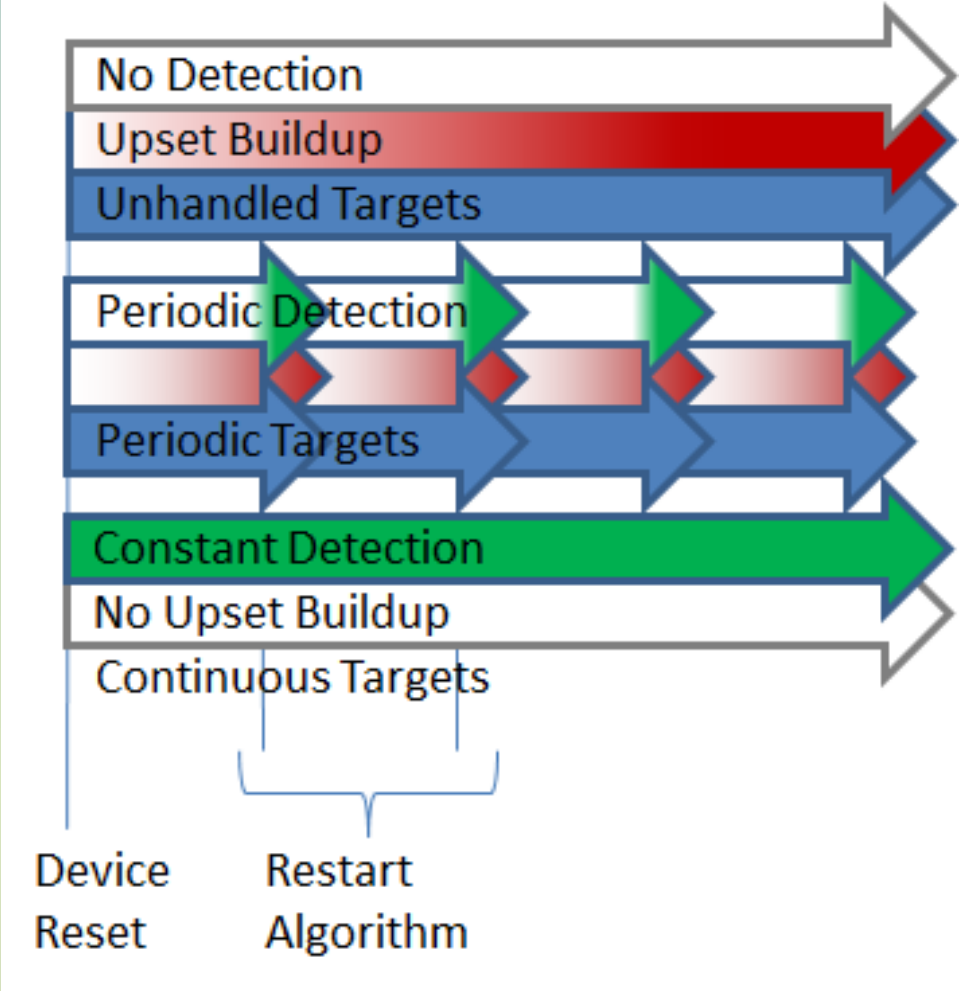
- Collaboration with Manufacturers and Users
- On-Chip Peripheral Approach/Prioritization
- Fault Tolerant Device Test Approaches
- RHBD Device Challenges to Test Development
- Multicore Device Unique Challenges
- General Test Methods
- Collecting Results from Sample Testing

Needed Radiation Data

- Details to Consider:
  - Mission environment – see standard guidelines and mission specifications – generally may need proton and heavy ion data
  - SOC details (e.g. RHBD construction)
  - Program usage of the SOC
  - Tool that will be used for rate calculations – Creme …
- SOC Details
  - Mechanical and thermal information – may impose range requirement
  - Trade study between custom hardware and inexpensive evaluation boards is recommended
  - Modern device feature size may warrant proton direct ionization testing
- Program usage
  - General testing may not be explicit enough for the user
  - But user must provide actual flight usage (unlikely till after launch)

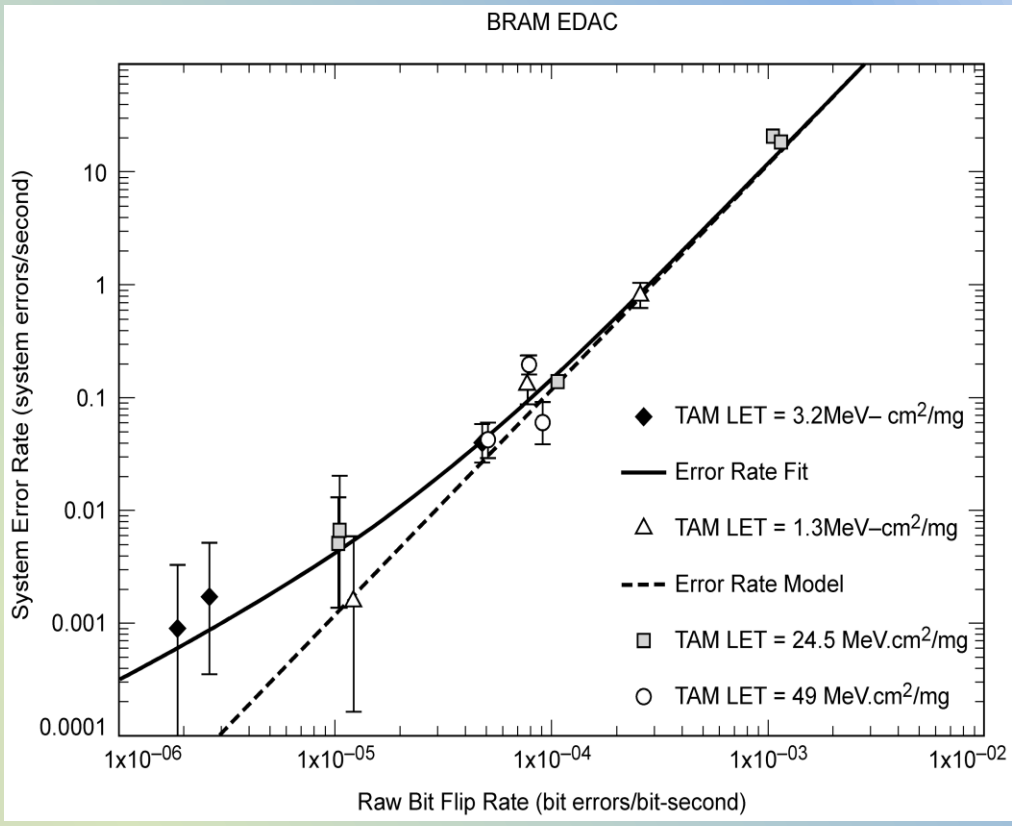
Test Algorithm Time Models

- Unhandled targets build upsets during exposure.
- Periodic targets build upsets during an integration phase
- Constant detection



Key Data to Collect

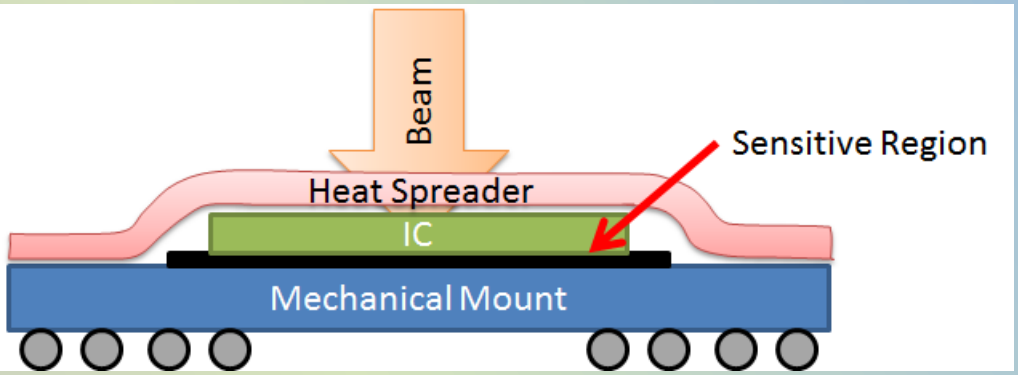
- DUT Preparation
  - Hardware modifications
  - Parameters of operation (V, T, I, f)
- # of observed events
  - Description of event
  - Details of code or test equipment that enables detection (machine-description if possible)
  - Details of event – algorithm dependence, throughput, FT/EDAC, etc
- # of incident particles
  - Species, energy/LET, angle of incidence
  - Structure of beam delivery (constant, Poisson, pulsed)



True FT protected element error rate follows dashed line. Real structure may have non-FT component leading to flattening.

Test Preparation

- Determination of appropriate test facility
  - Summarized: IUCF, UCD, Triumpf, TAMU, BNL, UCB, UCL, RADEF, NSRL
- Establish package materials and determine depackaging…



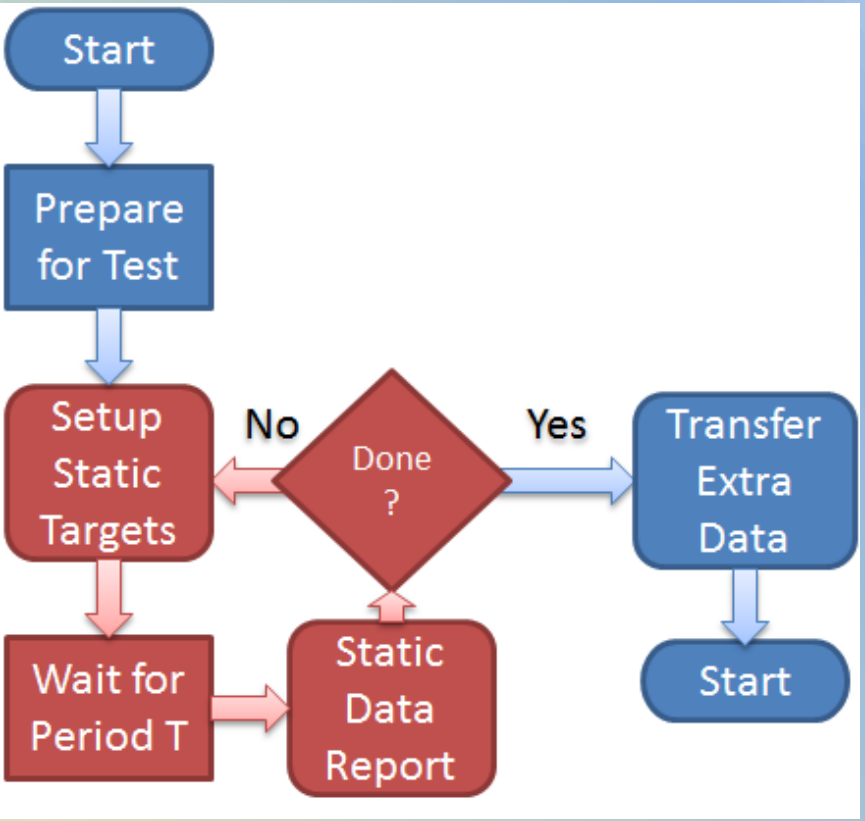
- Selection of DUT board – custom vs. inexpensive manufacturer evaluation board?
  - 10's of k vs. 0.5-4k
  - Note that lower-end evaluation boards may be sufficient (~0.5k)
  - Might be able to rework mfr board with socket

Keys to Test Algorithms - Structure

- Manufacturer equipment can perform SEE detection
  - Relatively easy to use
  - Limited ability to exercise the DUT
  - Difficult to automate
- Custom Algorithms
  - Recommend Assembly Language
    - Does not hide machine behavior or make assumptions about programming model (for example, C assumes a subroutine call structure and variable storage model)
    - Can make it difficult to debug, and may limit complexity of test algorithms

Standard Static Soak Test

- Test algorithms are generally based on repeated sub-tests that may report on each loop iteration…
- Test algorithms should periodically report results to enable immediate detection of loss of operation.
- Periodic reporting enables use of partial runs.



Keys to Test Algorithms - Anomalies

- It is common to want to explore test anomalies because they may be “rare SEEs”. Avoid this want as it leads to much lost time.
- Rely on beam and event statistics. If it doesn’t repeat, put a limit on it and move on. If it does repeat, figure out what it is if possible.
  - If you can’t figure out what it is, that’s ok. Report the rate, but don’t claim a mechanism.
  - Be aware you may be exploring a bug in your code, or even upsets in support or test equipment.
- When possible, use debugging tools to examine these as they enable fast and detailed examination

Preparation for the Test Trip

- Where possible, test SEE detection code by planting simulated SEEs (or using debugging tool to alter things)
- Consider use of laser facilities for fault injection and checkout (but be wary that laser can inject non-beam-type faults)
- Coordinate with test facility regarding requirements for thermal management
- Perform standard DUT preparation and equipment checkout for use at SEE test facilities
  - Long cables (power and/or communication), noise
  - Enable remote power-cycling and manipulation of key buttons (such as power and reset)

Testing – Determine Sensitivity

- Because of the nature of SOC testing many different types of events can influence reported data.
- This necessitates determining the sensitivity of the test system for each event type investigated.
  - Determine the system response that establishes a “floor” to detection – for example if the DUT “crashes” (fails to continue proper execution) this generally means that any more rare event is undetectable.
- Sensitivity can be improved by either improving robustness of the test system or by targeting a given event type.

Testing – Avoiding Redundancy

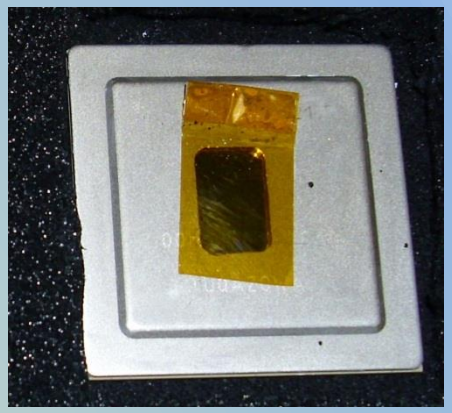
- Many modern SOCs are constructed from SRAM or similar elements that are easily tested.
- But these elements are known to be weak to SEE, so they are protected with FT or EDAC. Thus characterization is largely unnecessary.
- It is more important to verify to FT, EDAC or other protection works.
- And it is important to avoid measuring sensitivity of these elements many times (though they can be good for establishing a baseline and test-to-test consistency).

Testing – Recording the Test

- When possible, collect the following:
  - Facility test record
  - Test engineer test log
  - Power supply log files
  - All I/O logs between the DUT and support equipment (including key transfers to enable verification of commands)
  - SEE records stored during test and reported after the test completes

Example from Freescale

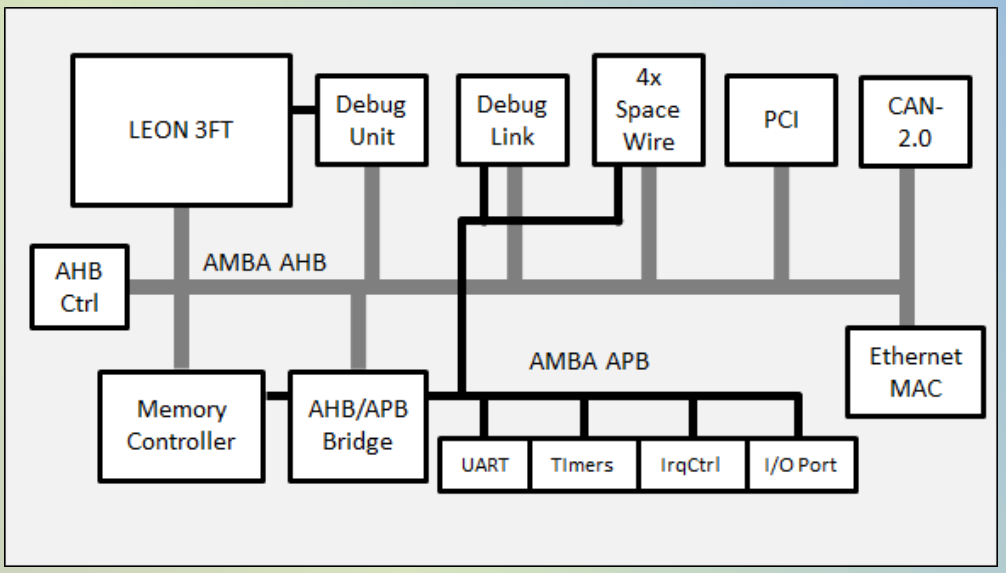
- The P2020 and P5020 processors provided the best example of commercial/COTS type devices with the relevant testing issues.
  - Thermal issues and depackaging dominate
  - Cannot reliably test at many angles
- Debugging tools are well-developed
  - Codewarrior tool set is useful for directly observing what is wrong with the processor (provided it can successfully perform).



P5020 – with hole to expose e5500 cores

P2020 with hole in heat spreader

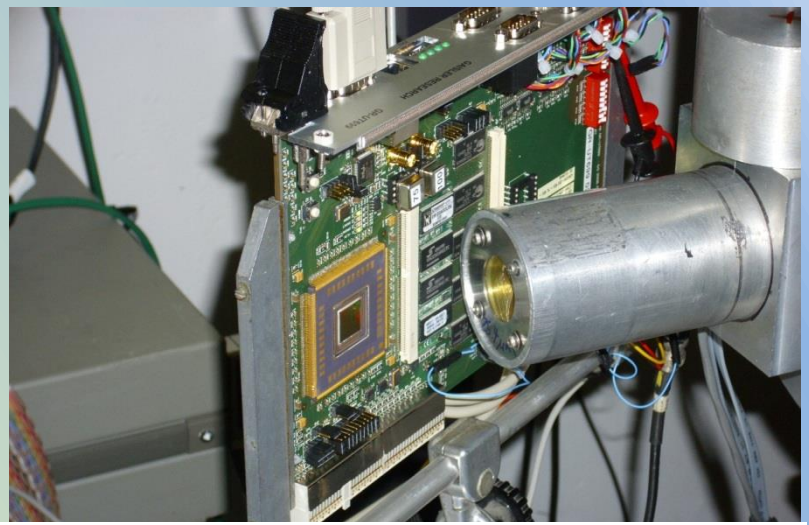
Example from UT699 - 1

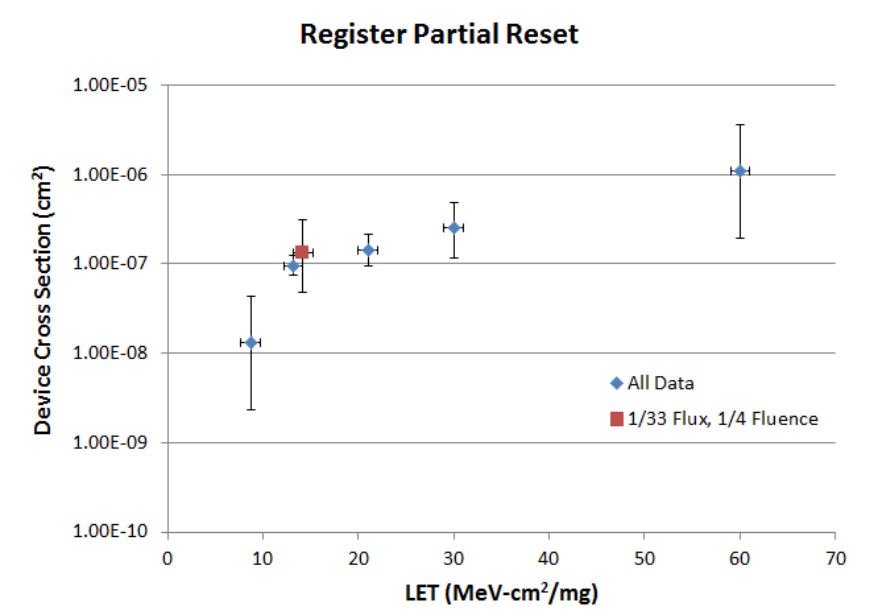


- Sparc V8 Leon 3FT core – desired by many space users
- RHBD with built-in FT
- Many different types of components
- Study includes “register partial reset” and Spacewire examination

Testing/Results

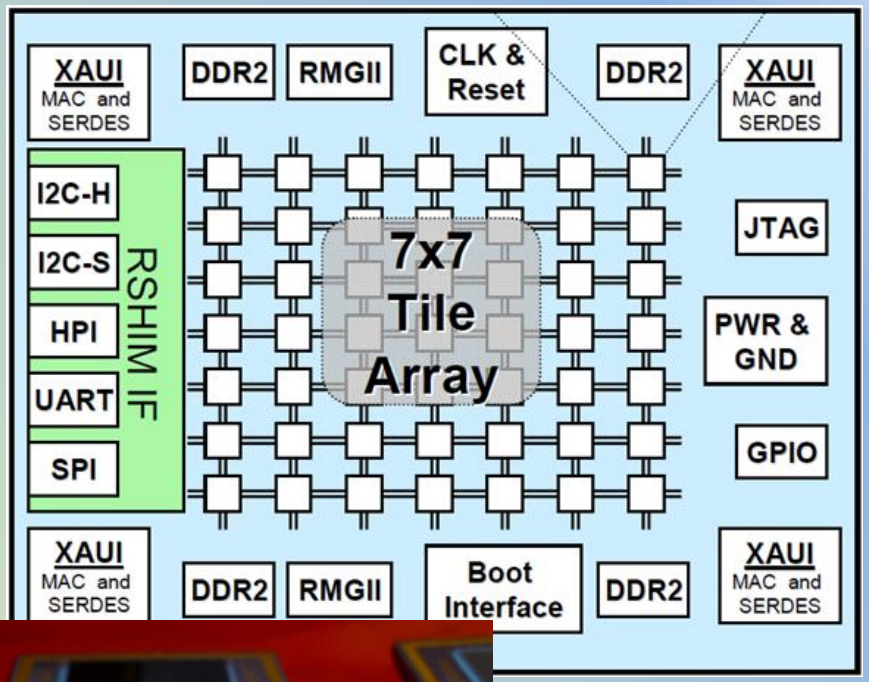
- Manufacturer involvement ensured successful DUT preparation and understanding of events
- Explored different types of flux and fluence dependence to lock-in on the register partial reset
- Spacewire results showed effective sensitivity was not sufficient, Spacewire is robust…





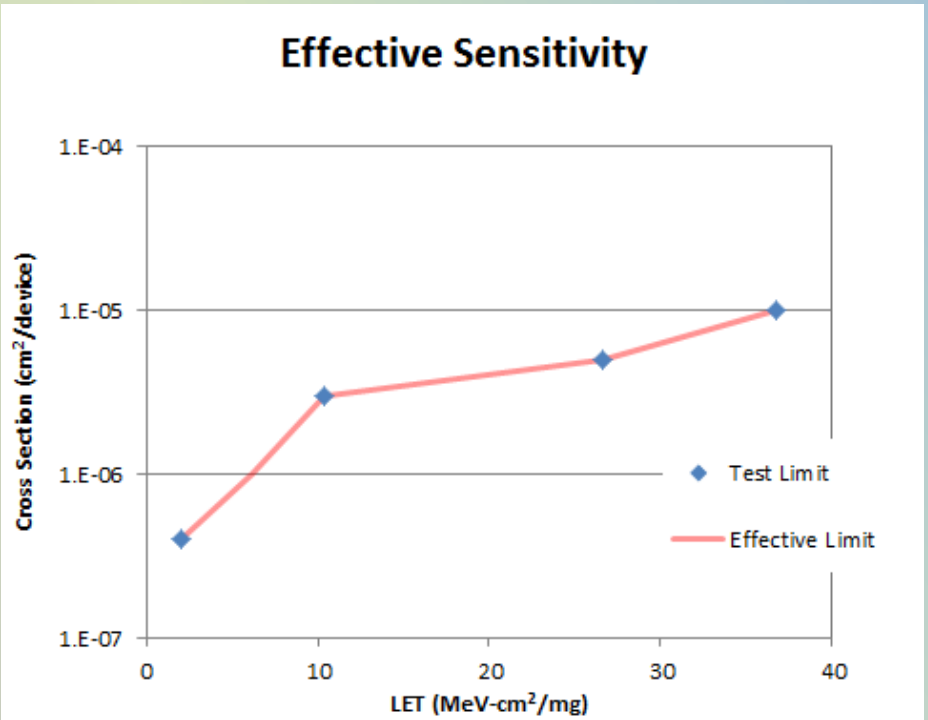
Example from Boeing Maestro ITC

- 49-core tiled microprocessor
- RHBD and FT construction with SRAMs expected to upset readily (but they are EDAC protected)
- Highlights need for custom DUT preparation.



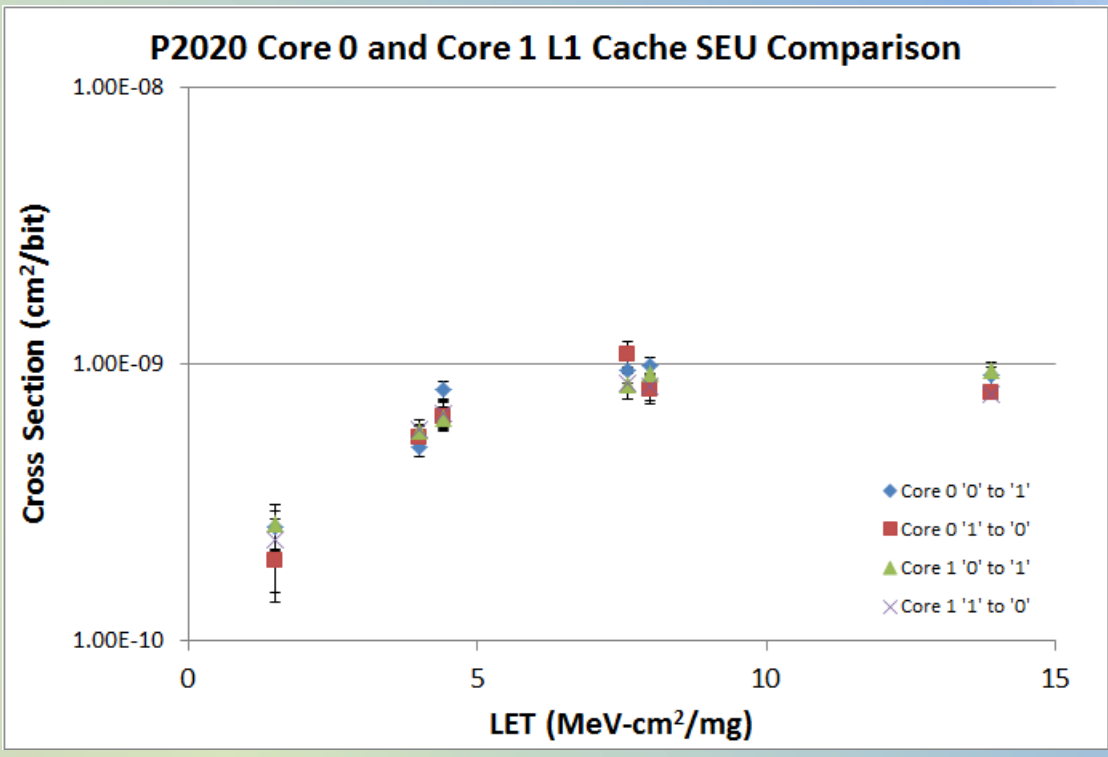
Test Efforts/Results

- Highlight of need to understand beam delivery and algorithm structure (algorithm behavior on multiple tiles potentially confusing).
- Effective sensitivity is a key player because the caches are very sensitive to SEEs and relatively high fluence is required to activate non-cache upsets. But in the meantime the caches are experiencing many SEUs.



P2020 Provides Dual Core Environment…

- Multicore testing will gain in importance…
- P2020 provides cache-coherency for communicating data between processors
- Testing with both cores active shows cache sensitivity is essentially the same.



Other Relevant Study

- Frequency Dependence is potentially important and is explored, but recent results indicate the sensitivity is a low priority in commercial devices where frequency is high – mostly because the sensitivity is already very high..
- Cross section vs. Feature Size has stayed within a factor of 10 from 180 to 45nm for Freescale/Motorola devices.
- Voltage is important but largely untestable on modern devices due to lack of control of point-of-load converters on demonstration boards.
- TID enhancement of SEE – it is recommended to be prepared for this, but it is unclear how to give general guidance on this case.
- Angular study of RHBD cells (such as DICE latches) is recommended but it is also pointed out that high angles of incidence may be infeasible.

Conclusion

- SOC SEE Test Guideline released by NEPP soon (end of May)
- SOCs require consideration of many different aspects of SEE testing and test development
- Guideline provides specific recommendations for conducting SEE testing
- Examples of testing Freescale e500/e5500 devices, Boeing's Maestro ITC, and Aeroflex UT699 provided

- **Feedback welcomed! (steven.m.guertin@jpl.nasa.gov)**