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Space Administration

Jet Propulsion Laboratory
California Institute of Technology
Pasadena, California

Advanced CMOS Technology Scaling – Can Space Parts Catch Up?

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Space parts ~0.01% of Total IC Market

Autumn 2012	Amounts in US\$M			
	2011	2012	2013	2014
Americas	55,197	52,771	54,727	57,345
Europe	37,391	33,401	33,695	35,198
Japan	42,903	42,018	43,424	45,354
Asia Pacific	164,030	161,745	171,207	180,870
Total World - \$M	299,521	289,936	303,053	318,766
Discrete Semiconductors	21,387	19,303	20,351	21,540
Optoelectronics	23,092	25,989	27,775	29,477
Sensors	7,970	7,934	8,518	9,132
Integrated Circuits	247,073	236,710	246,410	258,618
Analog	42,338	39,683	41,120	43,521
Micro	65,204	60,316	62,075	64,959
Logic	78,782	80,543	85,461	90,375
Memory	60,749	56,167	57,754	59,764
Total Products - \$M	299,521	289,936	303,053	318,766



Semiconductor manufacturers

1H12 Top 20 Semiconductor Sales Leaders (\$M, Including Foundries)

1H12 Rank	2011 Rank	Company	Headquarters	2011 Tot Semi	1Q12 Tot Semi	2Q12 Tot Semi	1H12 Tot Semi	2Q12/1Q12 % Change
1	1	Intel	U.S.	49,697	11,874	12,422	24,296	5%
2	2	Samsung	South Korea	33,483	7,067	7,484	14,551	6%
3	3	TSMC*	Taiwan	14,600	3,568	4,337	7,905	22%
4	4	TI	U.S.	12,900	2,934	3,135	6,069	7%
5	7	Qualcomm**	U.S.	9,828	3,059	2,869	5,928	-6%
6	5	Toshiba	Japan	12,745	3,232	2,382	5,614	-26%
7	6	Renesas	Japan	10,653	2,344	2,099	4,443	-10%
8	9	SK Hynix	South Korea	9,403	2,115	2,291	4,406	8%
9	10	Micron	U.S.	8,571	2,102	2,210	4,312	5%
10	8	ST	Europe	9,631	1,997	2,126	4,123	6%
11	11	Broadcom**	U.S.	7,160	1,770	1,917	3,687	8%
12	13	Sony	Japan	6,093	1,514	1,560	3,074	3%
13	12	AMD**	U.S.	6,568	1,585	1,413	2,998	-11%
14	14	Infineon	Europe	5,599	1,292	1,272	2,564	-2%
15	15	Fujitsu	Japan	4,430	1,216	931	2,147	-23%
16	21	GlobalFoundries*	U.S.	3,480	945	1,115	2,060	18%
17	17	NXP	Europe	4,147	969	1,084	2,053	12%
18	18	Nvidia**	U.S.	3,939	935	990	1,925	6%
19	16	Freescale	U.S.	4,391	912	988	1,900	8%
20	20	UMC*	Taiwan	3,760	834	970	1,804	16%
Top 20 Total				221,078	52,264	53,595	105,859	3%

*Foundry

**Fabless

Source: IC Insights' Strategic Reviews Database

“62% of TSMC’s wafer revenue from 65nm processes and below”



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Space vs. Modern COTS

Space

**Standards Based
Screening**

**Post manufacture
testing**

Vendor certification

Acceptance sampling

COTS

**Design rule and tool
improvement**

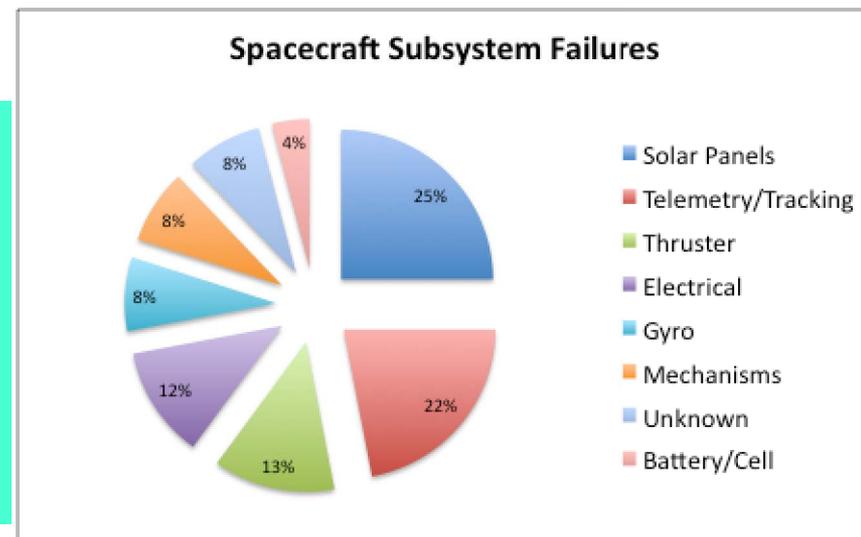
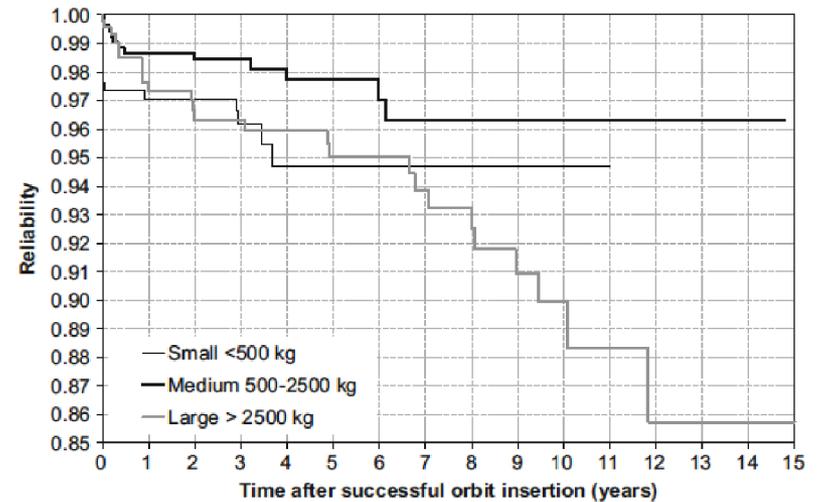
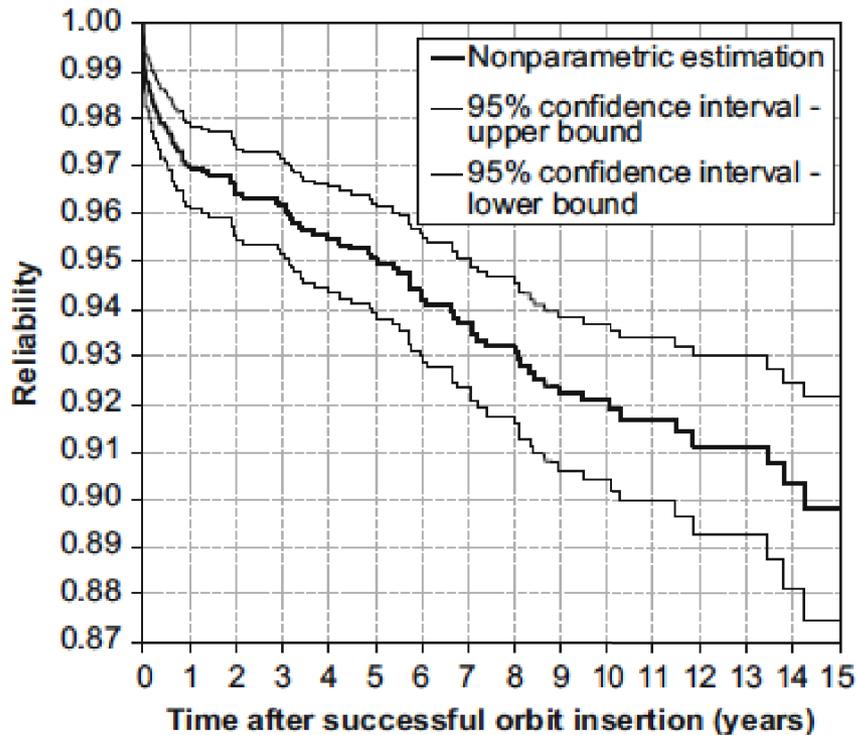
**Continuous Defect
reduction**

Vendor audit

Six sigma quality



1,584 Satellites – 1990 to 2008



- Failure => results in retirement of the satellite
- Reliability continues to decrease
 - there is no 'flat' region and the reliability never gets better
- Large satellites (>2,500 kg) have the worst reliability



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Significant Spacecraft Anomalies

Mars Reconnaissance Orbiter

	Date	Anomaly	Cause
A	27-Sep-05	Memory SEUs	Redundancy scheme incompatible with unexpectedly rad-soft parts
B	2-Nov-05	Star Tracker Long Acquisition Time	Star tracker sensitivity lower than expected
C	3-Jan-06	Computer Warm Reset	FSW bug
D	26-May-06	Transponder Ka Exciter Failure	Premature part failure
E	31-May-06	Safe Mode Entry	Command sequence design error
F	26-Jul-06	Safe Mode Entry	Ground command error
G	16-Aug-06	RF Transfer Switch Failure	Most likely: RF breakdown due to flaking plating
H	14-Mar-07	Computer Side Swap (A->B)	Computer memory controller lockup
I	18-Jul-07	Payload Interface Task Suspension	FSW not fully bulletproofed to noise-induced interface data corruption.
J	27-Sep-07	HiRISE Safing with SSR Full	Defect in software/sequence interface with instrument
K	7-Nov-07	Appendage Contact With Spacecraft	Incorrect parameter combination due to incomplete requirements
L	29-Nov-07	Safe Mode Entry	Ground command error
M	14-Mar-08	Computer Side Swap (B->A)	Computer memory controller lockup
N	27-May-08	Electra UHF Anomalies	FSW bugs

Space grade parts still represent ~20% failures
There is requirement for additional improvement

Bayer 2009



CMOS Scaling

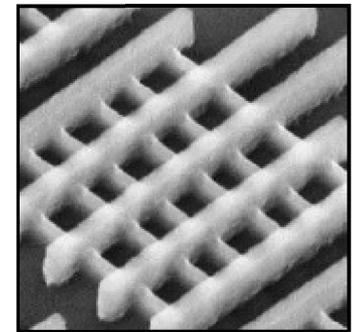
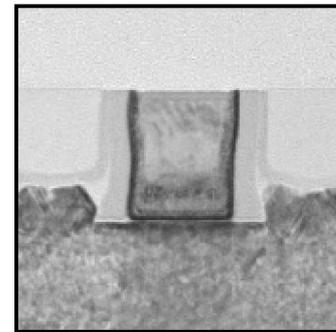
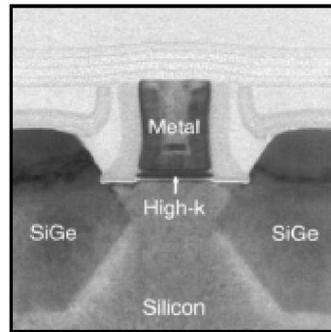
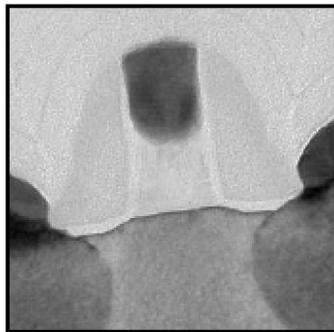
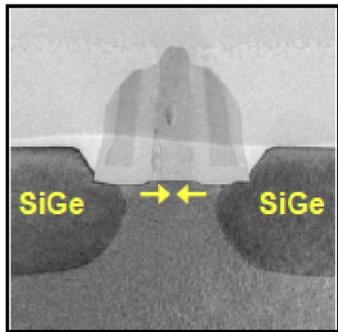
2003
90 nm

2005
65 nm

2007
45 nm

2009
32 nm

2011
22 nm



Invented
SiGe
Strained Silicon

2nd Gen.
SiGe
Strained Silicon

Invented
Gate-Last
High-k
Metal Gate

2nd Gen.
Gate-Last
High-k
Metal Gate

First to
Implement
Tri-Gate

Strained Silicon

High-k Metal Gate

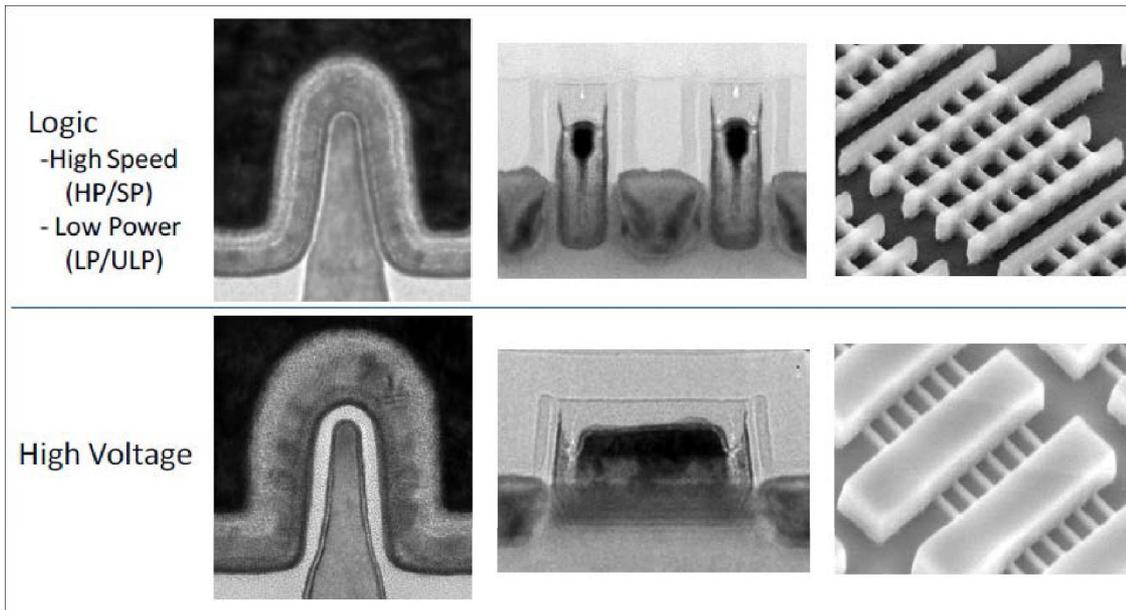
Tri-Gate





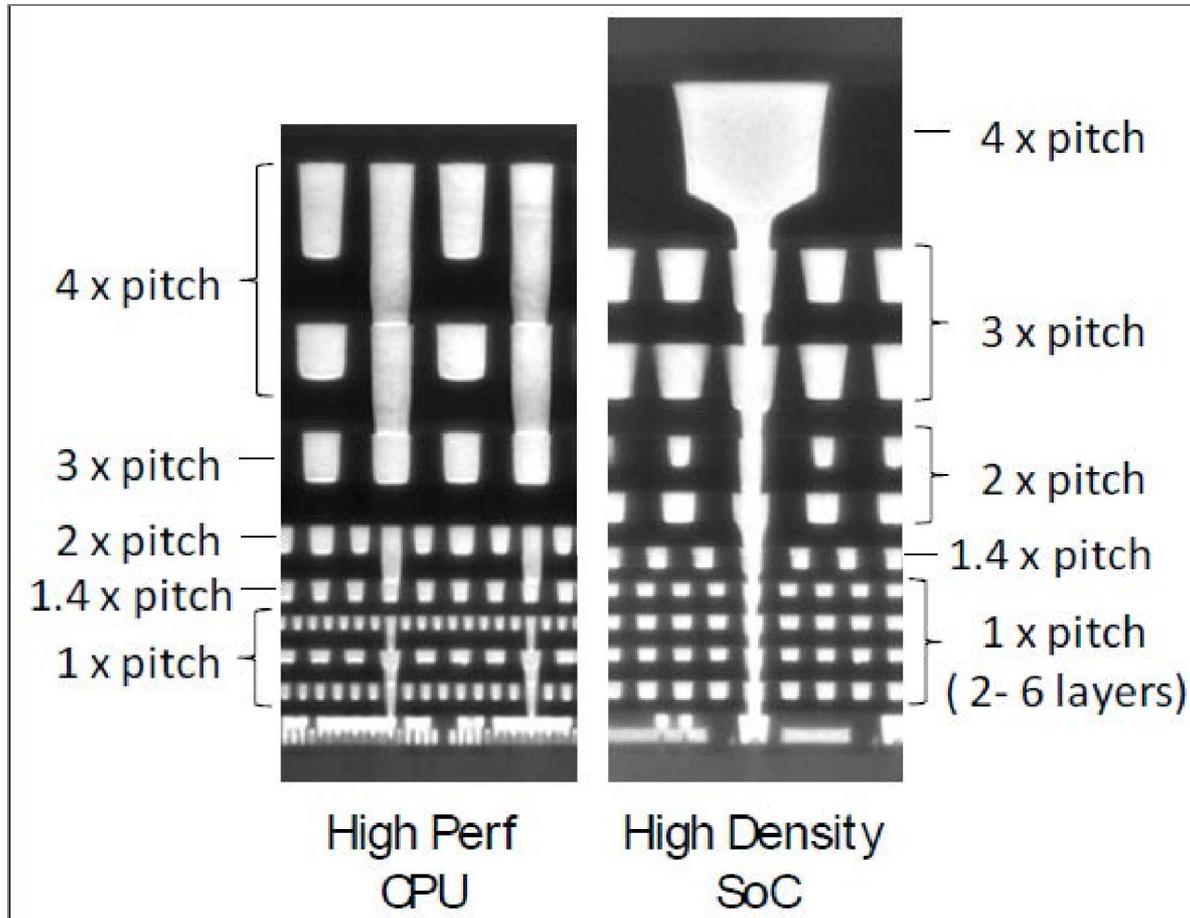
One node = more than one option

Transistor Type	High Speed Logic		Low Power Logic		High Voltage		
	Options	High Performance (HP)	Standard Perf./ Power (SP)	Low Power (LP)	Ultra Low Power (ULP)	1.8 V	3.3 V
Vdd (Volt)		0.75 / 1	0.75 / 1	0.75 / 1	0.75/1.2	1.5/1.8/3.3	3.3 / >5
Gate Pitch (nm)		90	90	90	108	min. 180	min. 450
Lgate (nm)		30	34	34	40	min. 80	min. 280
N/PMOS Idsat/loff (mA/um)		1.08/ 0.91 @ 0.75 V, 100 nA/um	0.71 / 0.59 @ 0.75 V, 1 nA/um	0.41 / 0.37 @ 0.75 V, 30 pA/um	0.35 / 0.33 @ 0.75 V, 15 pA/um	0.92 / 0.8 @ 1.8 V, 10 pA/um	1.0 / 0.85 @ 3.3 V, 10 pA/um





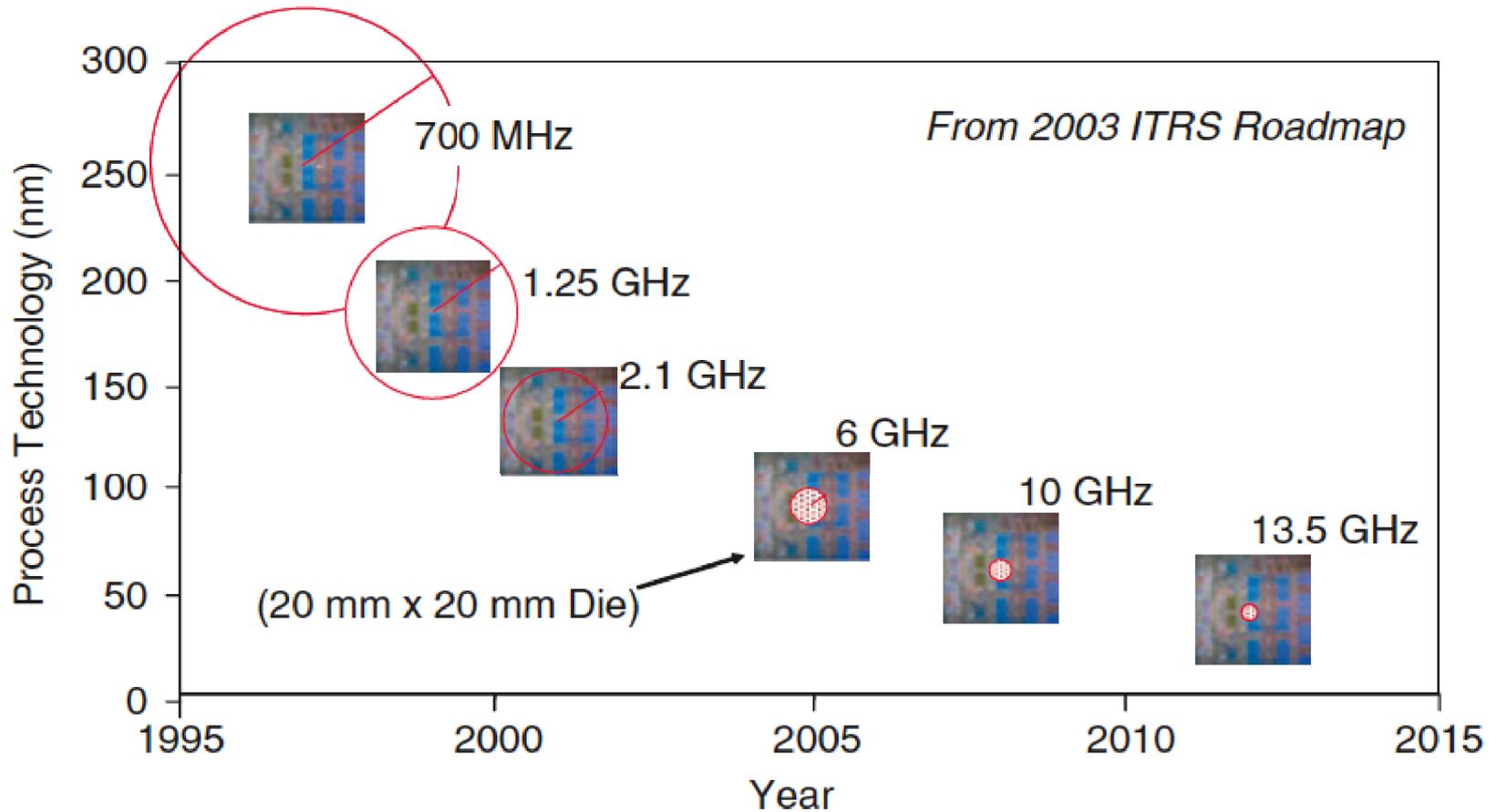
CPU vs. SoC process



SoC process has more interconnect layers with different design rules => additional reliability concerns



Speed vs. Distance Packaging Must Evolve

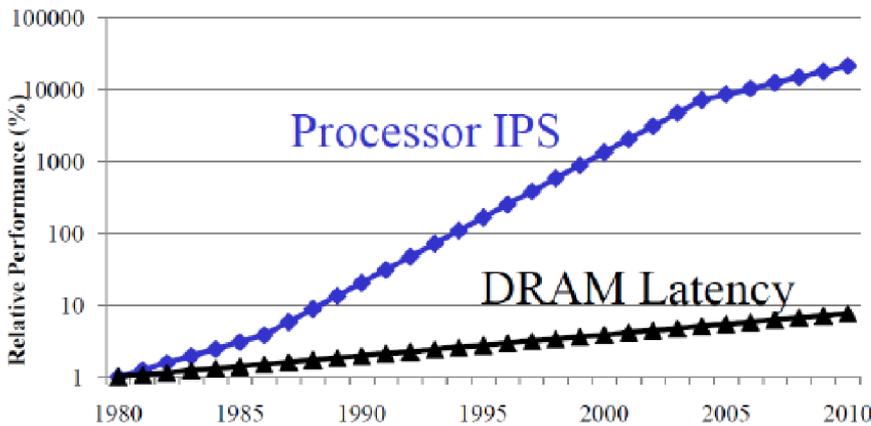
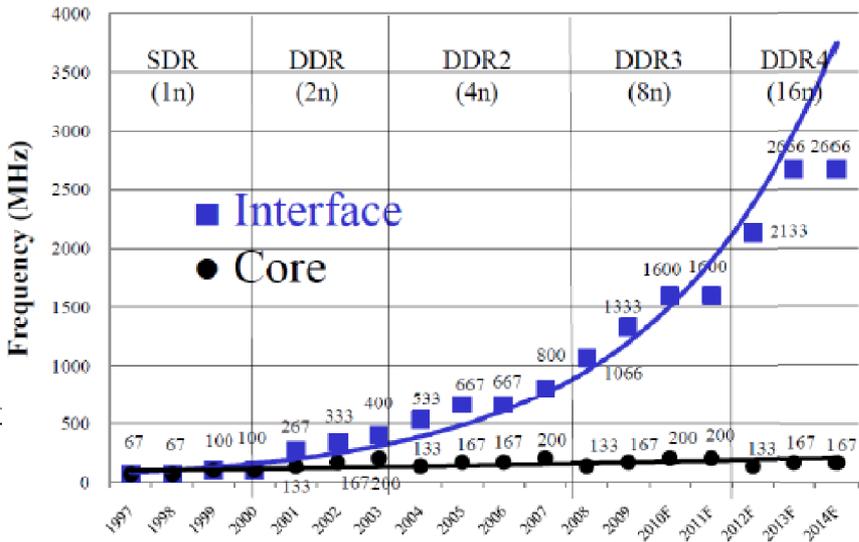
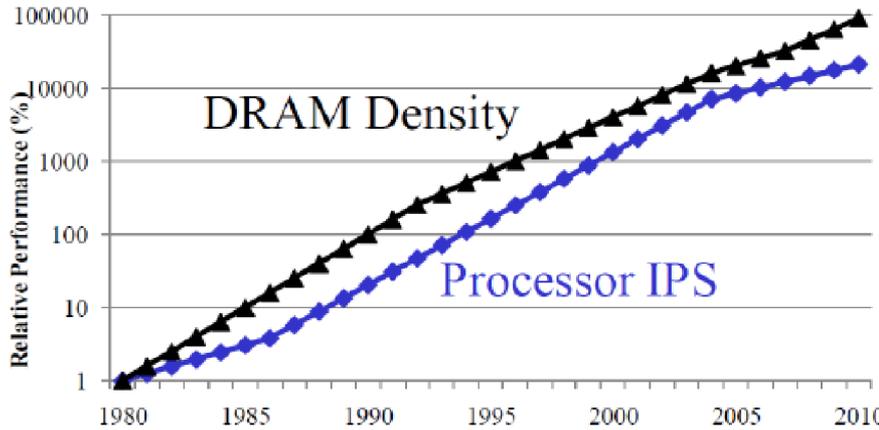


**Radius of circle = distance single
clock cycle can effectively propagate**



Need for Wide I/O

Mobile: Case for Wide I/O

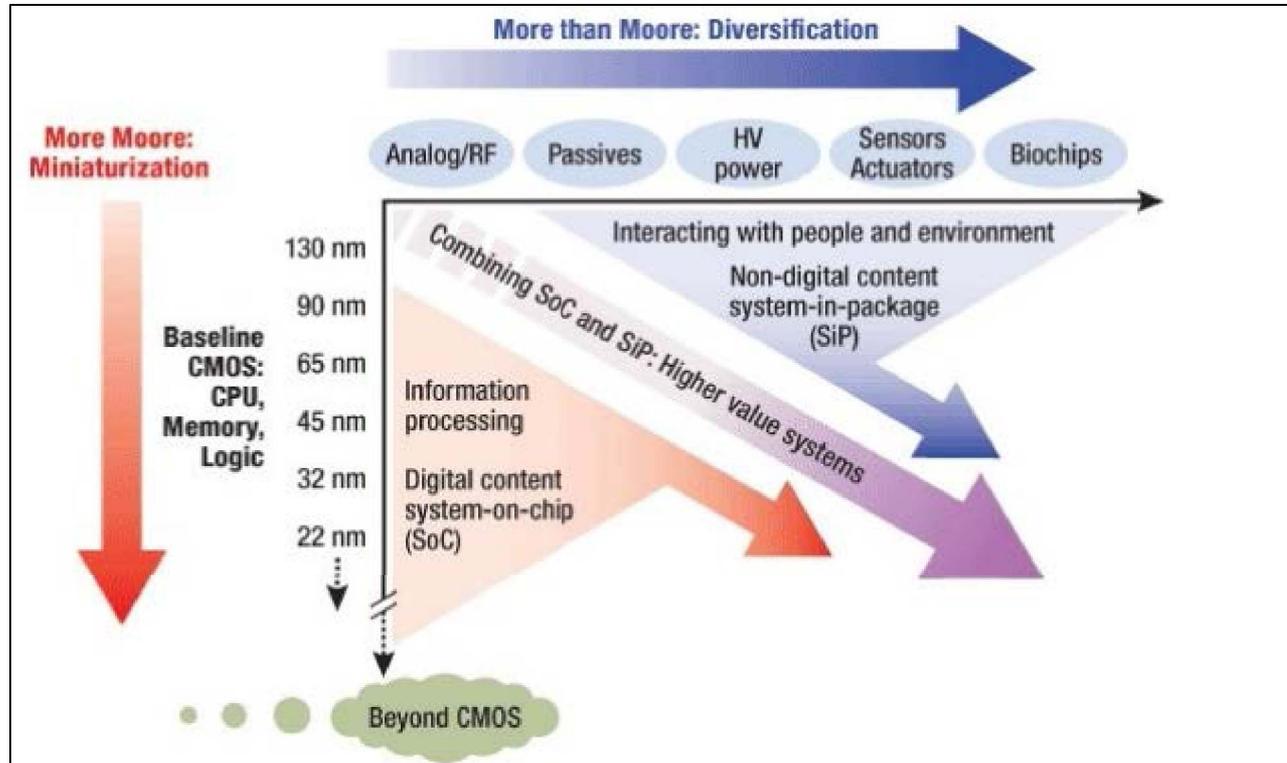


Source: SUN, Micron, Rambus

- The DRAM device density has scaled well with microprocessor performance, but DRAM performance has not kept up
- One way to solve the problem is through wide I/O



“More than Moore” Scaling – Diversification vs. Miniaturization



- Moore's Law addresses increases in digital content in devices
- Higher value, complex systems also must address analog, RF, passives, power, and sensors
- New packaging technologies are the means to accomplish this

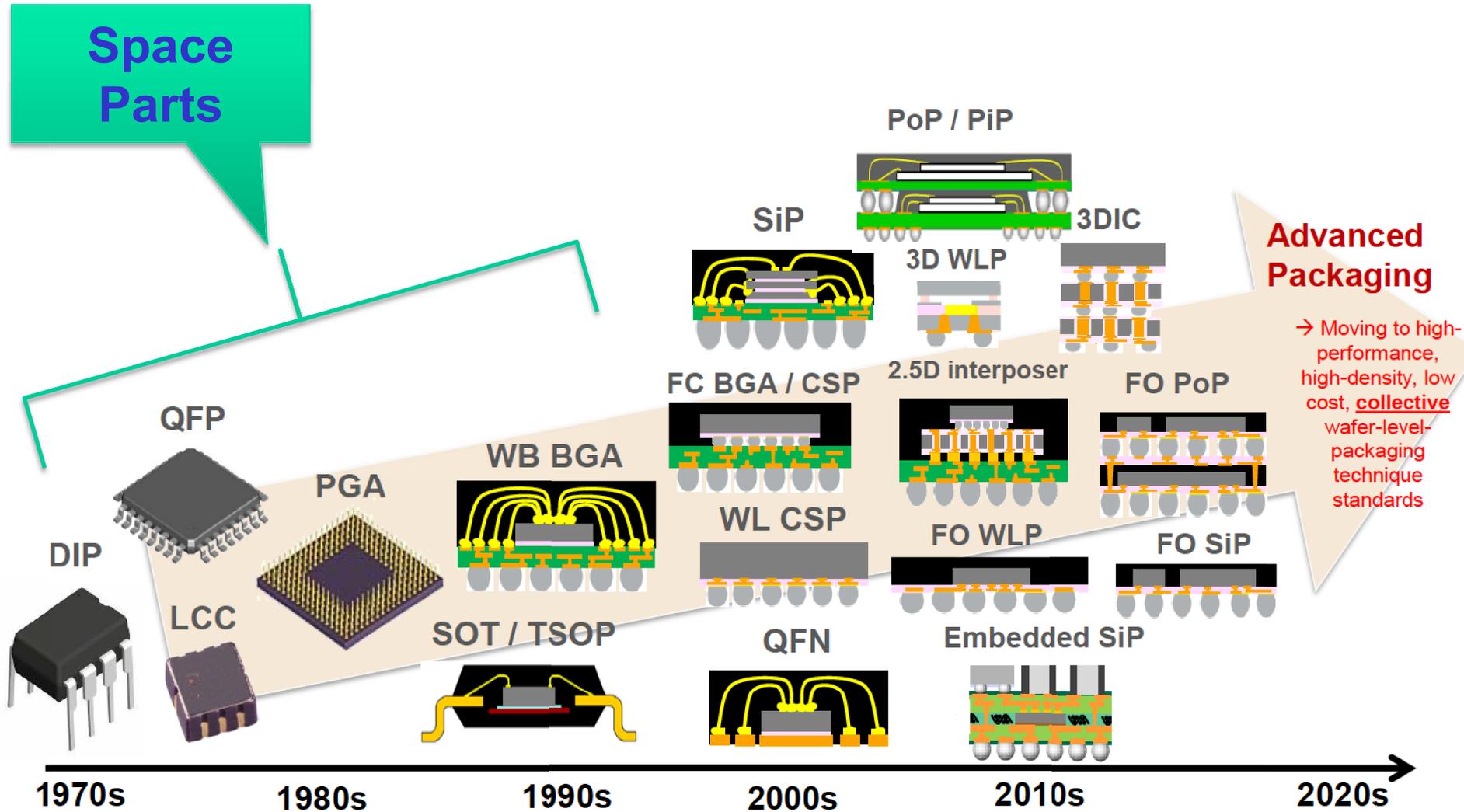


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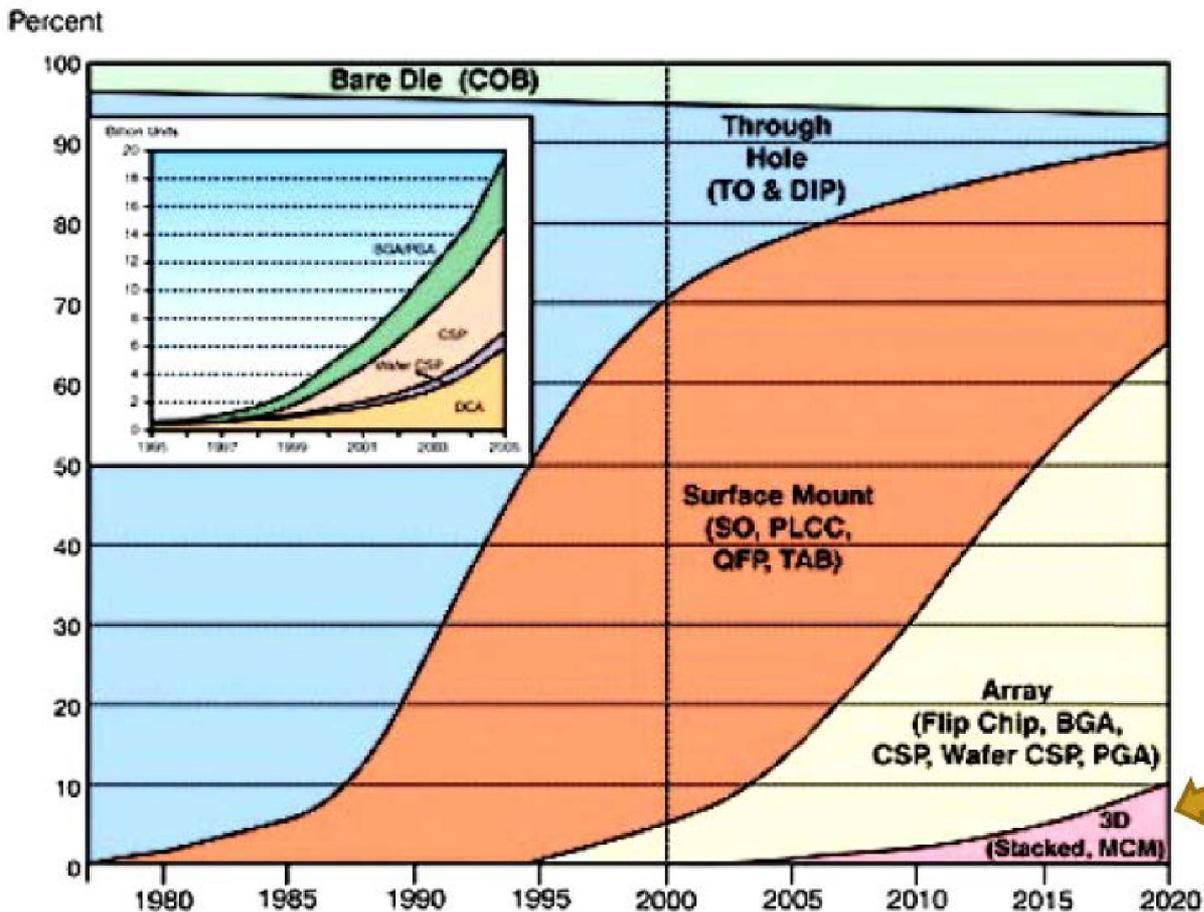
Evolution of chip/IC packaging

Space Parts





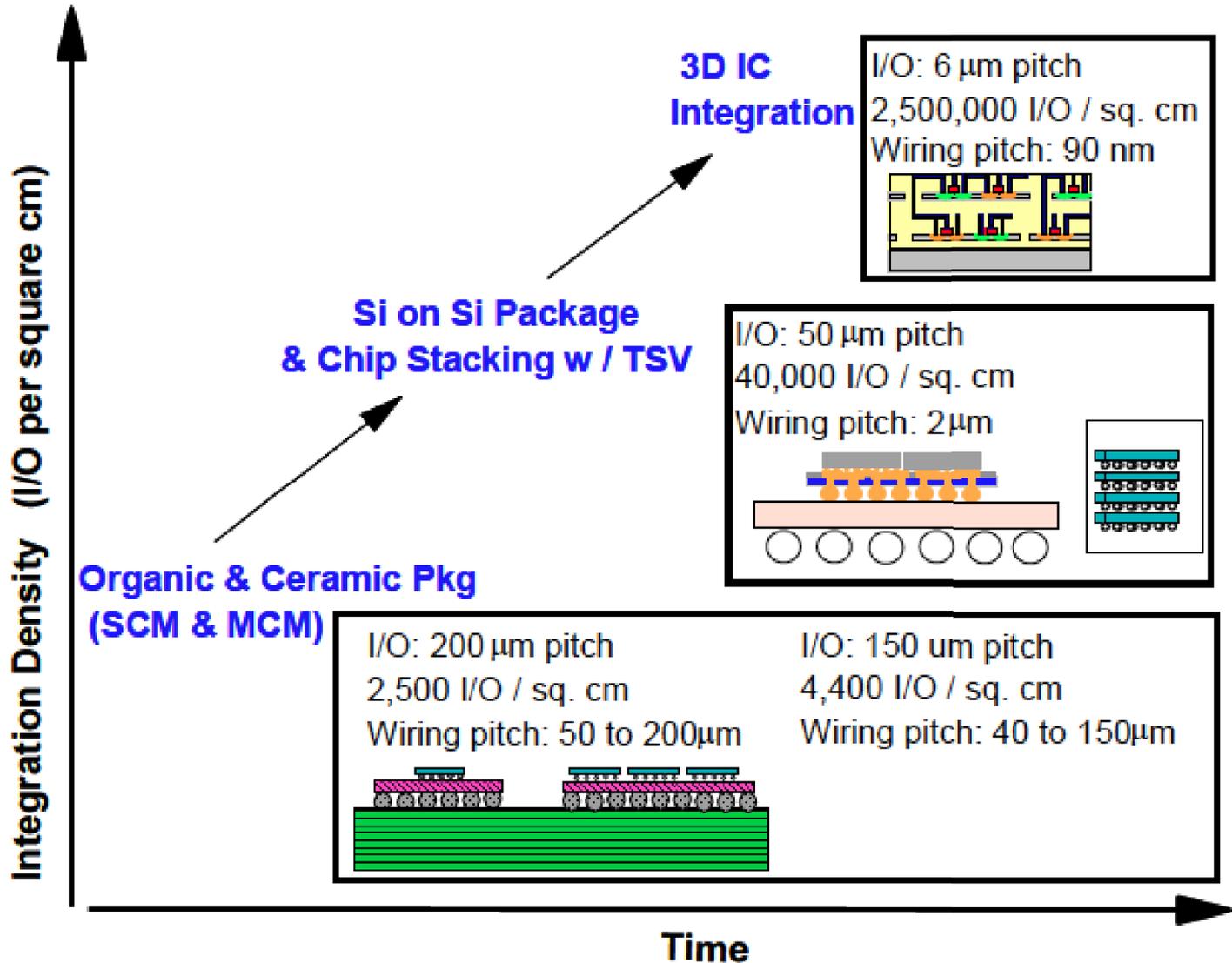
Overall packaging trends



Space must continue to adopt new packing technologies or risk obsolescence/unavailability



3D Package Integration – High I/O count



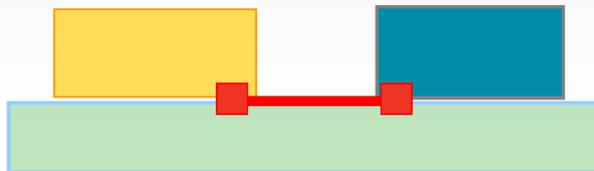
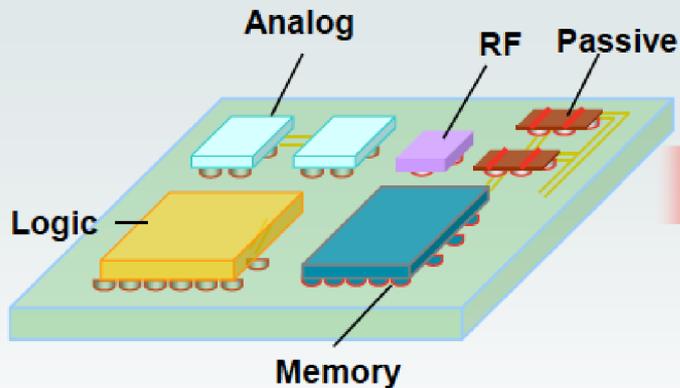


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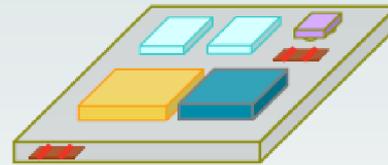
Progression of 3D Technology

Traditional MCM/PCB



Flipchip + wire bond

Silicon Interposer 2.5D



**2.5D side-by-side integration
with TSVs & silicon interposer**

Full 3D

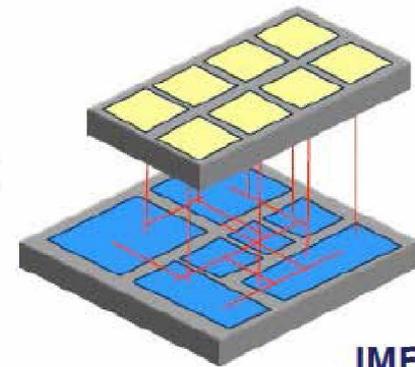
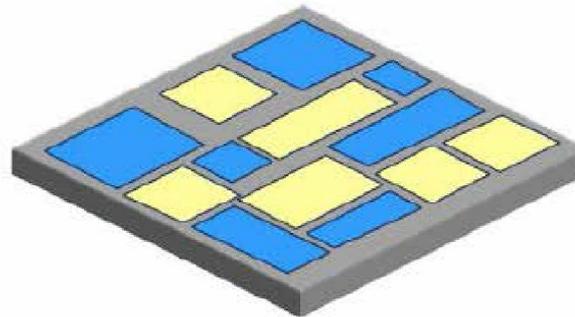
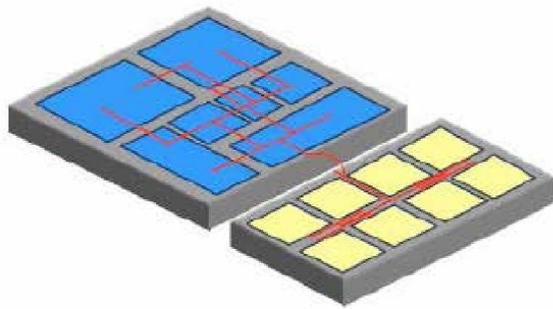


**Vertical stacking with
memory & logic**



3D vs 2D

Shorter lines = Better Performance



IMEC

2D SiP solution

- Long interchip connections between logic & memory

SOC solution

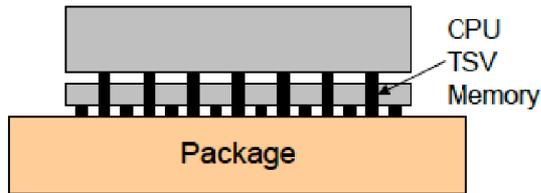
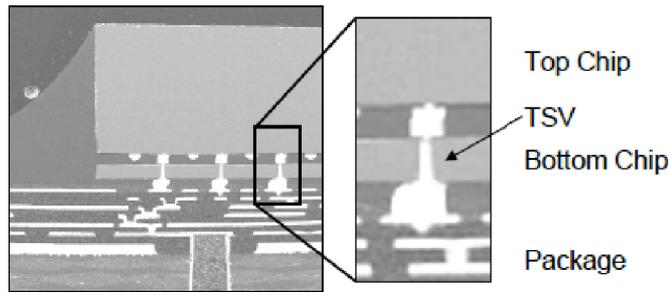
- Large die
- design, time to market, process issues

TSV stacked Si solution

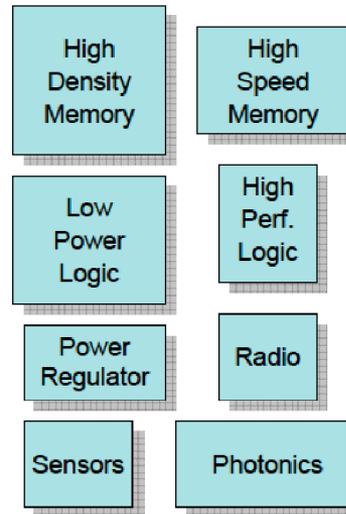
- Shortest interconnect between functions
- electricals better than SoC



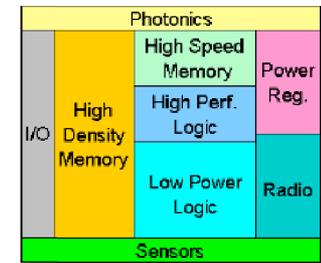
Through Silicon Vias (TSV) – Complexity that is coming quickly



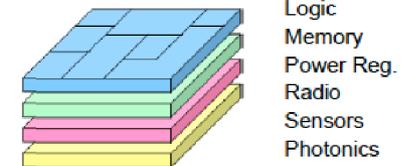
Discrete



2-D Integration (SOC)



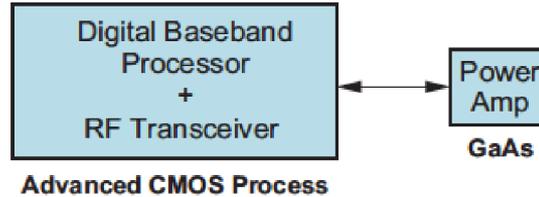
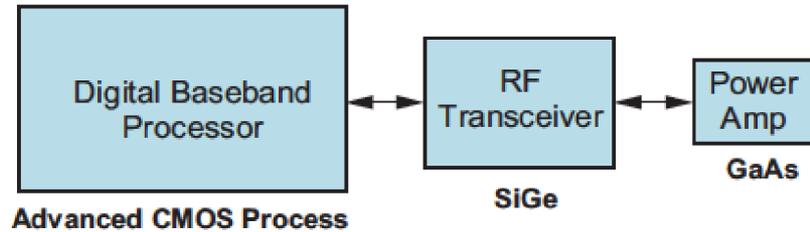
3-D Integration



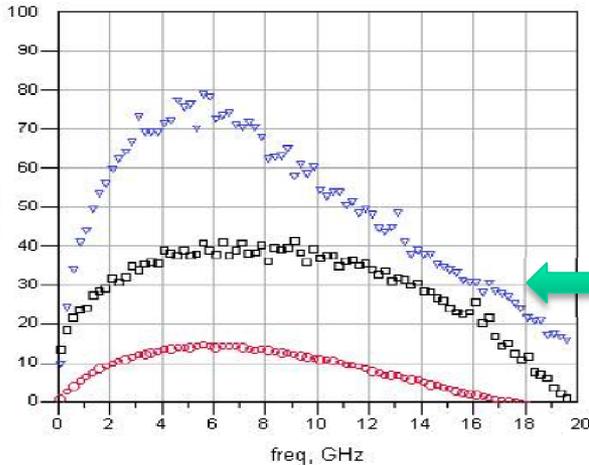
3D stacking is way to integrate together chips of dissimilar process technology that may be impractical to implement on a single piece of silicon.



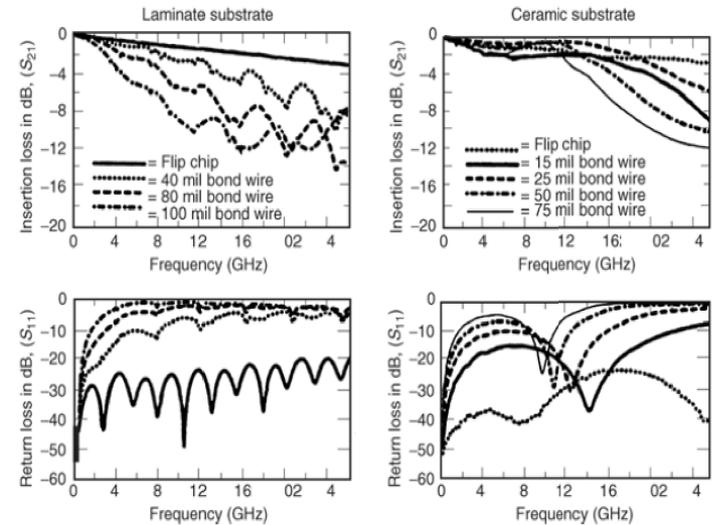
RF Benefits from Scaling



Characterization of package connections



- Inductor 'Q' factor vs frequency:
 - **Integrated**
 - **SIP**
 - **Wire bond**



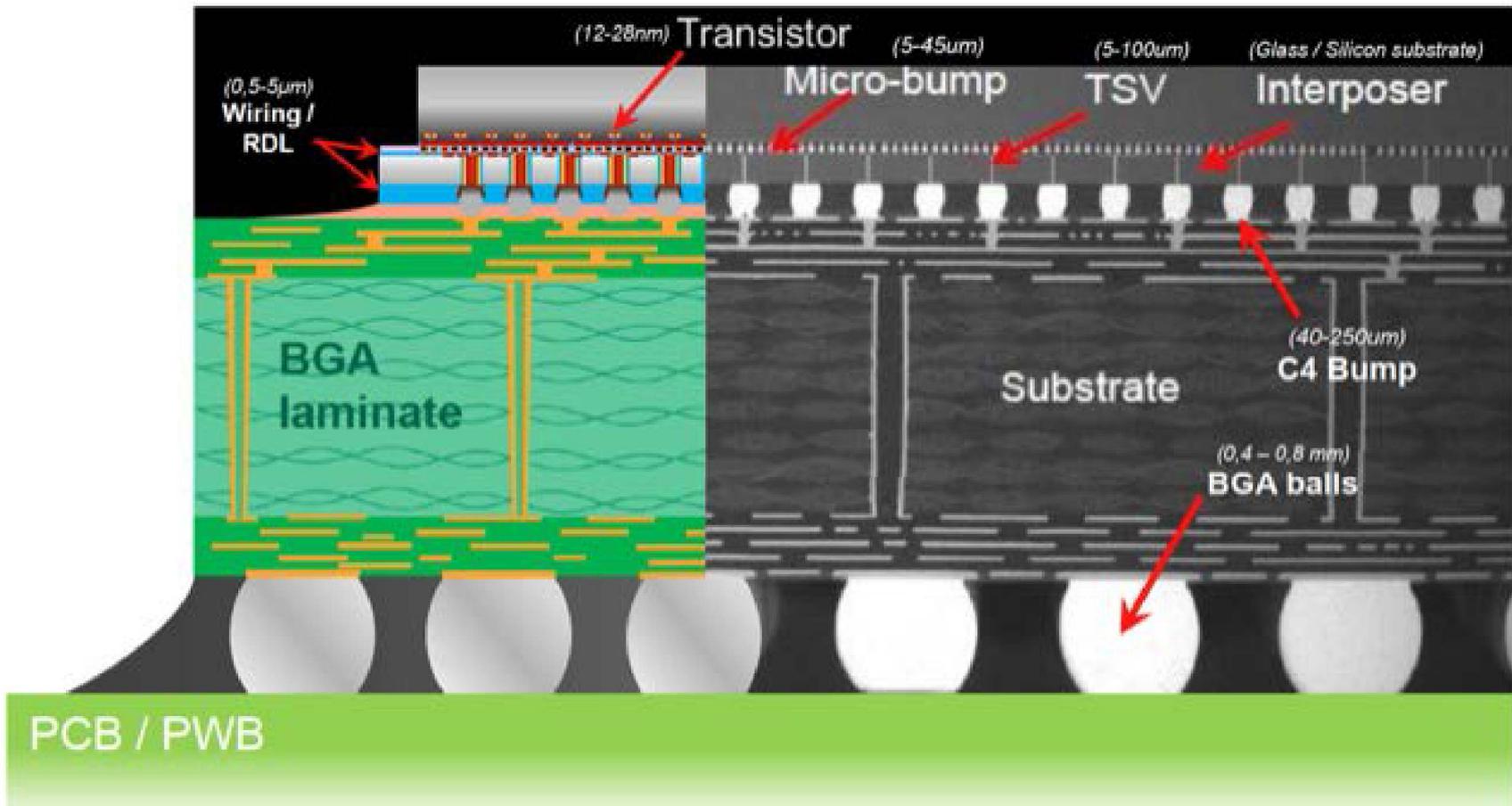
Advantage of Flip-chip



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Heterogeneous Package/Device Structures

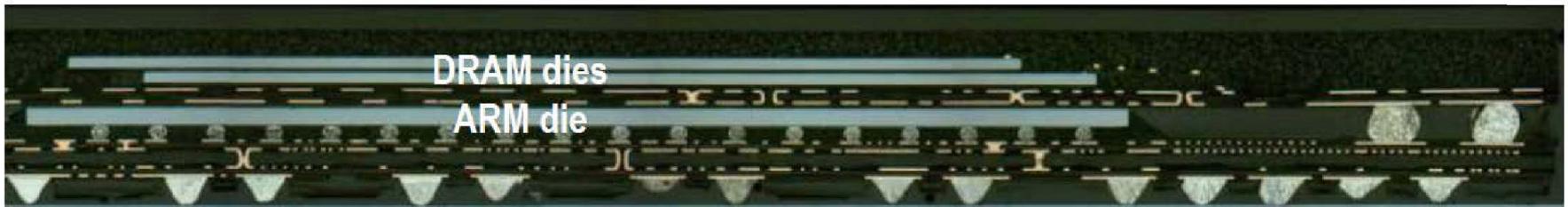
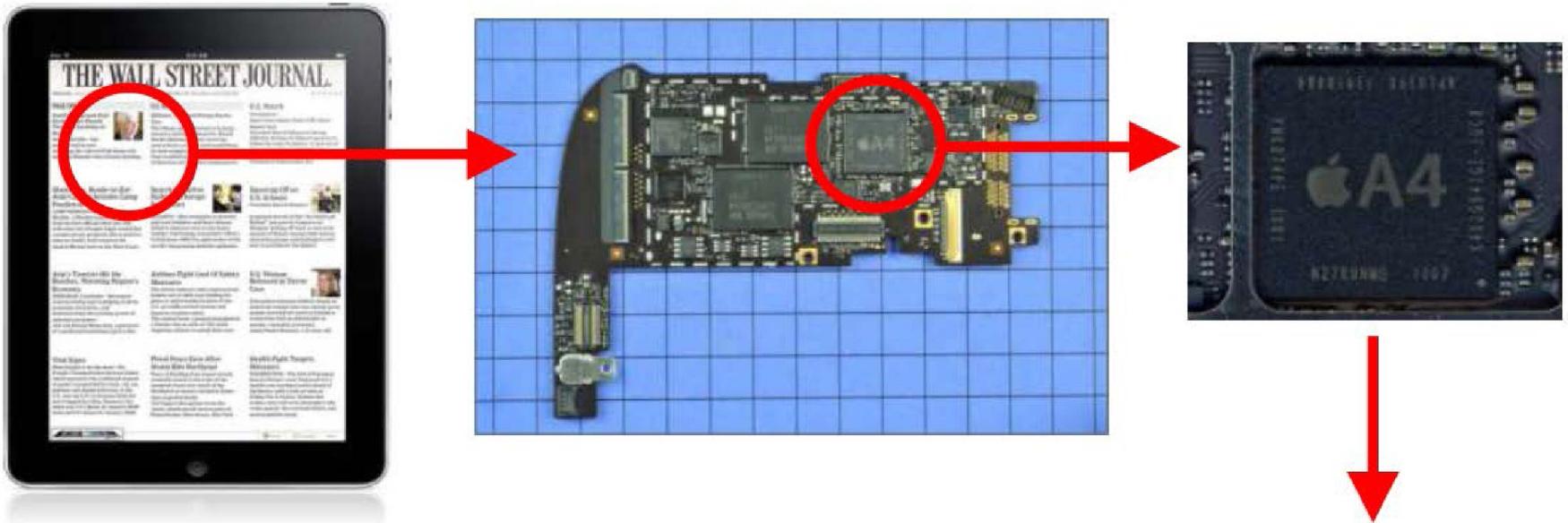




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Evolution of Device/Packaging Scaling



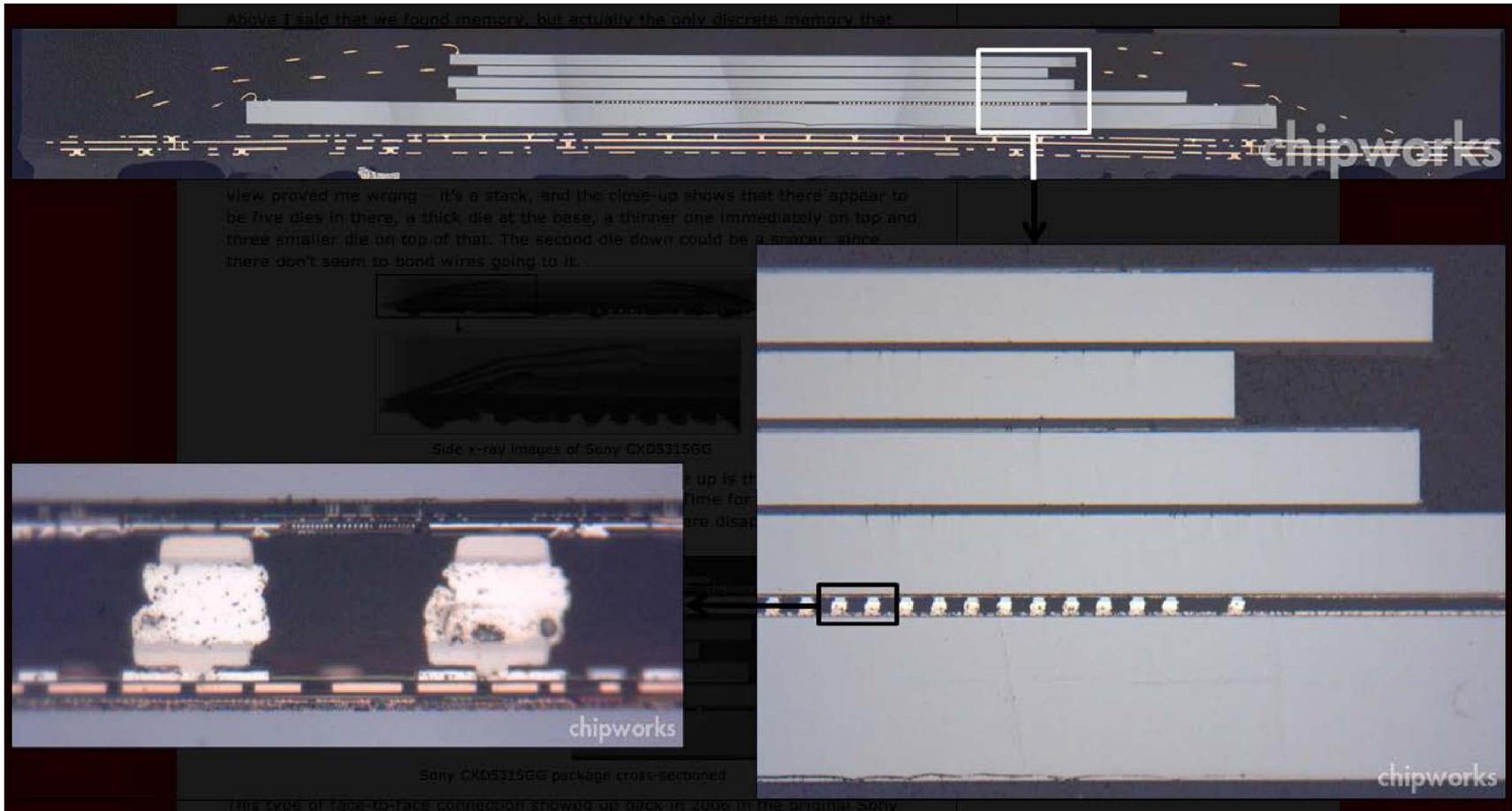
1 ARM die + 2 DRAM dies, stacked, wire-bonded (no TSVs... yet), and packaged



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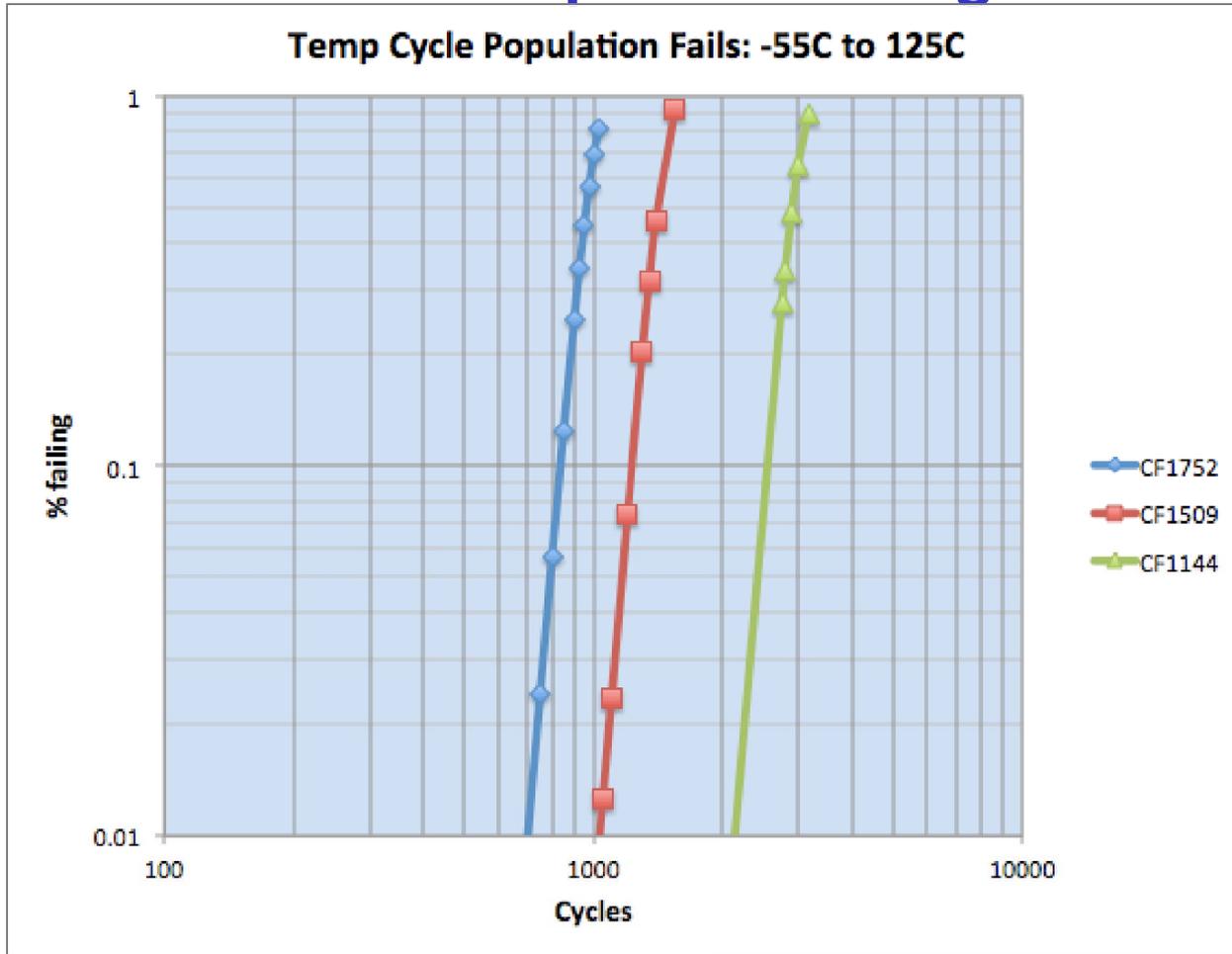
Details of Packaging



Quad core ARM 9 Cortex processor chip; face to face with it is a Samsung 1-Gb wide I/O SDRAM; and the top three dies comprise two Samsung 2-Gb mobile DDR2 SDRAMs, separated by a spacer die, and conventionally wire-bonded. The base die is $\sim 250 \mu\text{m}$ thick, and the others $\sim 100 - 120 \mu\text{m}$



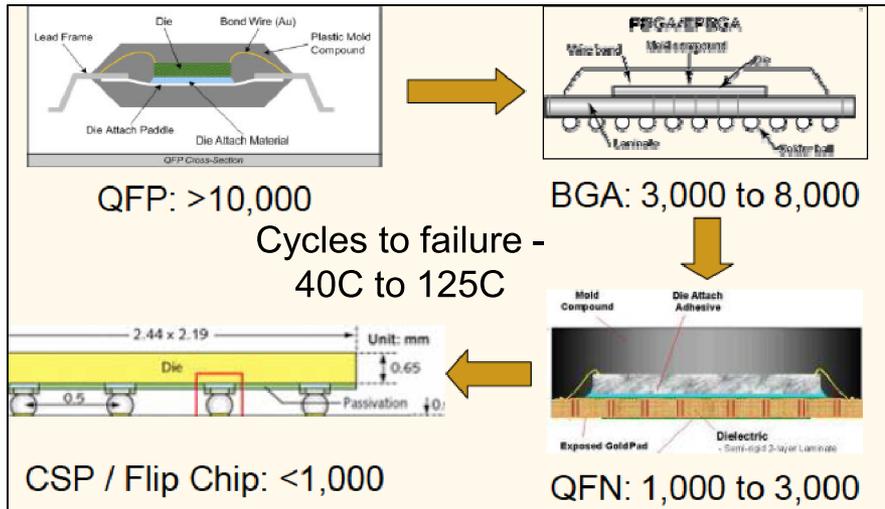
Generic Specification vs. Mission Specific testing



Bigger die and bigger packages have less capability in terms of total number of temp cycles

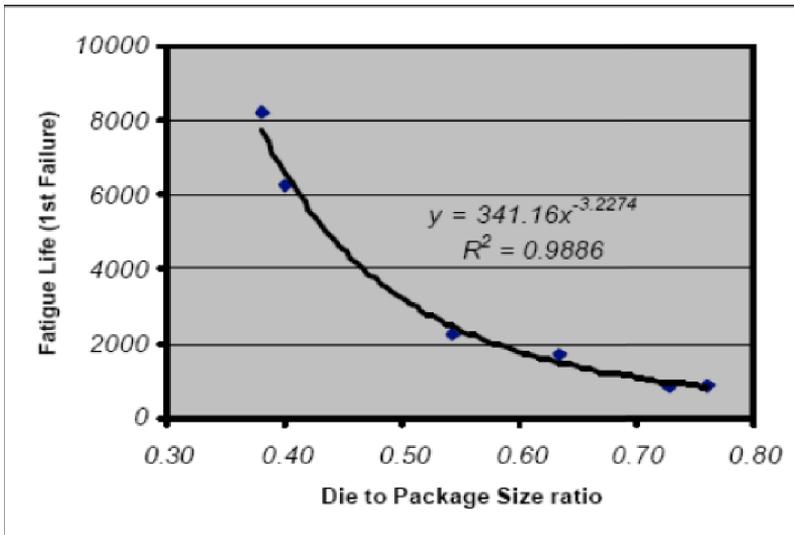


New packaging structures failures do not scale linearly



Elimination of leaded devices => Lower RC and higher package densities => Reduces # of temp cycles to failure

More silicon, less plastic => Increases mismatch in coefficient of thermal expansion (CTE)





New Qualification Issues

INTERFACE

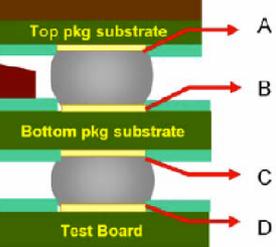


Table 1. 5 Leg BLR matrix and critical solder joint interfaces evaluated.

Leg #	Pad finish		Pad finish of bottom package		Solder ball	Additional Comment
	Top pkg (A)	Top pkg	Top side (B)	Bottom side (C)		
Leg 1	NIAu	SAC405	NIAu	NIAu	SAC3.0	
Leg 2	NIAu	SAC405	CuOSP	CuOSP	SAC3.0	
Leg 3	NIAu	SAC405	CuOSP	CuOSP	SAC3.0	Multiple reflow passes by to simulate prestack
Leg 4	NIAu	SAC405	NIAu	CuOSP	SAC3.0	
Leg 5	NIAu	SAC405	NIAu	CuOSP	LFA3	

Cumulative %

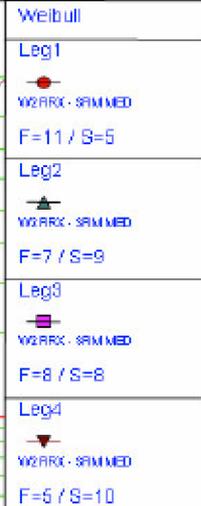
10.00
5.00
1.00

1.00

Drops to Failure

100.00

1000.00



$$\beta_1=0.65, \eta_1=4990, \rho=0.90$$

- Different vendors = different processes.
- Many materials interfaces = new physics of failure
- COTS success criteria ≠ Space criteria



BGA Materials Interactions

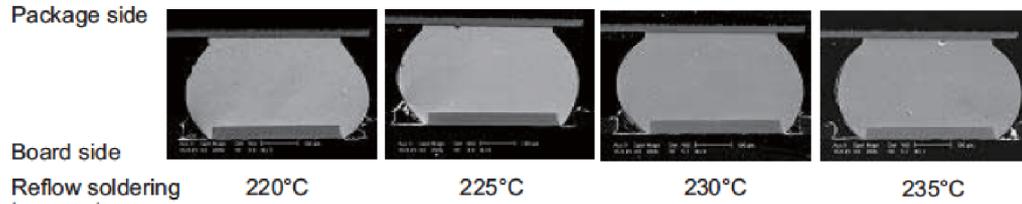


Figure 6.1 Sn-3Ag-0.5Cu Balls/Sn-3Ag-0.5Cu Paste

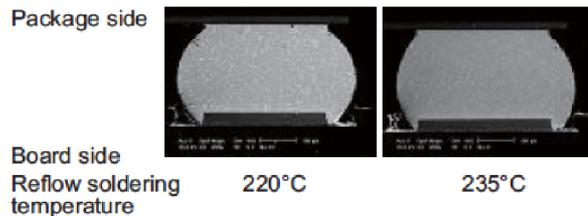
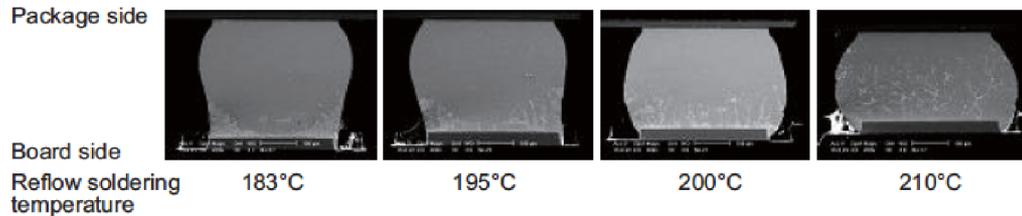
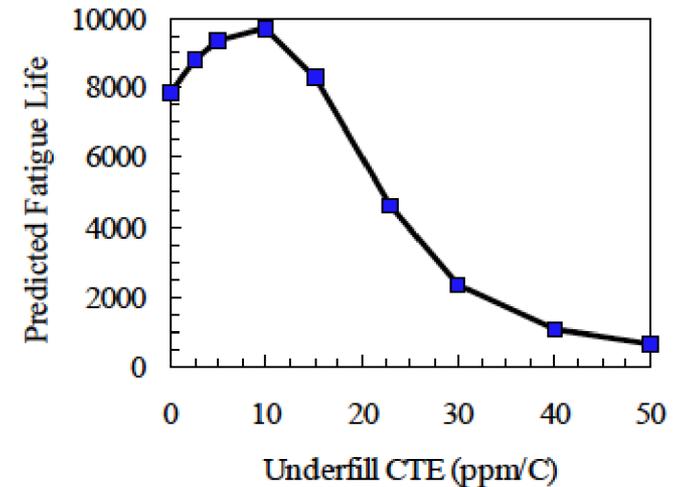


Figure 6.2 Sn-3Ag-0.5Cu Balls/Sn-37Pb Paste

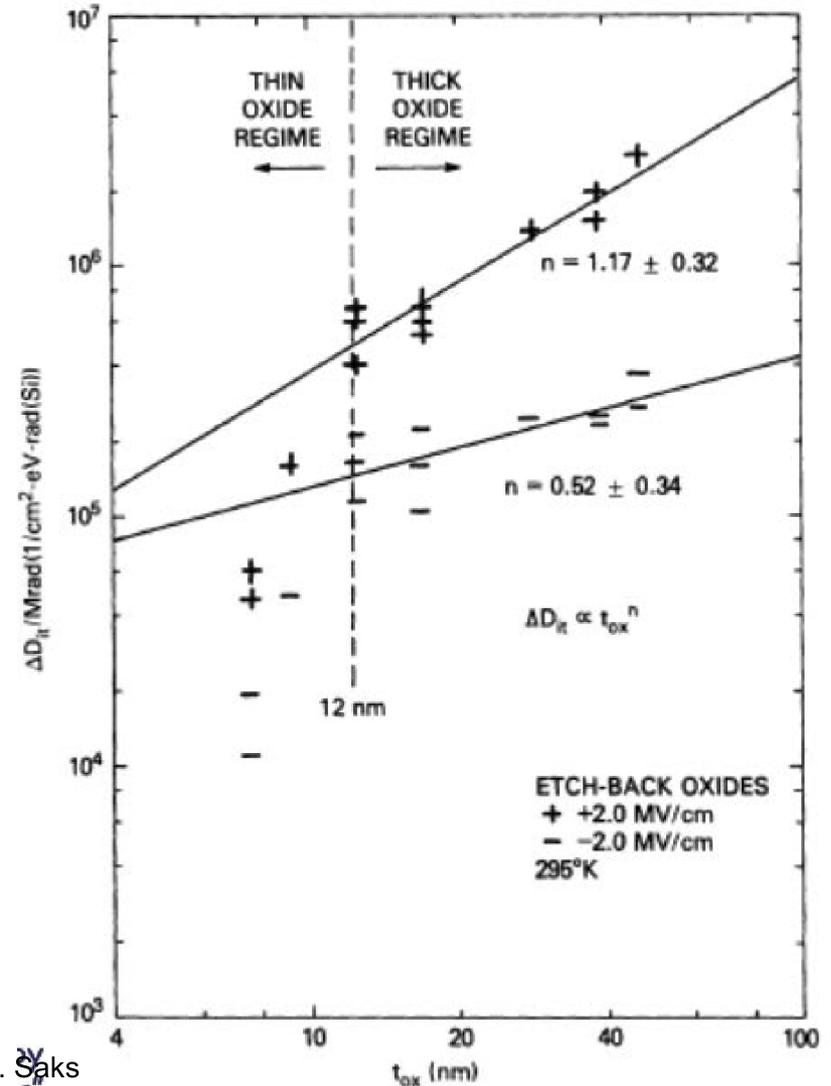
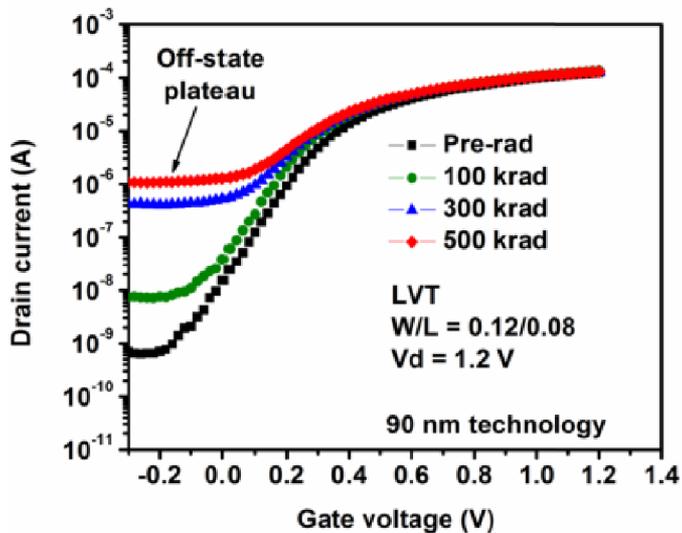
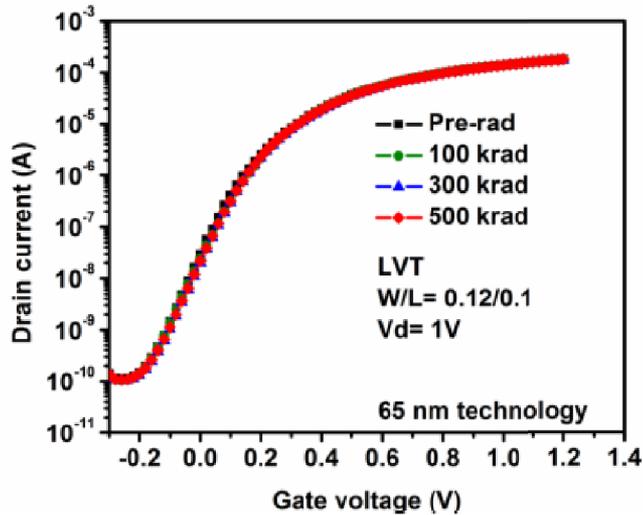
Underfill	FA10 Die Size	Weibull Life (cycles)	Weibull Slope
I	1x1 die	5534	11.0
I	2x2 die	3452	15.0
I	3x3 die	2807	5.4
III	1x1 die	3141	9.7
III	2x2 die	2090	5.3
III	3x3 die	1102	7.1
V	1x1 die	3740	11.1
V	2x2 die	2175	10.9
V	3x3 die	2219	3.9

Condition C, -65/150°C (15 minute dwells, 48 cycles/ day).



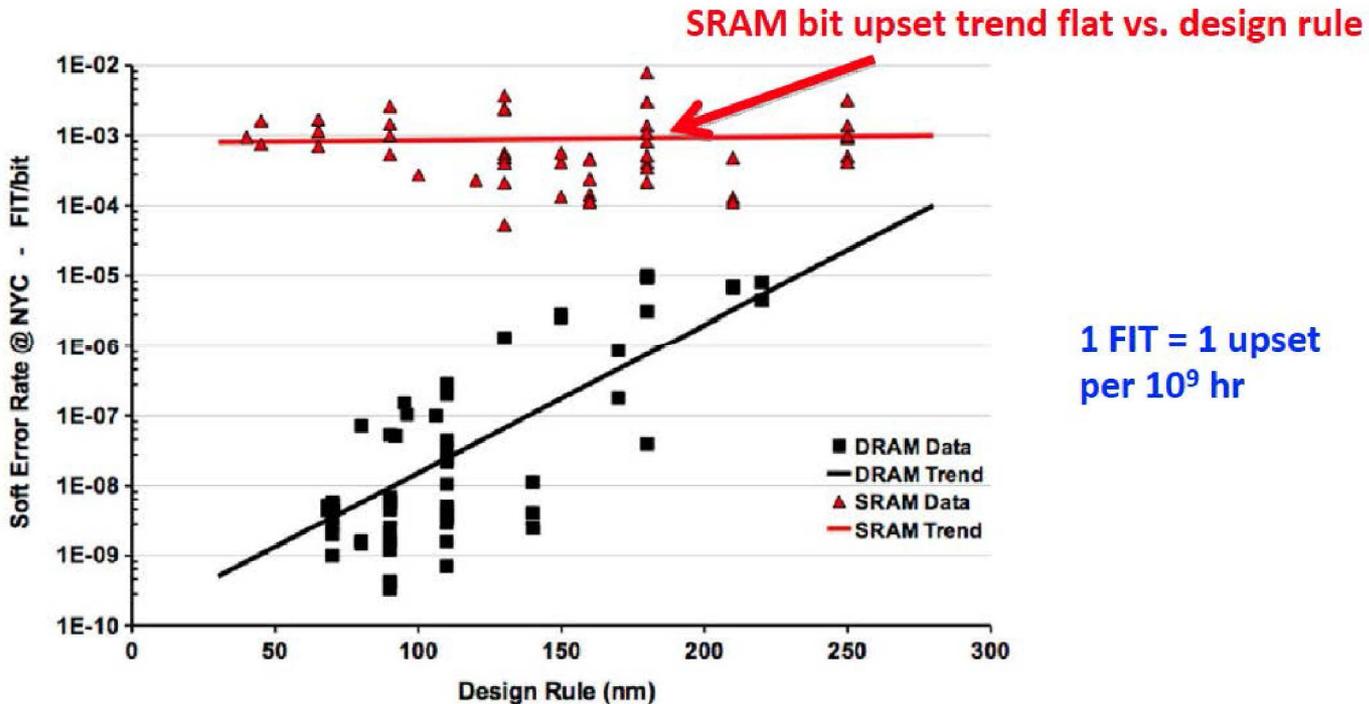


TID is limited concern for modern COTS





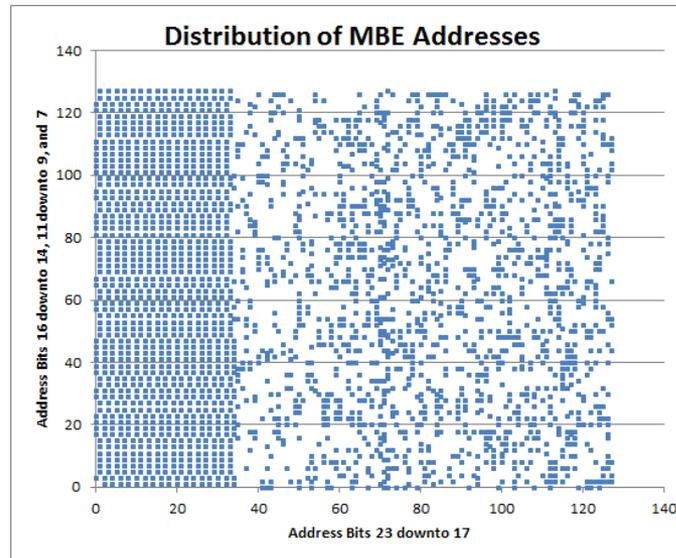
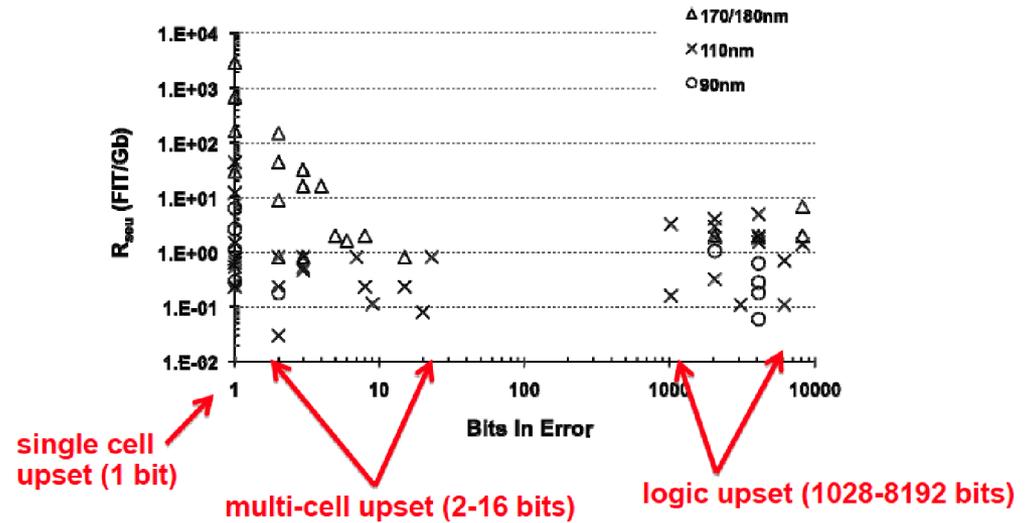
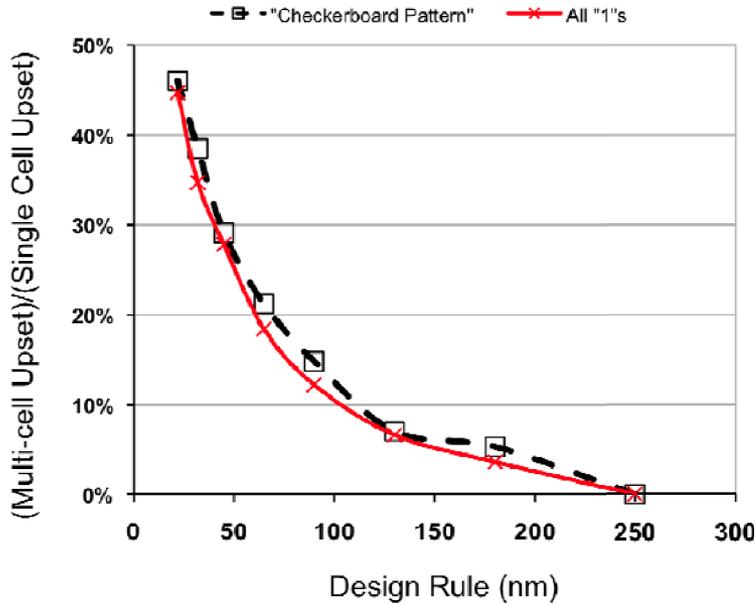
COTS emphasis on neutron radiation



- Decrease in SRAM cell Q_{crit} with process shrinks balanced by decrease in cell area, leading to flat soft error rate trend.
- Dramatic increase in SRAM bit density/part causes trend to go up slightly
- DRAM cell upset soft error rate trending downwards because Q_{crit} flat but cell area shrinking
- Upset of control logic in DRAM becoming more significant

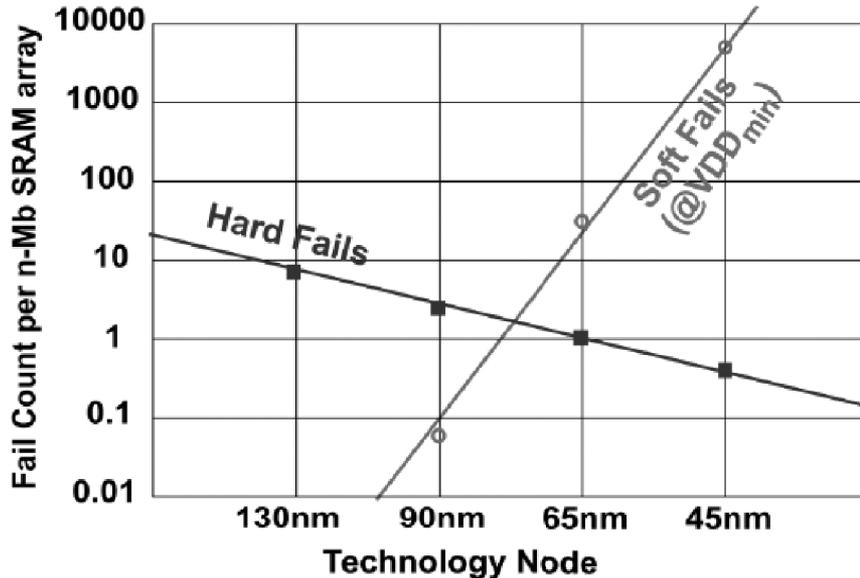


Multiple Bit Errors

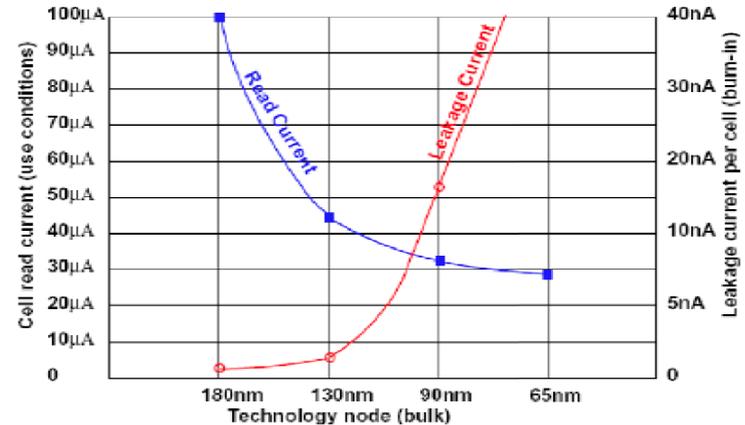




Failure types in SRAMs



Ion/loff: Cell Read and Leakage



H. Pilo, IEDM 2006⁸

- Hard fails are being reduced as processes have reduced defect densities
- Soft (voltage sensitive) failures increase due to reduced margins
 - Failure to write the cell
 - Signal margin fails which are driven primarily by slow bits that are otherwise stable and have write margin
 - Read stability fails for cells in the read or half-selected state
 - Retention fails.
- Manufacturers have to add new read and write assist circuit designs and innovative redundancy schemes to address performance issues.

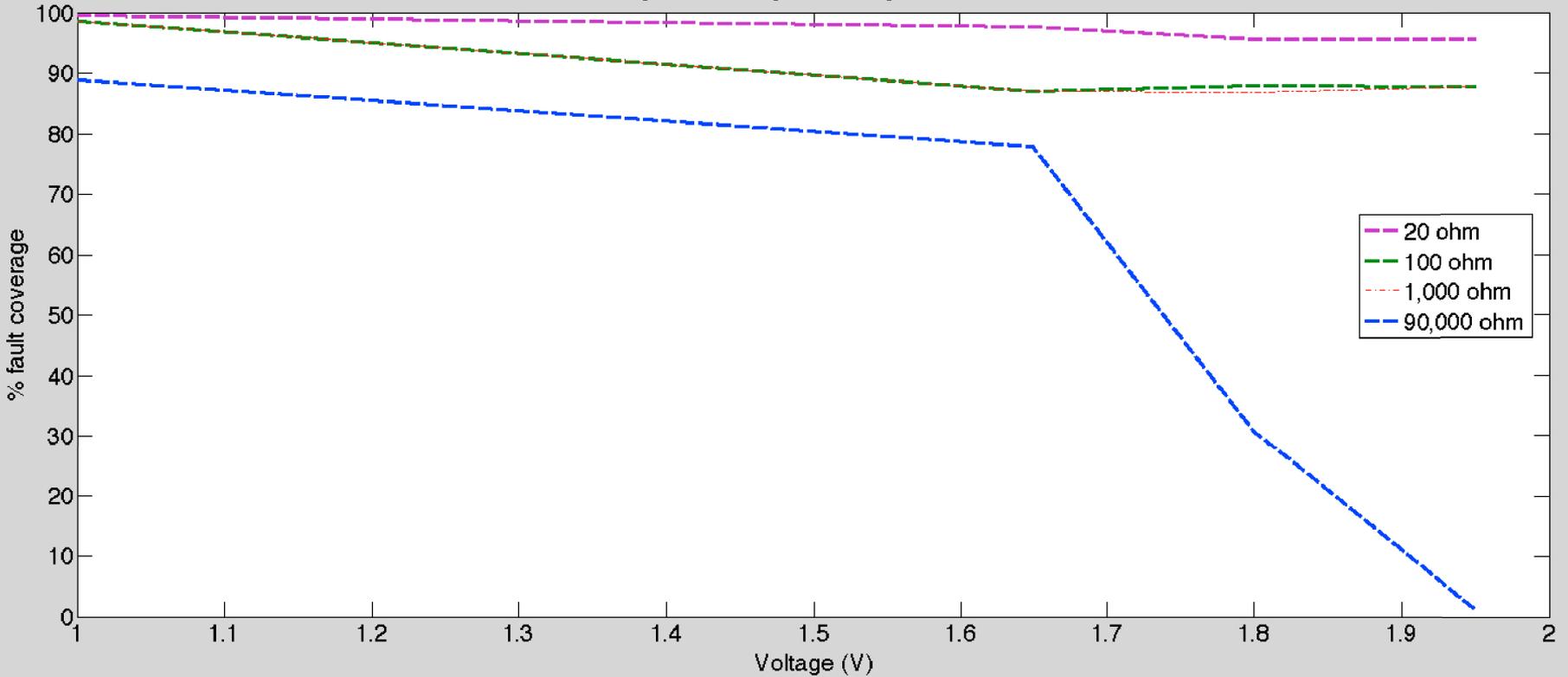


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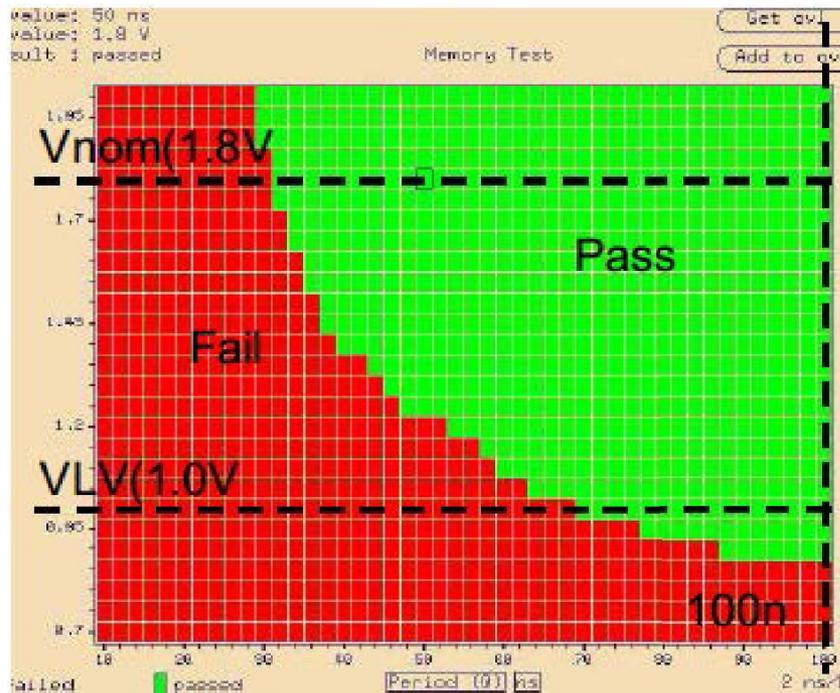
Electrical Testing Must Increase in Sophistication

Fault Coverage vs Voltage vs bridge resistance defect

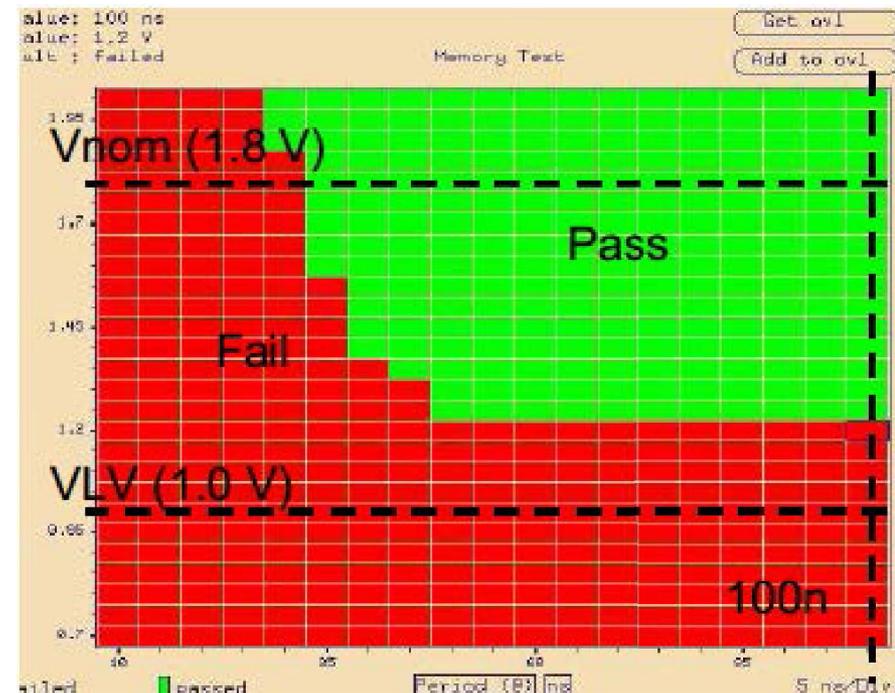




Shmoo plots to understand device performance



.vs.

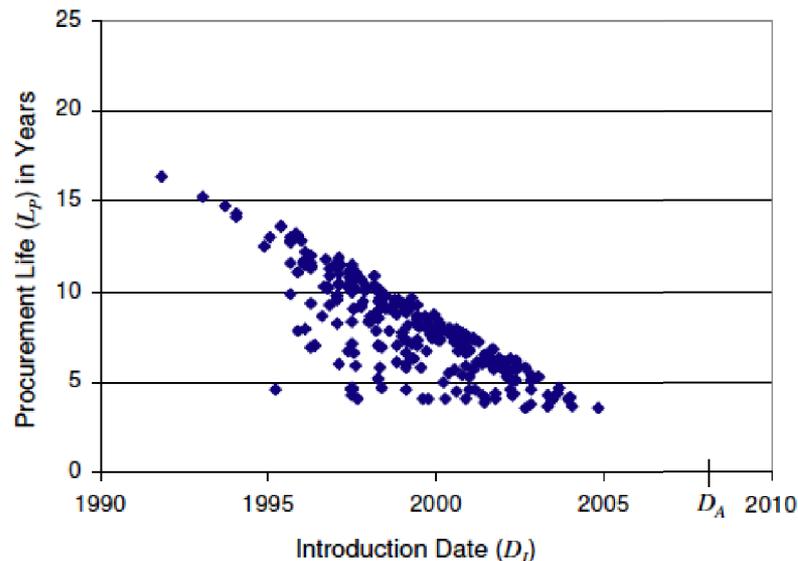


- Both parts pass normal test conditions (100nsec/Vdd_min/nom/max)
- RHS fails very low voltage screen



Technology Obsolescence

- **3% of global pool of electronic components become obsolete every month**
- **50 product discontinuances every day.**
- **Legacy parts and technology planning become a much more critical concern**
- **Heritage/legacy design success can no longer be easily assumed to be implementable**

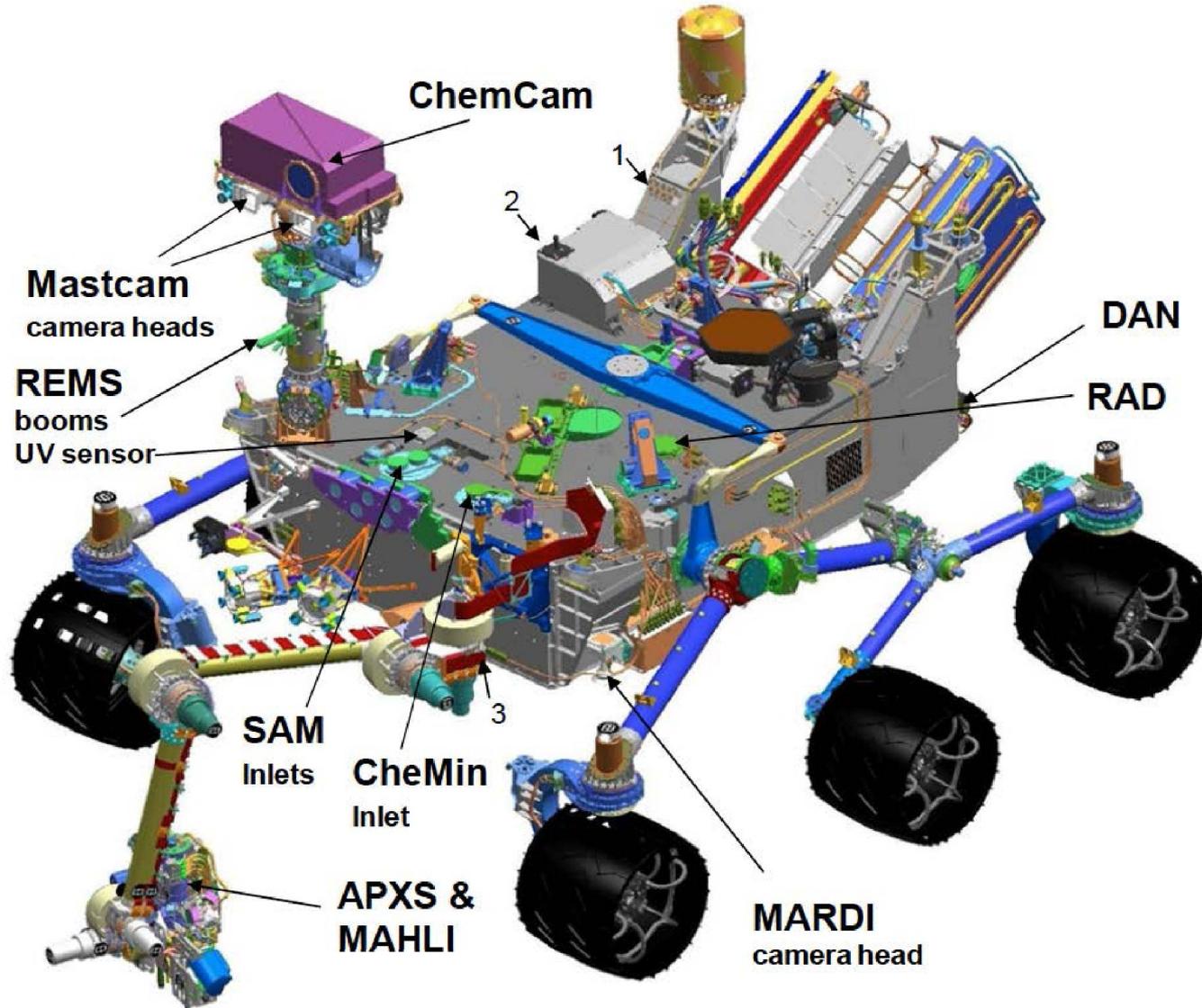




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MSL - Curiosity



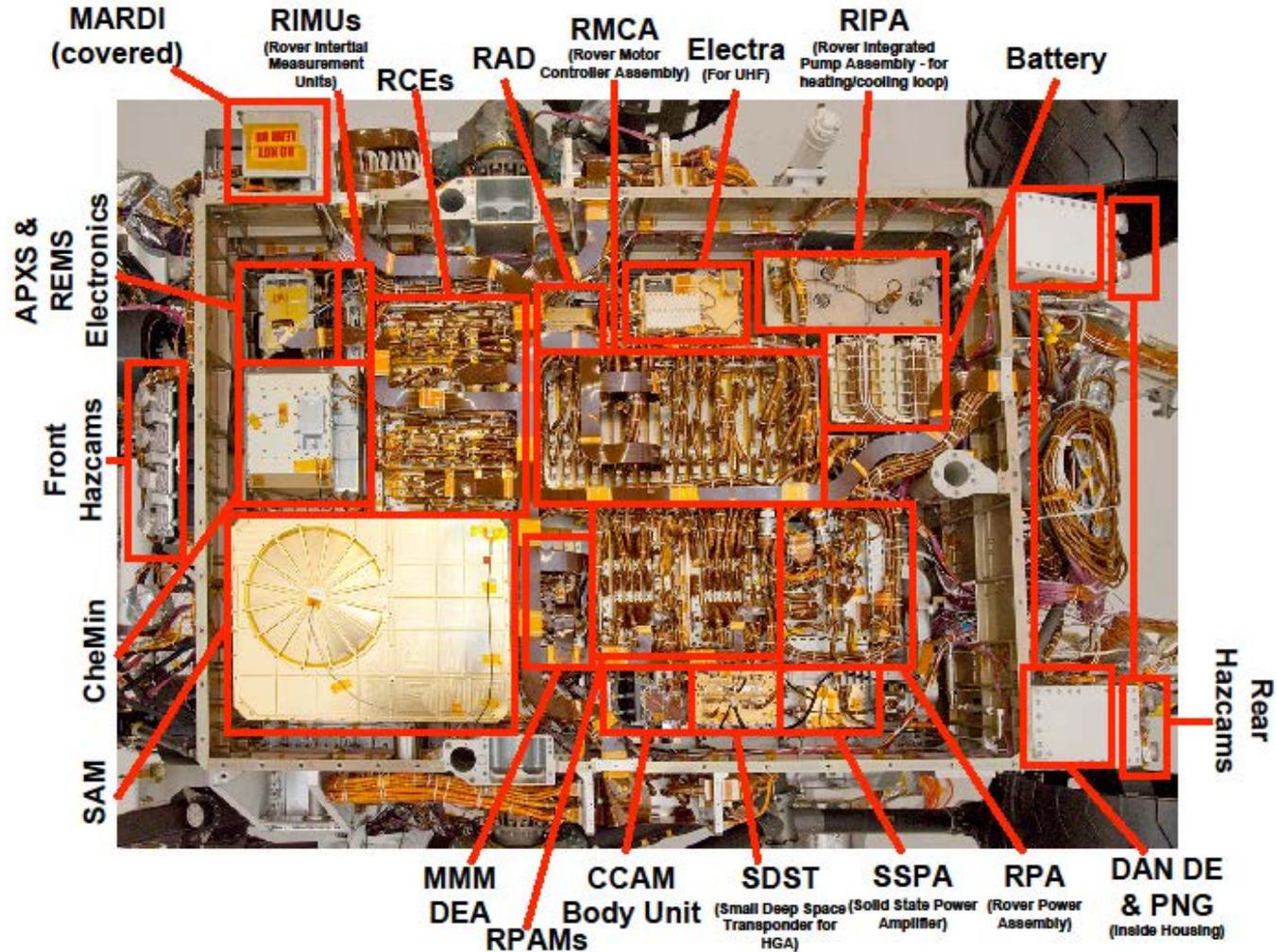


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Under the Hood

Avionics Environmental Design Challenges, HARSH2013
J. Donaldson, R. Manning, D. Sheldon





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FPGA Use on Curiosity

- **93 FPGAs in use on MSL (both rover and cruise/descent stages)**
 - Includes redundant design implementation and re-use
- **RTAX2000, RTSX72U, and XQR2V3000**
 - First use of a reprogrammable FPGA in mission critical radar and radio applications
- **Used in all aspects of operation**
 - **Avionics**
 - Command and Data Handling
 - Communication
 - Power management and control
 - Motor Control
 - **Science Instruments**
 - Hardware acceleration



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Sample FPGA Use in MSL Avionics

- **Interfaces to:**
 - **Ten science instruments**
 - **Attitude Control Systems: IMUs, Star Scanners, Sun Sensors**
 - **4 different radios (2 UHF radios and 2 X-band radios) that support uplink commands and downlink data**
 - **Two separate fully redundant 1553B buses to support commanding and collecting sensor data from Radios, MCAs, and Power/Analog Modules on the S/C**
 - **Motor and thruster actuators**
 - **Engineering Cameras**
- **Manage volatile/non-volatile memory allocations that support flight software images and data products**
- **Power regulation, control and switching**
- **Sleep & wakeup functionality along with dream mode...**
- **Battery charge and discharge control**
- **Pyro firing capability**
- **Analog telemetry (voltage and temperature measurement) sampling and collection**



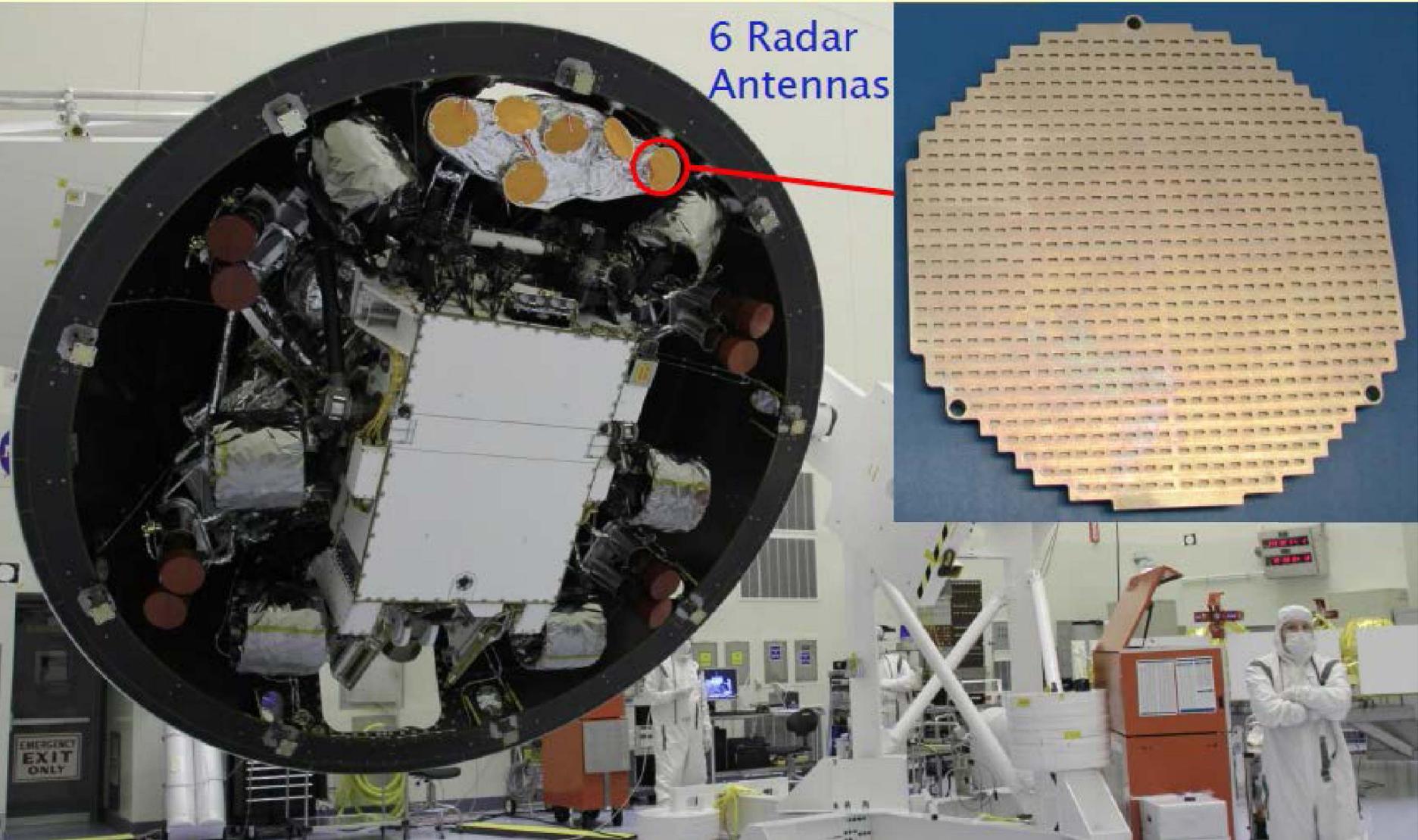
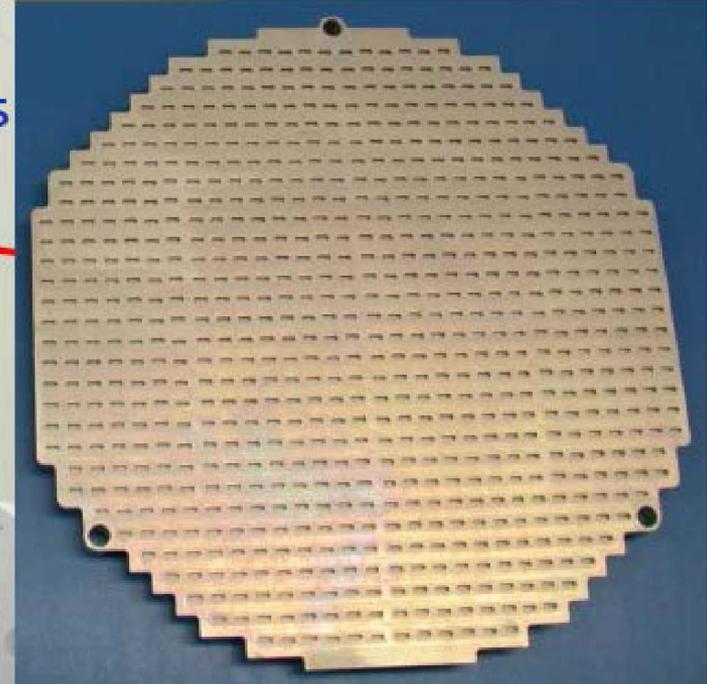
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Terminal Descent Sensor/Radar

“Antenna Design on Mars Landing Radar”, M. Guler, IEEE AESS/GRSS

6 Radar
Antennas





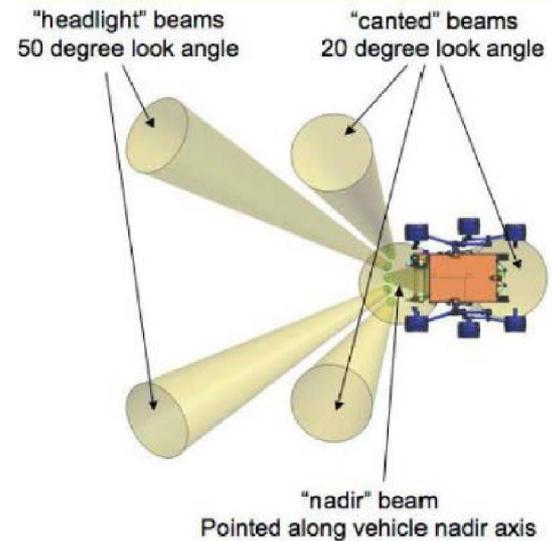
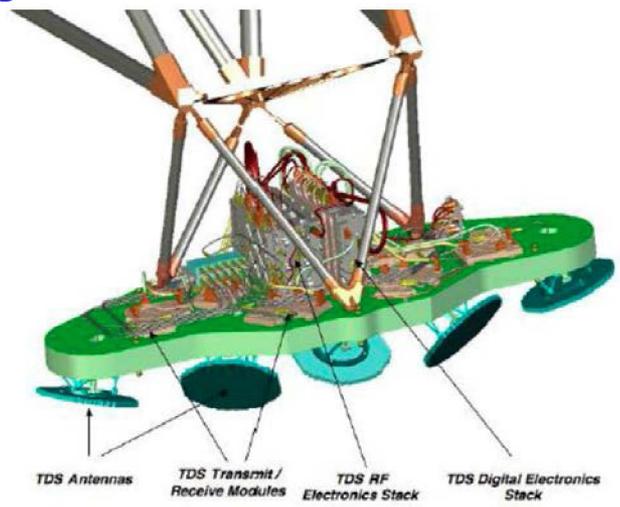
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Terminal Descent Sensor/Radar FPGAs

“Antenna Design on Mars Landing Radar”, M. Guler, IEEE AESS/GRSS

- **Ka-Band/Pulse Doppler Radar: Primary Navigation Sensor from the Point of Heat Shield Separation**
 - Provides exact Altitude and Velocity Data
 - Capable of measuring Terrain Relative Velocity
 - 6 independent Radar Beams: 3 beams canted 20 deg.
 - 2W peak power, 20Hz update rate, 4ns-16usec pulse width
- **XQR2V3000 provides a digital interface to/from the RF electronics and implements radar processing algorithms.**
- **RTSX-72SU provide low-level control functions: clocks generation/distribution, internal resets generation/distribution, 1553 interface, and XQR2V3000 configuration and scrub.**





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How This Relates to CMOS Scaling

- **MSL represents that state of the art in interplanetary rovers**
- **Significant complexity of operation required almost 100 FPGAs @ 130nm node**
 - **SWaP remains a key design issue for next generation**
- **Could a 10X reduction in SWaP be possible with highly scaled CMOS (>65nm) devices and packages?**
 - **Resulting fault-containment architecture may/may not become more complex and more difficult to design, analyze, and verify than either a single-string or fully redundant designs**
 - **Highly scaled devices imply many functions are integrated into one FPGA/SoC**
 - Historical test methods are serial, not parallel as now required for highly integrated devices.
 - **Functional Coverage vs. Code Coverage vs. Functional Simulation**
 - How and who determines when testing is complete and what the definition is



Summary

- **Commercial scaling technologies offer improvements in size, power, performance that will be required for next generation missions**
- **Demands for increased scientific data product quantity and quality require use of COTS parts**
- **Space architectures are different than telecom or consumer architectures.**
- **Graceful degradation and fault tolerant system solutions will be increasingly required over the entire spacecraft**
- **New materials, interfaces and physics will challenge historical part qualification schemes.**
- **Mission specific/custom qualification trends will increase**