



# Understanding Key Reliability Factors IPC Specifications

by

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**IPC Conference on Solder and Reliability: Process and Test  
November 13-14, 2013, Costa Mesa, CA**



# Outline

- Reliability
  - Definition
  - System to chip levels
  - Examples
- Key Reliability Parameters
  - Thermal cycle
  - Mechanical bend/shock
- IPC Spec on Reliability
  - TC
  - Mechanical
  - Detection/Characterization
- Summary



# MPF to Curiosity (1996-2012)





# Curiosity Rover

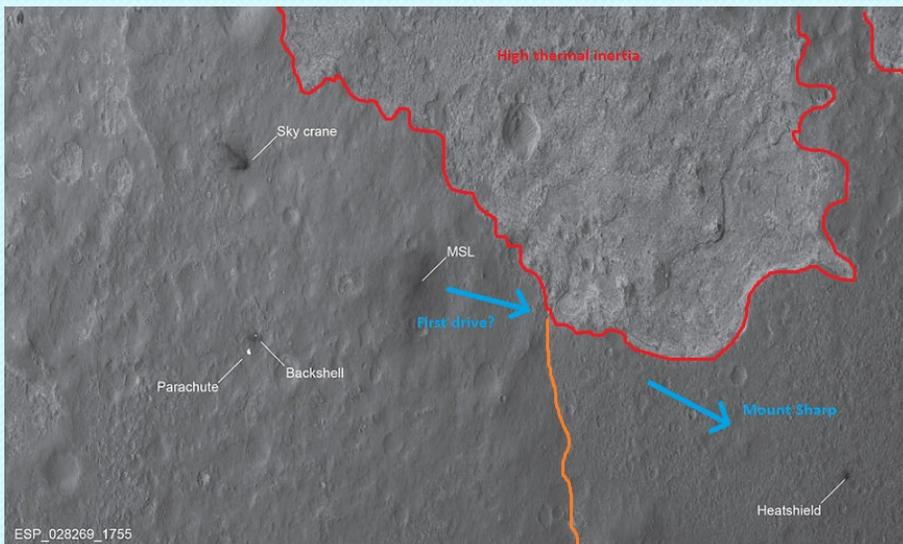
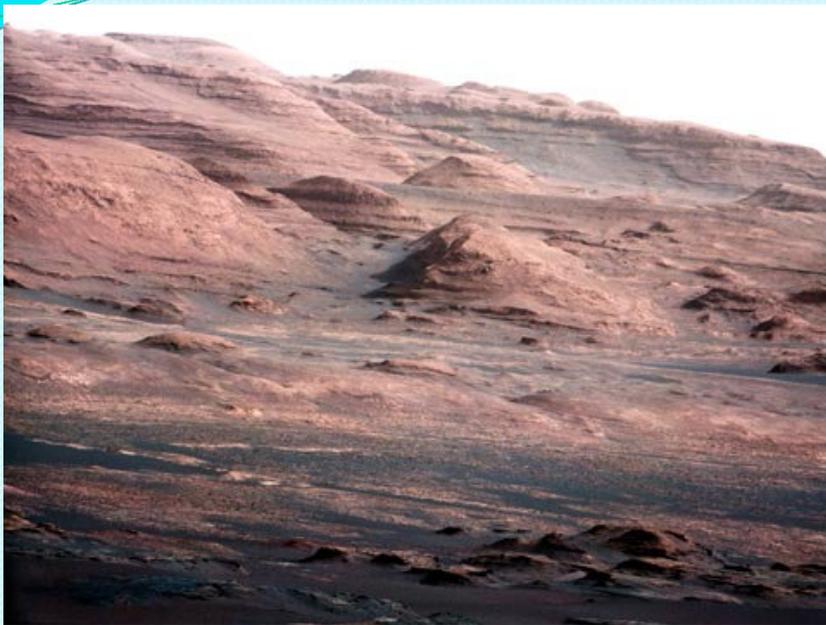




# Images & 1<sup>st</sup> Time Drill on Mars/Planet

*Detected Chloro-methane which could be resulted from organic-decomposition  
Such benign, could drink water*

NASA Briefing- Mar 12, 2013



ESP\_028269\_1755

IPC Conf. on Solder/Reliability, Nov 13-14, 2013

MAHLI - Sol 180 - Sweet Baby Drill Hole

Reza Ghahramani/JPL/Caltech



# Curiosity Finds Habitable Env.



**Opportunity-** Sulfate rich sand stone  
In presence of water  
**Not Habitable**

**Curiosity-** Neutral pH  
**Habitable Env.**  
If microbes ever present



# Curiosity Self-Portrait

## Updated Curiosity Self-Portrait at 'John Klein'

This self-portrait of NASA's Mars rover Curiosity combines dozens of exposures taken by the rover's **Mars Hand Lens Imager (MAHLI)** during the 177th Martian day, or sol, of Curiosity's work on Mars (Feb. 3, 2013), plus three exposures taken during Sol 270 (May 10, 2013) to update the appearance of part of the ground beside the rover.





# What is Reliability

**“Reliability is the ability to function  
as expected  
under the expected  
operating conditions  
for an expected time period  
without exceeding  
expected failure levels”**



# Reliability Threats





# Reliability Levels

## Missions

Benign- short/long

Extreme- short/long



## System/Box

TC/ Mech

Radiation



## Assembly - 2<sup>nd</sup> level

Package

Board

Interconnects



## Part - 1<sup>st</sup> level

Die/interposer

PTH/HDI

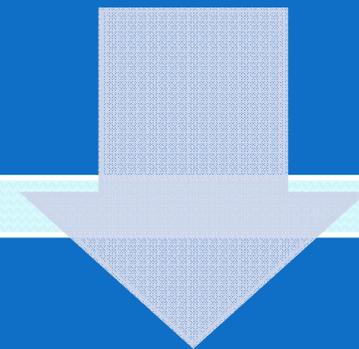
Flip-chip  
underfill



# SMT Array Reliability - I

## SMT

- Area Array (single/stack)
- PCB, (PTH/HDI)
- Interconnects (CBGA/CGA)
- Stake/Coat/Underfill)



## Advanced Arrays

- Hermetic/Non-H
- LGA
- FCBGA/interposer



# SMT Array Reliability- II

## SMT/Advanced Arrays

### Assembly, 2<sup>nd</sup> level

- Class Y, >1000 I/Os
- Hermetic, <1000 I/Os
- Interconnects, Pb & Pb-free

### Part, 1<sup>st</sup> level

- Chip cap
- FC balls/underfill
- Interposer



# Curiosity Memory Glitch

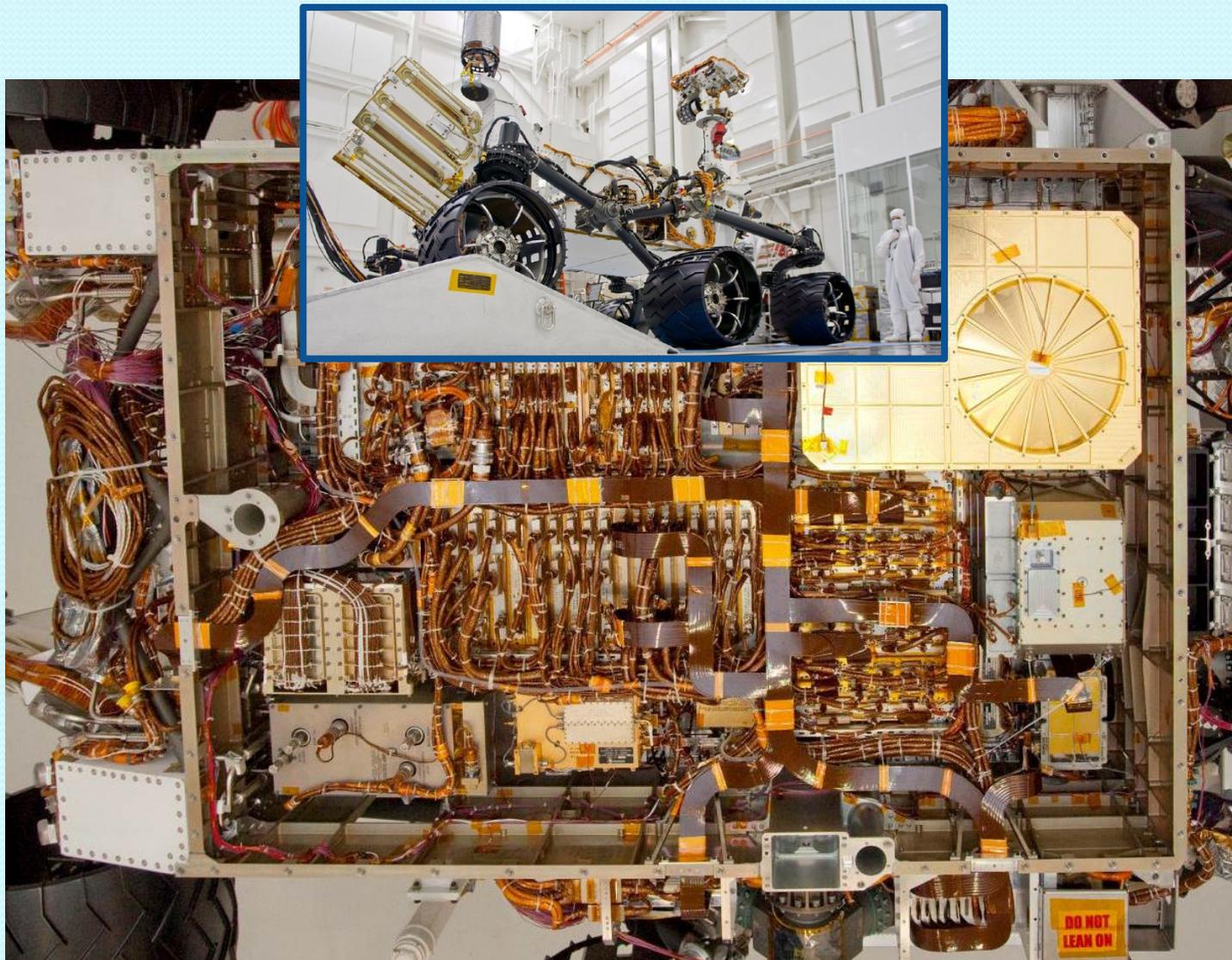
## Mission Status Report

PASADENA, Calif. - The ground team for NASA's Mars rover Curiosity has switched the rover to a redundant onboard computer in response to a **memory issue on** the computer that had been active.

The **intentional swap** at about 2:30 a.m. PST today (Thursday, Feb. 28) put the rover, as anticipated, into a minimal-activity precautionary status called "safe mode." The team is shifting the rover from safe mode to operational status over the next few days and is troubleshooting the condition that affected operations yesterday. The condition is related to **a glitch in flash memory** linked to the other, now-inactive, computer.

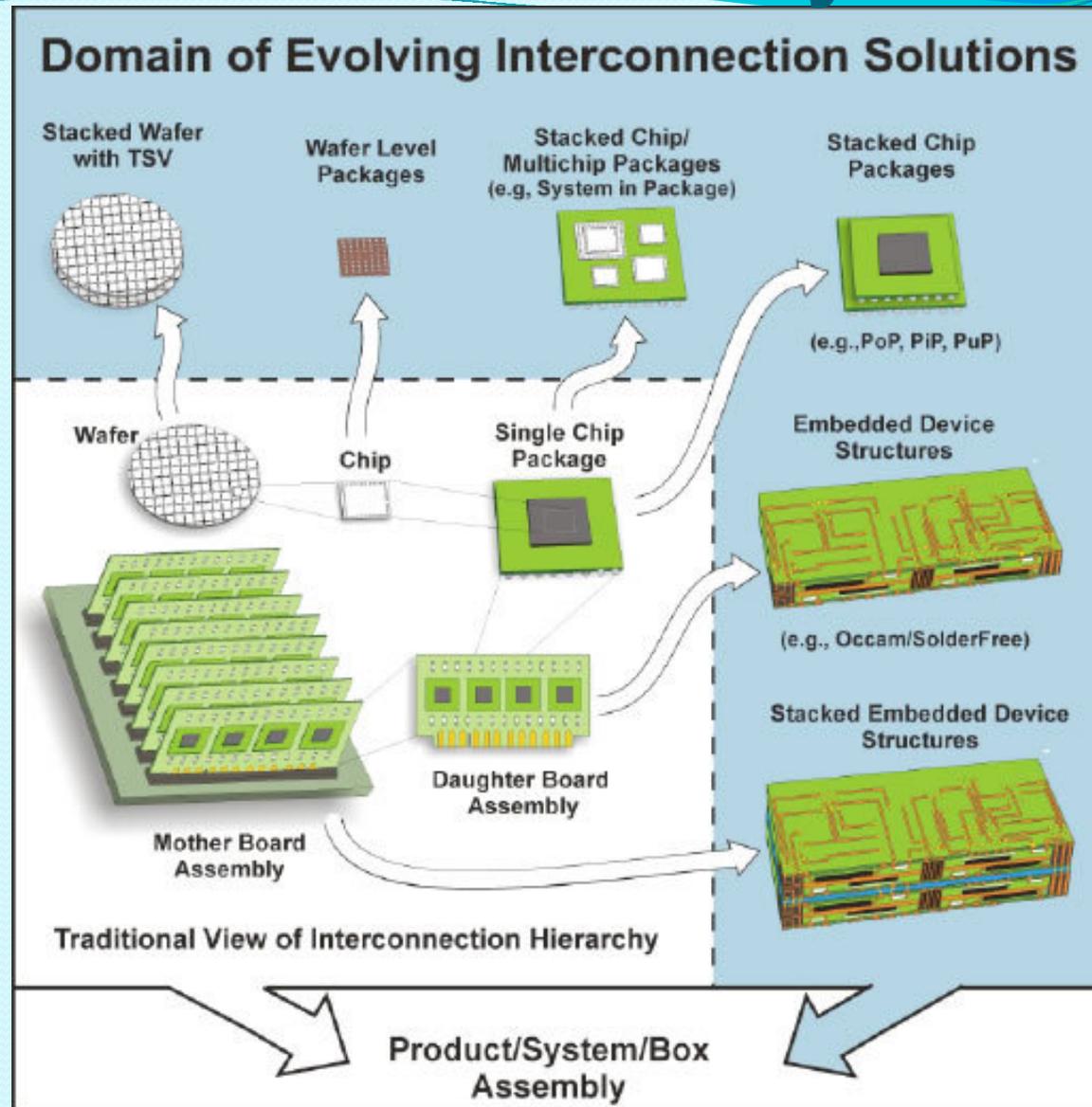


# System Level





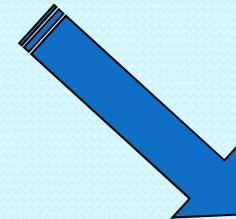
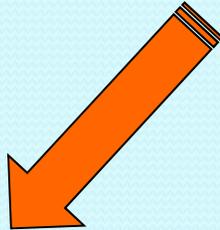
# Interconnect Hierarchy Changing





# Thermal & Mechanical

## Reliability



### Thermal

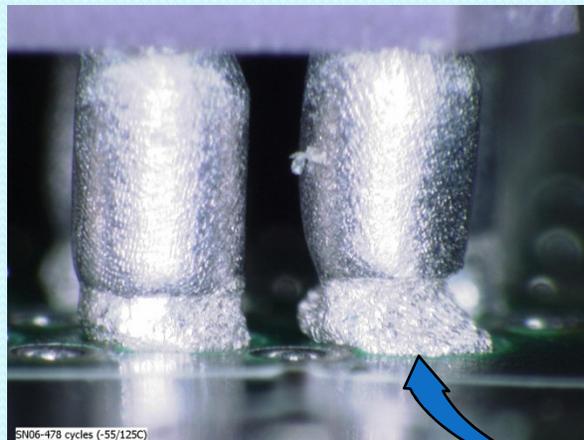
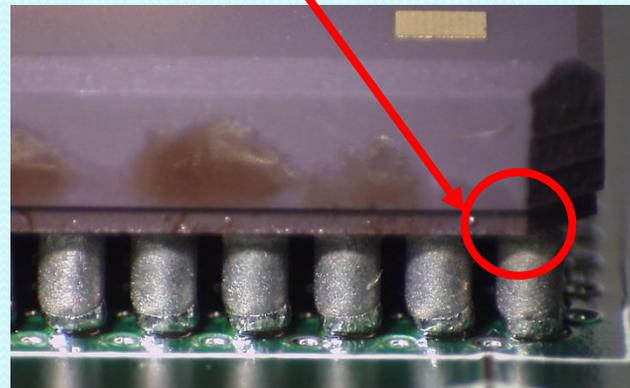
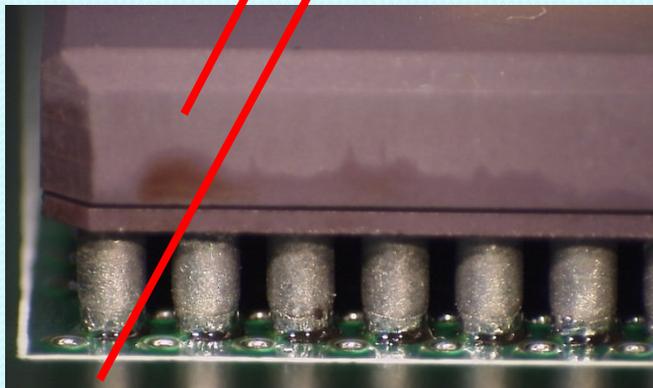
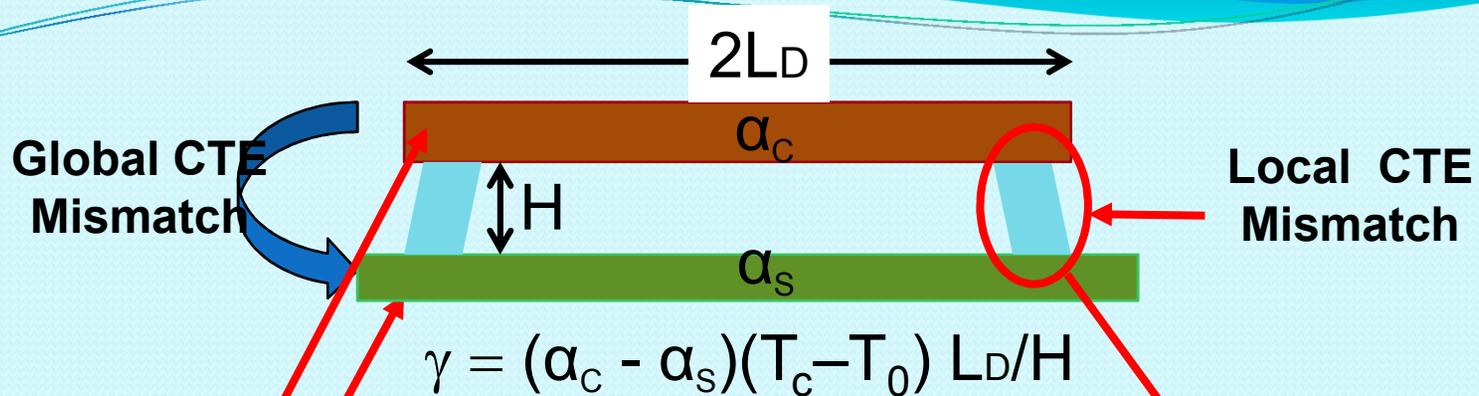
**Pkg/PCB Levels**  
**Thermal Cycle**  
**Storage**  
**Moisture**

### Mechanical

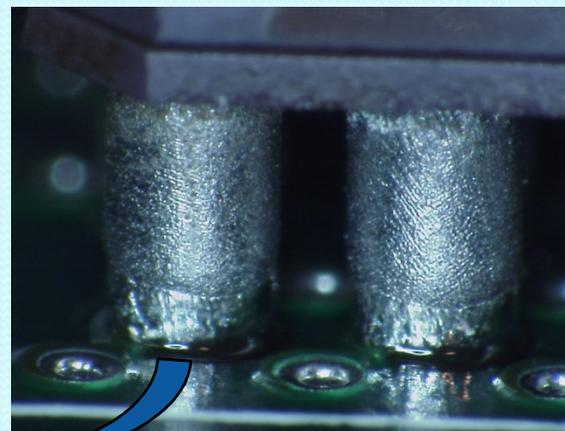
**Vibration**  
**Shock**  
**Drop**



# Reliability: Thermal Global/Local



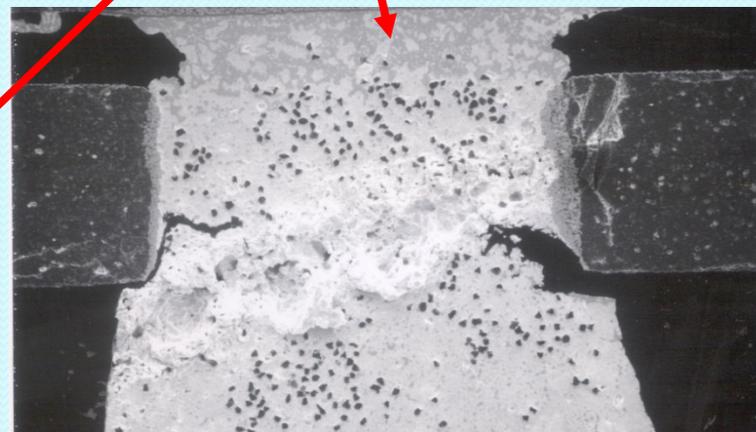
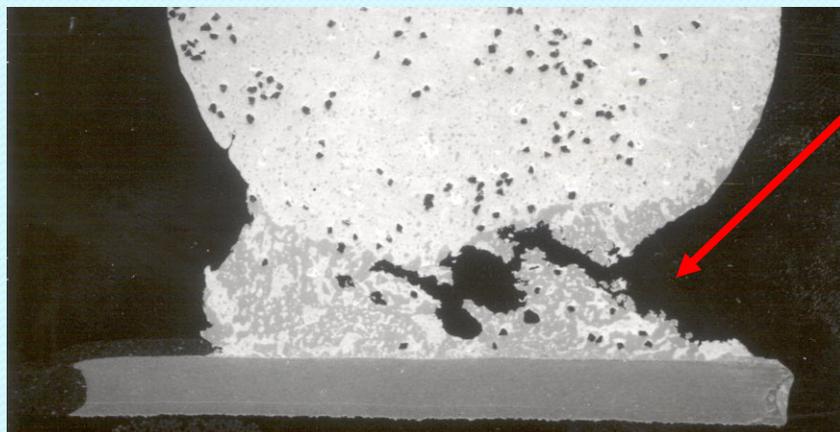
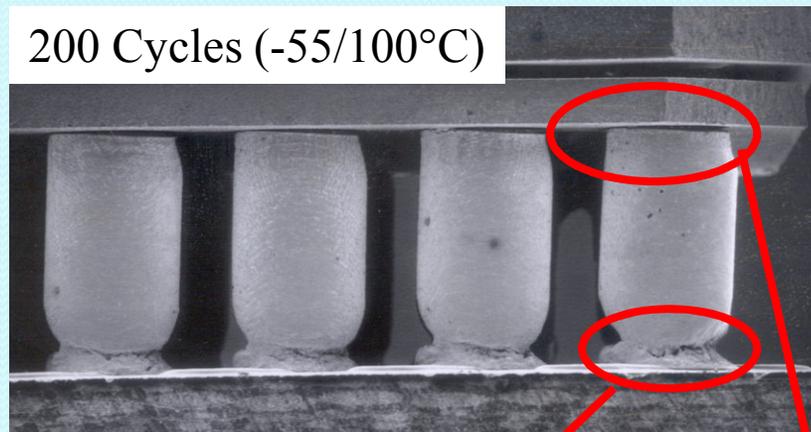
Solder Alloy  
CTE  
Mismatch





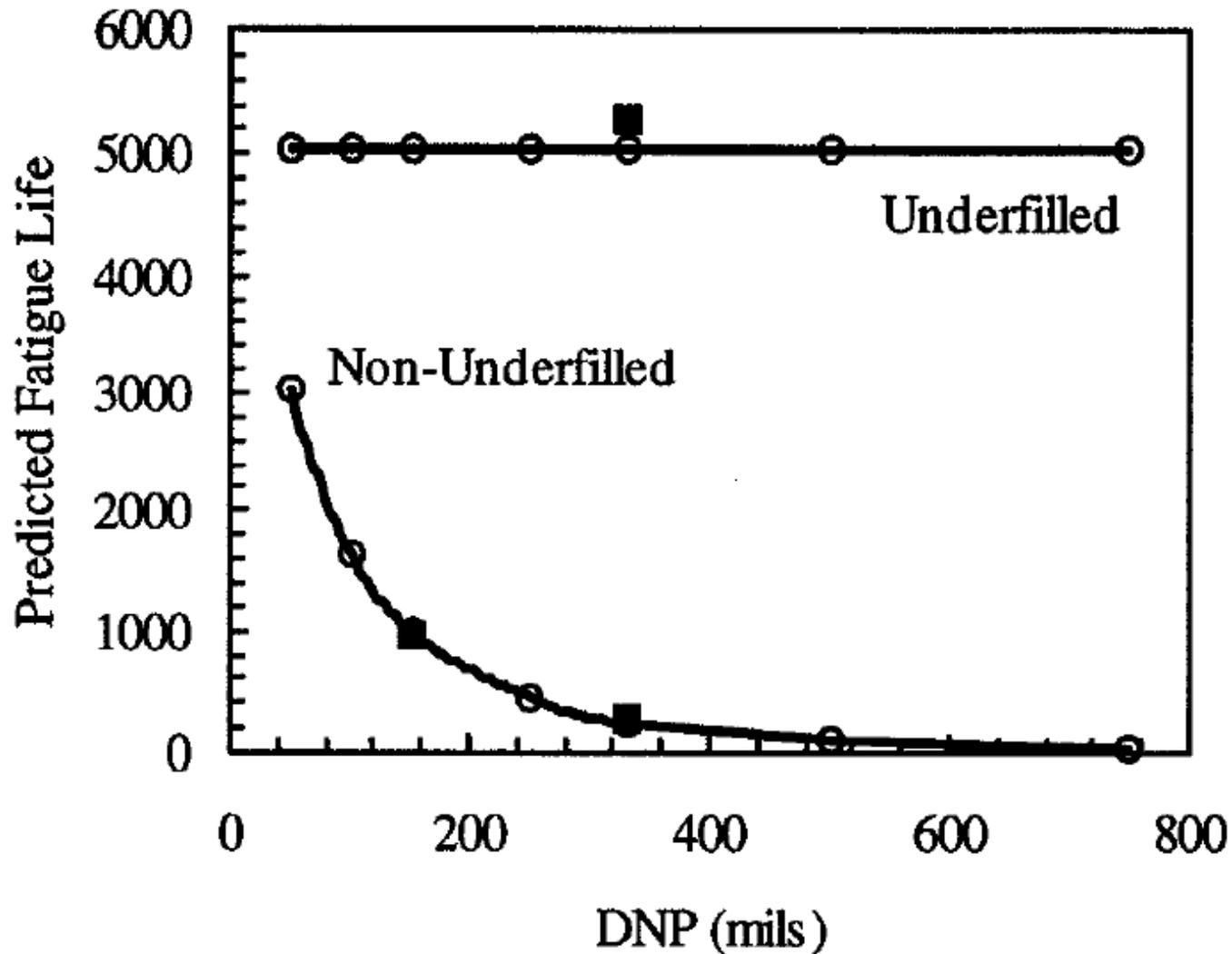
# Cracks Local/Global CTE

200 Cycles (-55/100°C)





# Flip-Chip TC W/Wo Underfill



Popelar, S.F., "A Parametric Study of Flip Chip Reliability Based on Solder Fatigue Modeling,"  
*IEEE/CPMT Int'l Electronics Manufacturing Technology Symposium*, 1997.



# TC Qual- IPC 9701

- IPC 9701, Released Jan 2002
  - IPC SM785- Guideline
    - No answer to the question of data for product application
    - Data comparison
  - IPC 9701
    - Details on thermal cycle test and acceptance
- Key Controls
  - Surface finish (OSP, HASL), thickness, 93 mil, NSMD, continuous monitoring, etc.
- Five Cycle Conditions
  - Preference 0/100°C
- Five number of thermal cycles
  - Preference 6,000 cycles

***IPC 9701- “Performance Test Methods and Qualification Requirements for Surface Mount Solder Attachments”***



# IPC 9701- Thermal Cycles

Table 1 Temperature cycling requirements specified in Table 4.1 of IPC 9701

Test Condition	Mandated Condition
Temperature Cycle (TC) Condition: <b>TC1</b> TC2 TC3 TC4 TC 5	<b>0°C ↔ +100°C (Preferred Reference)</b> -25°C ↔ +100°C -40°C ↔ +125°C -55°C ↔ +125°C -55 °C<-> 100°C
Test Duration Number of Thermal Cycle (NTC) Requirement: NTC-A NTC-B NTC-C NTC-D <b>NTC-E</b>	Whichever condition occurs FIRST: 50% ( <b>preferred 63.2%</b> ) cumulative failure (Preferred Reference Test Duration) or  200 cycles 500 cycles 1,000 cycles (Preferred for TC2, TC3, and TC4) 3,000 cycles <b>6,000 cycles (Preferred Reference TC1)</b>
Low Temperature Dwell Temp. tolerance (preferred)	10 minutes +0/-10°C (+0/-5°C) [+0/-18°F (+0/-9°F)]
High Temperature Dwell Temp. tolerance (preferred)	10 minutes +10/-0°C (+5/-0°C) [+18/-0°F(+9/-0°F)]



# IPC 9701- Pb free

- IPC 9701A, Pb-free guideline- Released 2006
- Appendix B, “Guideline for Thermal Cycle Requirements for Lead-free Solder Joints”
  - Moisture sensitivity, use J-STD-020
  - Reference to several models
    - Details to be covered in IPC 9706
- Release delayed due to lack of data on dwell- 2 dwells
  - D10 (10 minute dwell)
    - Most efficient
    - Use as “stand-alone”, only when modeling understood could be theoretically compared to tin-lead
  - D30+ (30 minutes or higher)- To experimentally induce damage somewhat comparable to tin-lead
- Surface finish
  - Only OSP, IAg
- Requalification is required when
  - Solder paste change
  - Lead terminal change



# IPC 9701- Failure Definition

Electrical (High and Low Temperatures)	Continuous intermittent event monitoring (preferred reference)  OR  Continuous electrical resistance monitoring (maximum scan interval of all chains = one minute). Manual monitoring is not allowed.
Failure Definition	Event detector: 1000 $\Omega$ , 10 events (maximum), 1 micro-second duration (maximum), report first verified as time-to-failure  AND/OR  Data logger/Voltmeter: 20% nominal resistance increase (maximum), five readings/scans (maximum)

## Failure Definition:

**Celestica:** 20% increase and data logger

**Solectron/Sun:** Event detector, not specified failure

**Xilinx:** Event detector, >500 ohms



# Questions on IPC 9701

Electrical (High and Low Temperatures)	Continuous intermittent event monitoring (preferred reference)  OR  Continuous electrical resistance monitoring (maximum scan interval of all chains = one minute). Manual monitoring is not allowed.
Failure Definition	Event detector: 1000 $\Omega$ , 10 events (maximum), 1 micro-second duration (maximum), report first verified as time-to-failure  AND/OR  Data logger/Voltmeter: 20% nominal resistance increase (maximum), five readings/ scans (maximum)

## Wrong Interpretation of Using Data Logger

- Take each scan and compare it to the last 5 scans. If the value is 20% higher than any of the five previous scans, then you have failure
- Compute moving average on 5 scans and plot the values. A 20% increase in from previous subgroup = failure
- Compare each scan to the previous value, if 20% higher, look for 5 scans at the higher value.

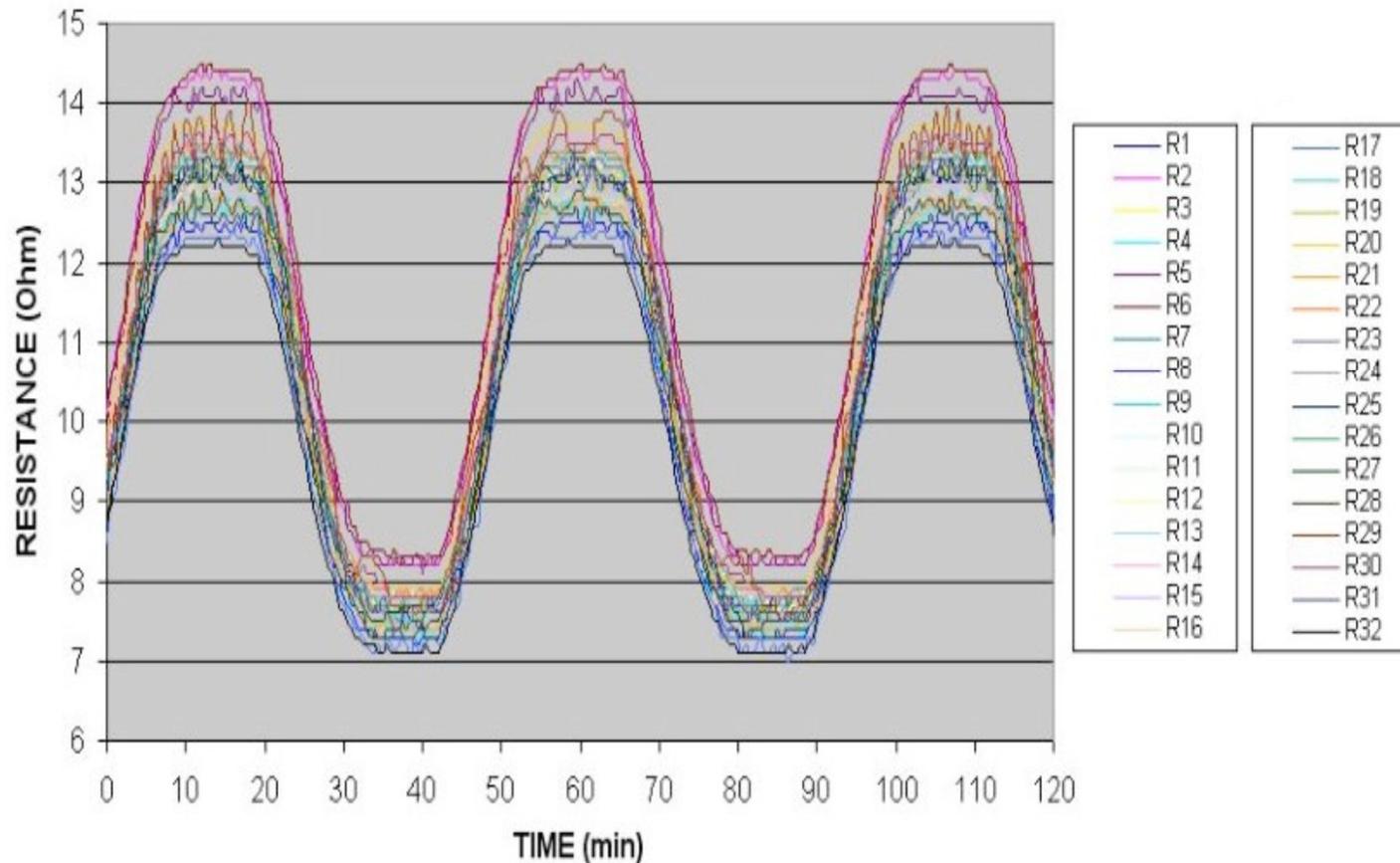
## Correct

Establish resistance value, preferably at max temp., and compare 20% resistance increase to this, five readings



# Correct Failure Interpretation

RESISTANCES MONITORING



Cycle -40°C to 125°C

Reference: CMSE, 2008, Olivier Gaillard, E2V



# Specifications Mechanical Testing

IPC & JEDEC

IPC/JEDEC-9702	Monotonic Bend Characterization of Board-Level Interconnects
IPC/JEDEC-9703	Mechanical Shock Test guidelines for Solder Joint Reliability
IPC/JEDEC-9704	Printed Wiring Board Strain Gage Test Guidelines
IPC/JEDEC-9707	Spherical Bend Test Method for Characterization of Board Level Interconnects
IPC-9708	Test Methods for Characterization of Printed Board Assembly Pad Cratering

JEDEC

JESD22-B111	Board Level Drop Test Method of Components for Hand Held Electronic Products
JESD22-B110A	Subassembly Mechanical Shock

Military

Mil-STD-810F  
Vibration/Shock  
Methods 514/516



# IPC 9704 Strain-Rate Guideline

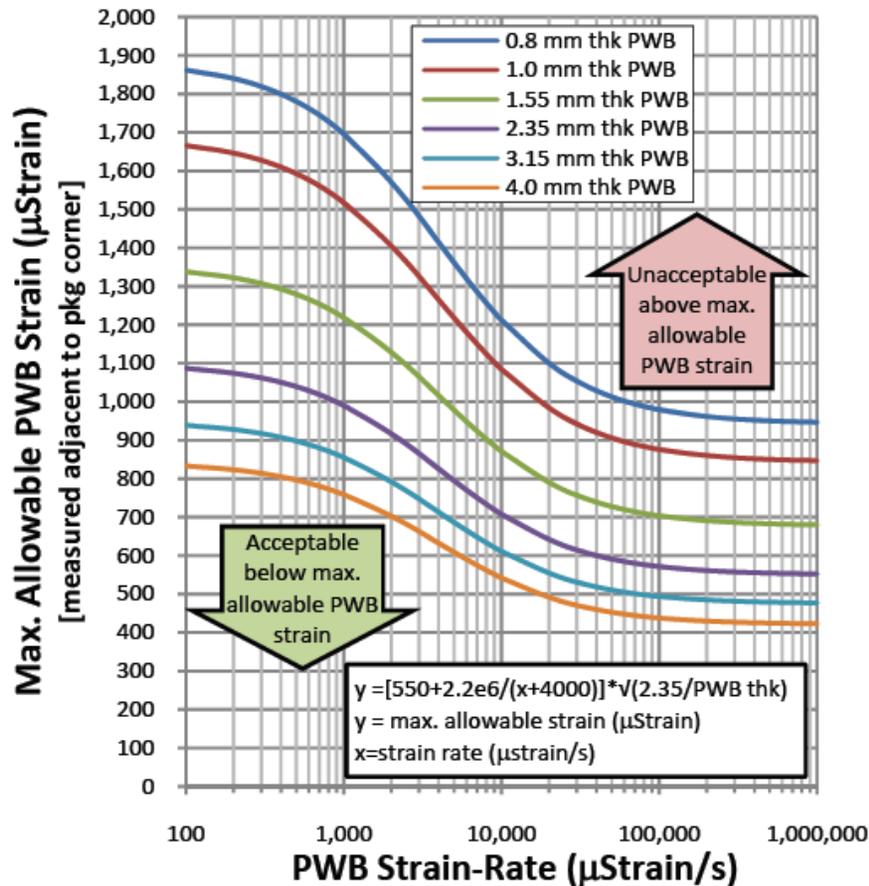
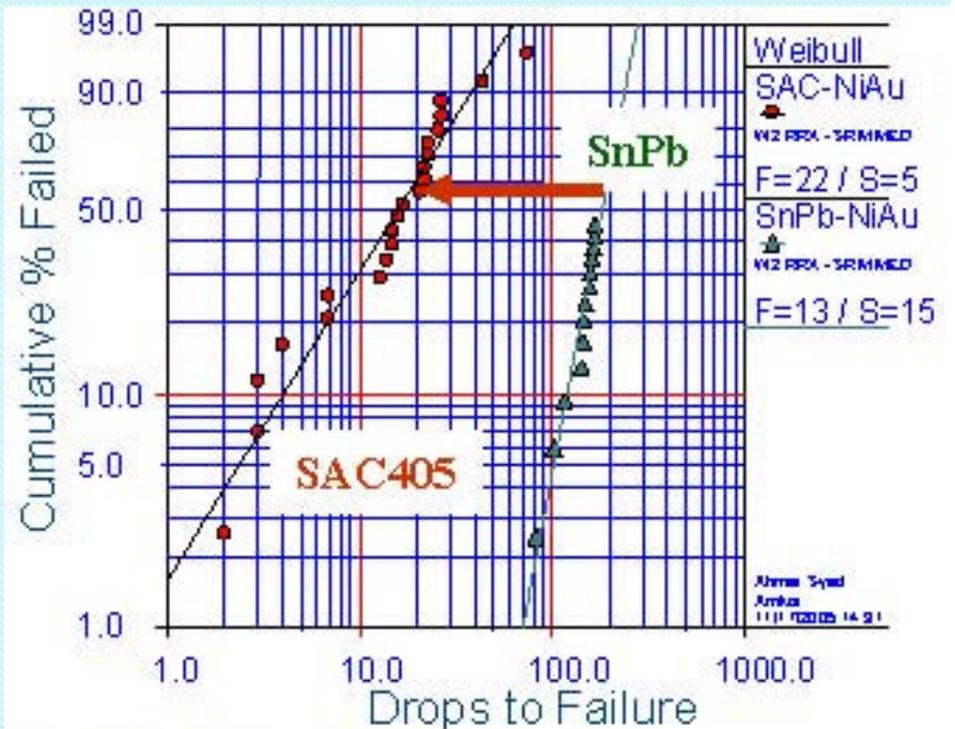


Figure 4 – Maximum allowable PWB strain (2005 guidance)



$\beta_1 = 1.36, \eta_1 = 21.14, \rho = 0.97$   
 $\beta_2 = 4.49, \eta_2 = 199.10, \rho = 0.97$



# Adhesives for Improvement M/T

## Function

- Mechanical Attachment
- Electrical Connection: Isotropic/Anisotropic(ACA)
- Stress Dissipation, low module elastomer
- Thermal Dissipation, silver epoxy

## Intended Use

- Bare die or chip device attachment, chip-on-board (COB), cap
- Substrate Attachment
- Lid Attachment

## SMT

- Package level: Underfill for flip-chip
- PCB level: Underfill/Corner stake for BGA, FPGA, CSP
- Solder replacement act as Pb-free
- Particle getters



# Flip-chip Die Reliability and Underfill Type

Flip-Chip Condition	T <sub>g</sub>	CTE1	CTE2	TC (0/125°C) Failure Model	TC Failure Experiment
No Underfill	NA	NA	NA	63	75
Underfill A	110	57	145	1228	1050
Underfill B Reworkable	80	30	87	1716	NA
Underfill C	125	30	86	5476	NA
Underfill D	150	33	87	6110	> 1500

Kwak, J.B., Chung, S., (*ITherm*), June 2, 2012

IPC Conf. on Solder/Reliability, Nov 13-14, 2013

Reza Ghaffarian/JPL/Caltech



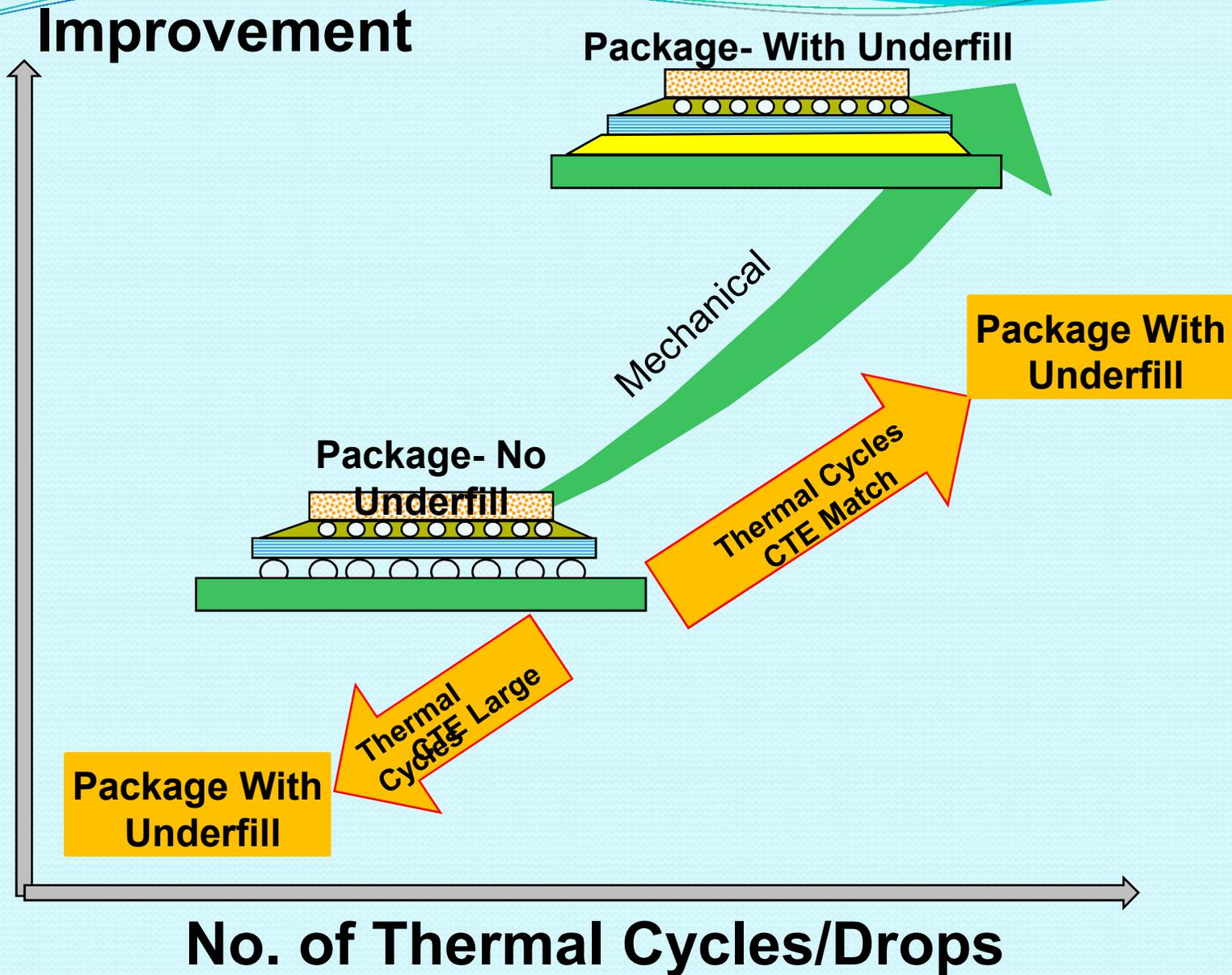
# FPBGA and Underfill

<b>FPBGA 108 I/Os 0.8 mm Pitch</b>	<b>T<sub>g</sub></b>	<b>CTE1 &lt;T<sub>g</sub></b>	<b>CTE2 &gt;T<sub>g</sub></b>	<b>TS Failure (-40/125°C)</b>	<b>10 Drops (6 feet)</b>	<b>Flex (1/2 max deflection)</b>
<b>No Underfill</b>	NA	NA	NA	~1000	100%	113
<b>Underfill A (3566)-Fast Flow</b>	135 (DSC)	50	170	~1000 (voids)	No Failure	>1250
<b>Underfill B (3567) Reworkable</b>	94 (TMA)	65	190	>3000	30%	>1250
<b>Underfill B- Reworked</b>	94 (TMA)	65	190	NA	10%	> 5000

Tian, G., Liu, Y., Johnson, W., Lall, P., Palmer, M., Islam, M., Crane, L., Yeager, E., Konarski, M., Torres, A., *IEEE Transactions on Electronics Packaging Manufacturing*, July 2005.



# Underfill Effect Mech. & TC Improvement





# IPC- Mech & Electrical Metrology

**Advanced  
Characterization  
For Mech Tests**

**IPC 9708  
Pad Cratering  
Released 2008**

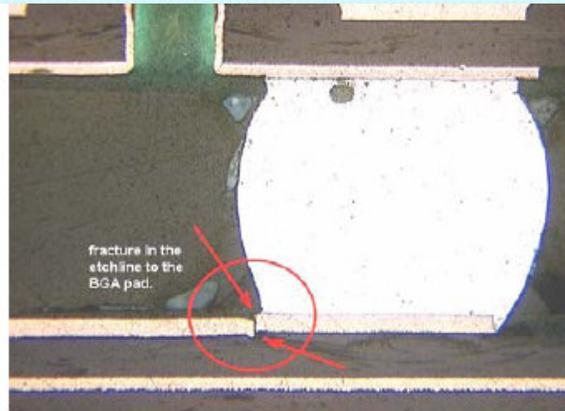
**Pin Pull  
Ball Pull  
Ball Shear**

**IPC 9709  
Early 2014  
Acoustic Emission  
For Mech Testing**

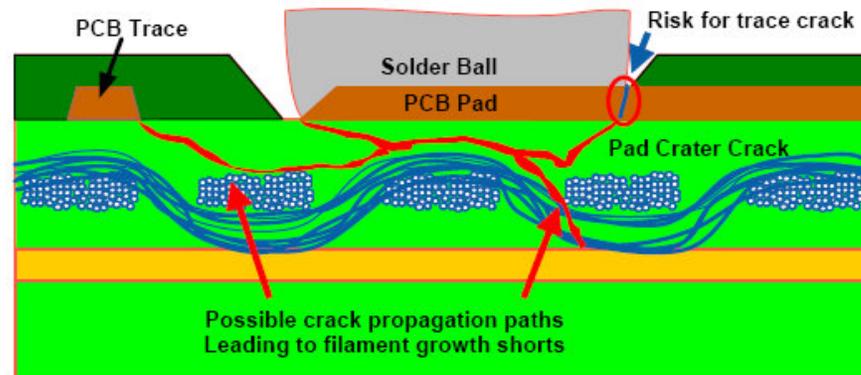
**IPC/JEDEC 9706  
Early 2014  
FCBGA/Mech Shock  
Electrical Metrology**



# IPC 9708 for Pad Crater Failure



Figures 1A and 1B – Open failures resulting from Pad crater circuit fractures.



## Lead Free Assembly Impacts on Laminate Material Properties and “Pad Crater Failures

Gary Long, Todd Embree, Muffadal Mukadam, Satish Parupalli, and Vasu Vasudevan  
Intel Corporation



# IPC 9708- PCB Pad Cratering

- **Pin-Pull Test**

- Any pad geometry
- No solder ball attachment
- More sensitive in differentiating printed board material and design variables than the ball shear test
  - *Pin to solder pad, expensive, time consuming*
  - *Solder paste printing*

- **Ball-Pull Test**

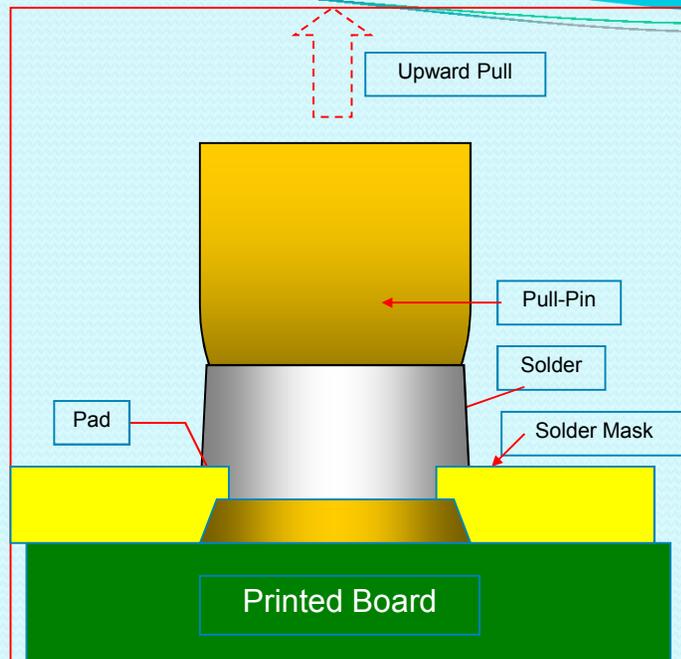
- Quick test after BGA ball attachment
- Cost effective – does not require expensive pins
- Can produce comparable failure modes as the pin pull test
  - *Can only be used for BGA pad geometries*
  - *Requires BGA ball attachment*
  - *Depends on solder ball, requires controls of more parameters*

- **Ball-Shear Test**

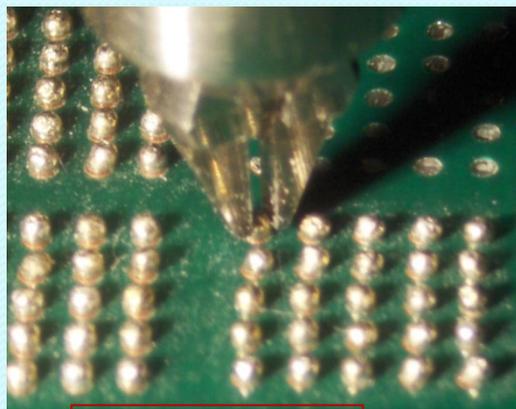
- Widely used, Quick test, easier than ball pull test
  - *Only BGA, require ball attach, less sensitive to PCB*



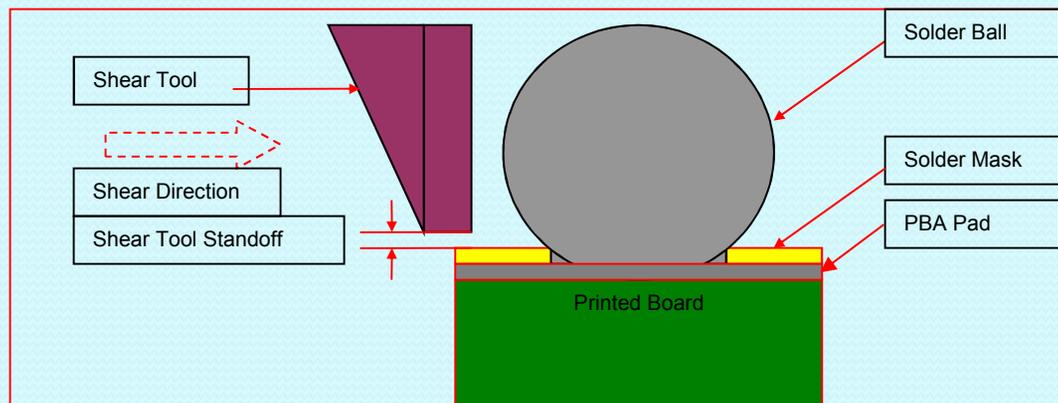
# IPC 9708- PCB Pad Cratering



**Pin Pull**



**Ball Pull**

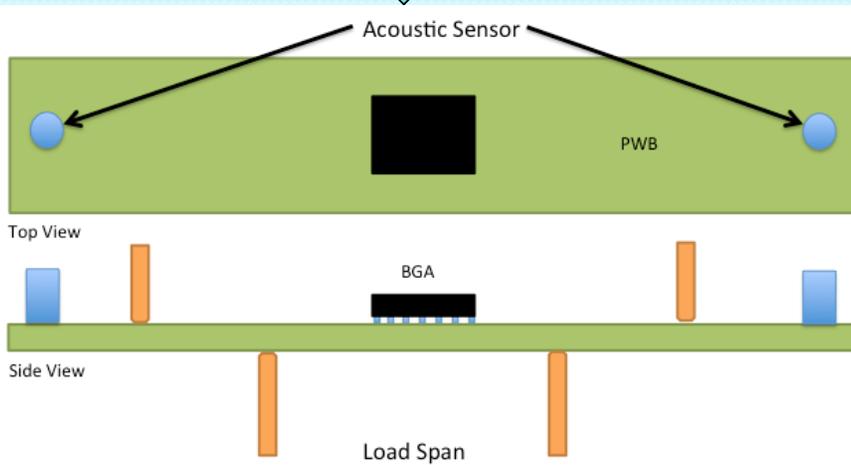


**Ball Shear**

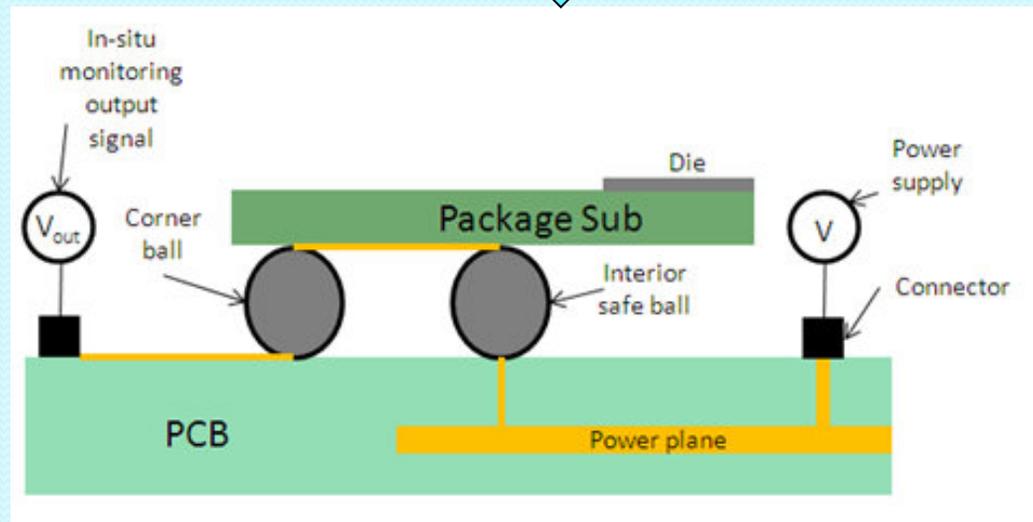


# IPC-9709 & 9706

**IPC 9709**  
Acoustic Emission  
For Mech Testing as  
Monitoring

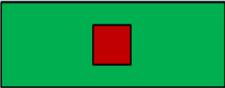


**IPC/JEDEC 9706**  
FCBGA/Mech Shock  
Using Voltage as  
Monitoring





# AE & Early Detection

<b>FCBGA 1517 I/Os SAC 305 balls</b>	<b><math>\mu</math>Strain Electrical</b>	<b><math>\mu</math>Strain Acoustic</b>
 <b>0°, NSMD, 3x reflow</b>	<b>~2800</b>	<b>~ 2000</b>
 <b>45°, NSMD, 3x reflow</b>	<b>~ 3250</b>	<b>~ 1800</b>
 <b>45°, SMD, 3x reflow</b>	<b>~ 2250</b>	<b>~2100</b>
 <b>45°, NSMD, 1x reflow</b>	<b>~3500</b>	<b>~2000</b>



# Summary

- Reliability

- Define intended use, narrow requirements
- Level 1 to system cost increases

- Key Parameters

- Underfill/staking for TC/Mech
- Judicial selection

- IPC/JEDEC 97xx Spec on Reliability

- IPC 9701 for TC widely used
- IPC/JEDEC 9702 Bend, 9703 Shock, 9704 Strain gauge, 9707 Spherical bend
- IPC9708 Pad Cratering, IPC 9709 AE
- IPC/JEDEC 9706 Electrical Metrology for Mech Shock



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