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NASA Space Component Strategies for Today and Tomorrow

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Curiosity, the big rover of this artist's concept depicts the moment that NASA's Curiosity rover touched down onto the Martian surface. Image credit: NASA/JPL-Caltech

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Introduction



- **Thank you Tamura-san and JAXA for your invitation. It's always a pleasure to visit Tsukuba.**
- **Our congratulations to JAXA on the 26th anniversary of the MEWS Workshop!**
- **JAXA is our valued partner in NASA Electronic Parts Assurance Group (NEPAG) activities**
- **This talk is about NASA space component strategies for today and tomorrow.**
- **It is divided into four parts:**
 - **Present Issues**
 - **Changing landscape**
 - **Challenges associated with infusion of state-of-the art complex devices into the QML system – the Class Y initiative**
 - **Future**

Space Component Strategies Today

Existing Military Documents



- **Microcircuit Devices**

- **Current Activities**

- **MIL-STD-883, Test Method (TM) 2017 (Visual Inspection for Hybrids)**
 - ◆ Changes were discussed in last Task Group meeting
 - ◆ The TM is to be updated
 - **MIL-HDBK-217, Reliability Prediction**
 - ◆ The most recent version is Revision F, Notice 2, released in 1995
 - ◆ No change in status
 - **MIL-STD-883, Test Method 1014 (Hermeticity)**
 - ◆ Clarified Krypton leak test for flat-top crystals
 - ◆ Optical leak test
 - **MIL-PRF-38534**
 - ◆ Add Photonics?
 - **MIL-PRF-38535, Revision K (Draft)**
 - ◆ Introduces Class Y

Space Component Strategies Near-Term Challenges



- **Microcircuit Devices**
 - **Some Challenges**
 - **Dual-use Technology**
 - ◆ Infusion of selected commercial device functions into QML
 - ◆ Parts might not operate over the full military temperature range
 - ◆ There may be hot spots on the die (use thermal imaging)
 - **Testing High-speed Devices**
 - ◆ Request new JEDEC task group to address this challenge
 - ★ What can be tested?
 - ★ How?
 - ★ What is good enough?
 - ◆ Consider forming consortium with manufacturers and other users
 - **Upscreening of plastic encapsulated microcircuits (PEMs), lower grade hermetic parts**
 - ◆ Many challenges:
 - ★ electrical testing,
 - ★ type of burn-in,
 - ★ Glass-transition temperature (for PEMs),
 - ★ third-party management, etc.
 - ◆ Several Variations

Space Component Strategies Near-Term Challenges



- **Microcircuit Devices**

- **Some Challenges**

- **Counterfeit Parts.**
 - ◆ World-wide problem
 - ◆ Buy parts from franchised/authorized distributors
 - **Cyber attacks via back doors**
 - ◆ World-wide problem
 - ◆ Work with manufacturers
 - **Supply Chain Management**
 - ◆ Self audits are an issue
 - ◆ Work with (in case of the United States) DLA Land and Maritime
 - ◆ Handling and electrostatic discharge (ESD)
 - **Xilinx Field Programmable Gate Arrays (FPGAs)**
 - ◆ Details in later slides

Space Component Strategies Near-Term Challenges



- **Microcircuit Devices**
 - **Current Activities**
 - **Burn-in screening and life test**
 - ◆ Clarify requirements
 - ◆ Insure proper implementation
 - ◆ Details in later slides
 - **Base-Metal Electrode (BME) Capacitors**
 - ◆ Develop a proper screen to allow for their use in space products
 - ◆ Several evaluation efforts in progress
 - ◆ Also, see page 22
 - **Column Grid Arrays (CGAs)**
 - ◆ Effect on device performance
 - ◆ Details in a later slide
 - **Infusion of new technology into U.S. Department of Defense (DoD) standards**
 - ◆ Created a new category (Class Y)
 - ◆ MIL-PRF-38535, Revision K introduces Class Y
 - ◆ Details in later slides

Infusion of New Technology into MIL Standards



The “Class Y” Initiative

- **Advances in packaging and device technology are happening rapidly.**
- **How do we enable space flight projects to benefit from the newly developed devices?**
- **NASA is leading a G12 initiative, called Class Y, for infusing this new type of complex devices into military/space standards. Class Y is envisioned as a new category of ceramic-based non-hermetic microcircuits, such as the Virtex-4 and Virtex-5 field programmable gate arrays (FPGAs) offered by Xilinx Corporation.**
- **Creation of a new class of microcircuits (such as Class Y) has required considerable effort. It must be coordinated with manufacturers, government agencies, prime contractors, and other interested entities (e.g., academia). Also, we need to ensure that all aspects of packaging configuration are adequately covered by the military documents, such as MIL-PRF-38535 and MIL-STD-883. These packaging aspects include flip-chips, underfills, adhesives, column attaches, and others**
- **New test methods must be created and the existing standards updated as necessary.**

Infusion of New Technology into MIL Standards

Adding Class Y to Microcircuits Specification



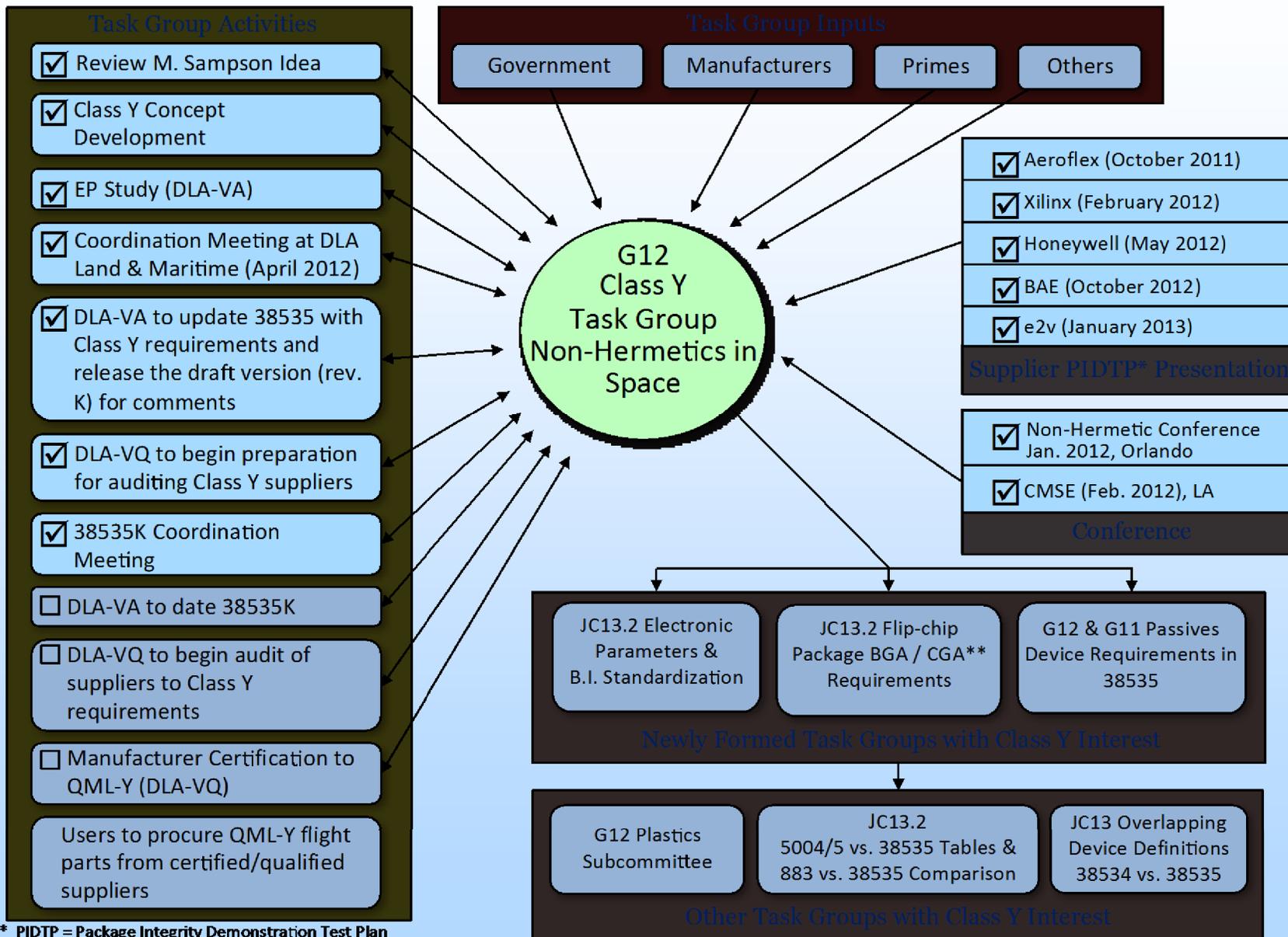
- **Microcircuits specification, MIL-PRF-38535**
 - Next revision (K) is in preparation
 - Introduces Class Y
 - Second draft available now
 - Comments were due by June 24, 2013

- **Acknowledgements**
 - Special thanks to DLA-VA
 - Thanks to everyone including task group (TG) members and advisors

- **Class Y Status**
 - See the next sheet

Infusion of New Technology into MIL Standards

G12 Class Y Effort at a Glance



* PIDTP = Package Integrity Demonstration Test Plan

** BGA / CGA = ball-grid array / column-grid array

Infusion of New Technology into MIL Standards Class Y



Qualifying New Packaging Technology

- **Issue**
 - How to address the manufacturability, test, quality, and reliability issues unique to specific non-traditional assembly/package technologies intended for space applications?
- **Proposal**
 - Each manufacturer to develop a Package Integrity Demonstration Test Plan (PIDTP).
 - Addresses issues unique to non-hermetic construction and materials, such as potential materials degradation, interconnect reliability, thermal management, resistance to processing stresses, thermo-mechanical stresses, & shelf life.
 - The PIDTP shall be approved by the qualifying activity after consultation with the space community. Ref: 38535K, Para B.3.11

Infusion of New Technology into MIL Standards

Class Y

Applicability of the PIDTP



- **The Packaging Integrity Demonstration Test Plan (PIDTP) requirement would apply to:**
 - Non-hermetic packages (e.g., Class Y)
 - Flip-chip assembly
 - Solder terminations
- **Microcircuits employing more than one of above technologies shall include elements for each in the PIDTP (See 38535K, Para H.3.4.4.1).**

Screening Requirements in Draft 38535K Class V vs. Class Y



- **Screening**
 - Same for both V and Y except the differences related to hermeticity vs. non-hermeticity.
- **Column Attached Parts (as offered by Manufacturers)**
 - 100% DC electricals post column attachment (same for V and Y)
 - Visual inspection (same for V and Y)
 - No additional screening requirement for V or Y



The Hubble Space Telescope (HST) is a 2.4-m (7.9-ft) aperture space telescope. It was carried into low Earth orbit by a Space Shuttle in 1990, and it remains in operation.

QCI Requirements in Draft 38535K

Class V vs. Class Y



- **Quality Conformance Inspection (QCI) (Land Grid Array)**
 - **Group A :**
 - **Same for both V and Y**
 - **Group B:**
 - **Same, except hermeticity vs. non-hermeticity differences**
 - **Group C:**
 - **Same**
 - **Group D:**
 - **Same except hermeticity vs. non-hermeticity differences**
 - **Added PIDTP.**
 - ◆ **PIDTP (Flip-chip) and PIDTP (Solder terminations): Same for V and Y**
 - ◆ **PIDTP (Non-hermetic packages): Class Y only**
 - **Group E:**
 - **Same for both V and Y**

- **Column Attached Parts (as offered by Manufacturers)**
 - **Columns shear test**
 - **Group A, Subgroup 1 only:**
 - **Same for V and Y**

Pre and Post Column Attach Data

(Ref: BAE Presentation at Oct. 2012 Class Y meeting)



Electrical Test With or Without Columns

BAE Systems performs burn-in and 3-temp testing without columns

- Post-column attach: BAE Systems performs room temp testing only

CGA Module Test Experiment (requested by Aerospace/NASA)

- 3 RAD750 devices were 3-temp tested without columns (Land Grid Array)
- Columns were attached
- Devices were then re-tested with columns (Column Grid Array)
- All 3 parts passed full Group A test both pre- and post-column
- Test results were compared pre- and post-column

- Comparison of Input-Output Test Parameters shows < 8% deltas between pre- and post- column electrical test:

Parameter	Temp	s/n 2605	s/n 2788	s/n 2829
Input leakage (high voltage) (IIH)	+25C	< 0.5%	< 1%	< 0.5%
	-55C	< 6%	< 1.5%	< 1.5%
	+125C	< 7%	< 7%	< 8%
Input leakage (low voltage) (IIL)	+25C	< 1%	< 1.5%	< 1%
	-55C	< 3%	< 3.5%	< 3.5%
	+125C	< 1.5%	< 2%	< 2%
Voltage Output High (VOH)	+25C	< 0.5%	< 0.5%	< 0.5%
	-55C	< 1%	< 0.5%	< 0.5%
	+125C	< 0.5%	< 0.5%	< 0.5%
Voltage Output Low (VOL)	+25C	< 3.5%	< 7%	< 3.5%
	-55C	< 6% *	< 7%	< 5%
	+125C	< 4%	< 4%	< 3.5%
Dynamic I/O Idd	+25C	< 3%	< 3%	< 3%
	-55C	< 3%	< 3%	< 2.5%
	+125C	< 3%	< 3.2%	< 3%

* except 1 pin at 12%

Xilinx Product Change Notice (PCN)



Virtex-4 and Virtex-5 QV FPGA CF Package Assembly Location Change

XCN13005 (v1.0) February 25, 2013

Product Change Notice

Overview

The purpose of this notification is to communicate that Xilinx is discontinuing the current Virtex[®]-4 and Virtex[®]-5 QV FPGA Ceramic Flip Chip Column Grid Array (CF package code) parts due to current supplier line discontinuance. However, Xilinx will continue to offer Virtex-4 and Virtex-5 QV FPGA Ceramic Flip Chip Land Grid Array products under a new CN package code with a new assembly supplier.

Description

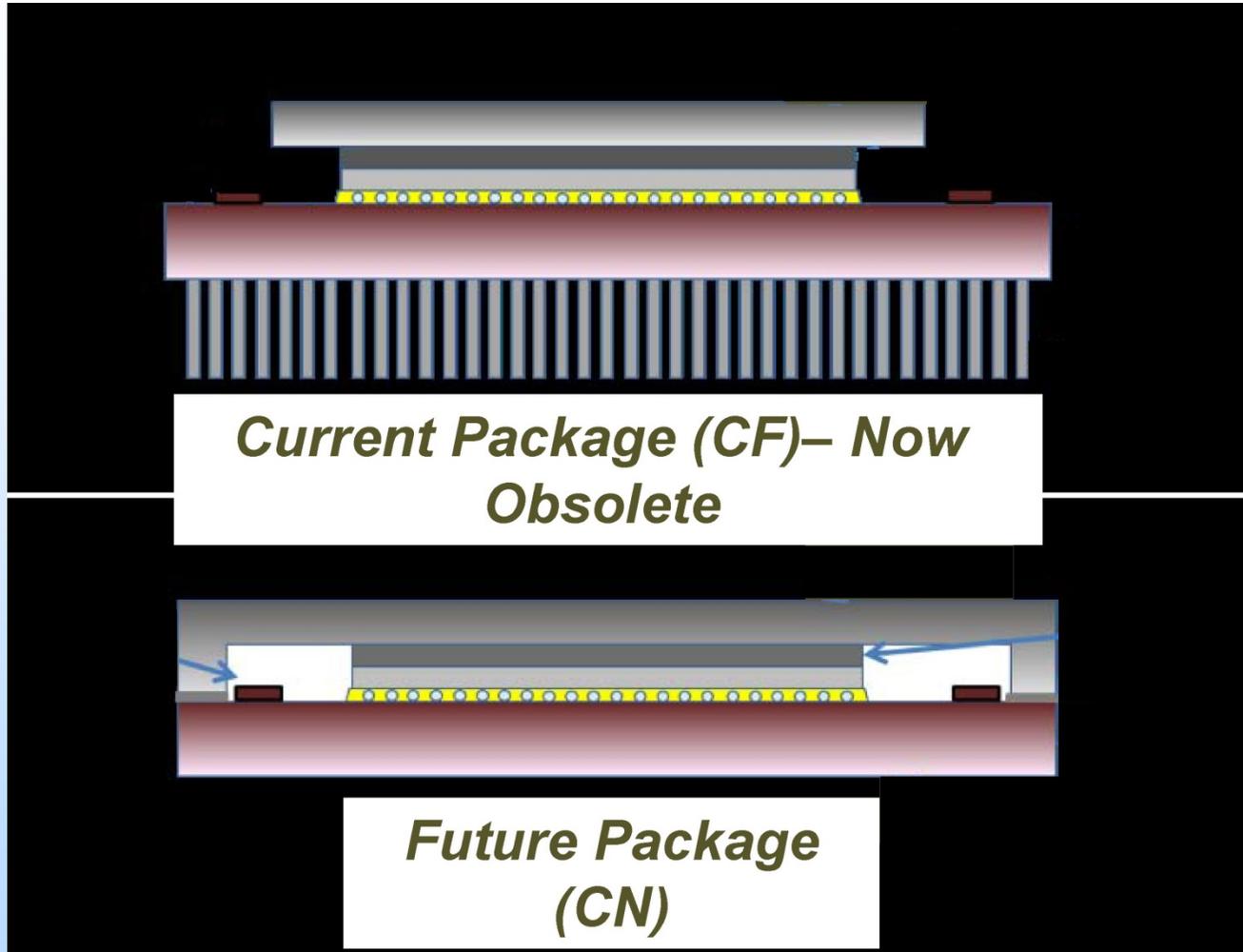
Xilinx's supplier, IBM is shutting down their Ceramic Flip Chip assembly line including column attach of the Ceramic Column Grid Array (CCGA). This line shutdown is impacting our Virtex-4 and Virtex-5 QV FPGA ceramic CF package products. To ensure supply continuity, Xilinx is in the process of qualifying a new supplier with new part numbers released for production in CYQ1, 2014.

Virtex-4 and Virtex-5 FPGA QV Ceramic Flip Chip will be offered in Land Grid Array products (without columns) will be qualified with a new Bill of Material (underfill, lid and lid attach adhesive, eutectic bumps) at the new assembly supplier.

**Final Last Time Buy (LTB) orders are accepted until August 30, 2013.
All orders will be Non-Cancellable, Non-Returnable (NCNR).**

Xilinx PCN

CF to PN Package Change



Xilinx PCN

What Will Change?



- Die bumping will be done by a previously used supplier
- Flip chip and packaging completion will be by a new supplier with extensive flip chip experience
- The new lid is electrically conductive
- The BIGGEST change is the part will only be available as a **Land Grid Array (LGA)**
 - Customer will have to arrange for column attach OR
 - Find a socket that can successfully accommodate 1752 closely-spaced contact points
- Customer remains responsible for post column attach electrical testing

Xilinx PCN

The CF to CN Transition



- **Availability**
 - IBM still operates until Q3 2014.
 - Xilinx last time buy ended August 2013.
- **For Kyocera Qualification**
 - Doing feasibility build and test on representative samples in preparation for qualification builds
 - By the time qualification is completed and the Qualifying Activity (QA) has given approval, the single-event effects immune reconfigurable (Virtex 5QV) CN parts are expected to be available immediately.
- It is planned to have Class Y (non-hermetic space grade) fully incorporated in M38535 in time to allow Xilinx to qualify as part of their overall qualification program.

Issues with Microcircuits Burn-in (BI) Screening



- **BI is the key screening step – the whole industry relies upon burn-in as a critical screening step to weed out product infant mortality.**
- **The same BI circuit is used for life test (reliability assessment)**
- **Our recent audit and specification review work has shown that the microcircuits BI screening requirements as specified are out of date and have multiple interpretations.**
- **Can't burn-in the new high speed devices at or close to their speeds because**
 - **Parts are specified in hundreds of MHz to several GHz**
 - **But, the burn-in equipment is limited to ~ 6MHz**
- **MIL-M-38510 slash sheets used to specify the burn-in circuits. But, the performance specs (SMDs) don't.**
 - **NASA has recommended that the requirement to supply the burn-in circuits at initial qual review be added to MIL-PRF-38535, Appendix H, Para H.3.4.6.**

Issues with Microcircuits Burn-in (BI) Screening



- **Should review the element level burn-in of the microcircuits used in hybrids, such as DC/DC converters, crystal oscillators, and others.**
- **NASA and others brought up these issues at the JC13 meeting and a Task Group was formed to address and provide guidance on these issues. Ref: S. Agarwal presentation at the Space Parts Working Group (SPWG), 2013.**
- **Pool together the expertise in this area**
- **Any updates made to the MIL specs should be based on test data.**
- **A dialog with the burn-in equipment manufacturers would be necessary**
- **Limited test data should be taken by the users**
 - **To validate our understanding of the fundamentals of burn-in**



Monolithic vs. Hybrid Microcircuits and Related Issues

Standard Microcircuits	Monolithics	Hybrids
# Elements	Single	Multiple
Mil Spec	MIL-PRF-38535	MIL-PRF-38534
<p>Changes in Last Few Years: The boundary between monolithics and hybrids has become blurred.</p>		
	Capacitors Inside IC Packages	Single Die Hybrids
Issues: (First Reported by NASA)	Signal Integrity capacitors Used In IC packages	Manufacturers building single die hybrids
Mitigation:	Added capacitor screening requirements In 38535 Spec (Para 3.15)	Encouraging suppliers to also get 38535 Certification (M.S. Kennedy has already received it.)
<p>A New Issue: No MIL capacitors to satisfy the needs of new high-speed, low voltage designs. They are using Commercial BME (Base Metal Electrode) capacitors with unproven space heritage. Affects Class Y.</p>		
BME Used?	Yes, but not tested to 3.15 (Xilinx V-4/V-5 FPGAs, Class Y candidates)	Yes, but meet existing element evaluation requirement which are not as stringent as for 38535.
Mitigation	Evaluate BMEs (NASA, Aerospace, Suppliers, ESA, JAXA) Double Derating ?	Stop use until evaluation done. (Ref: G12 letter to DLA)

Space Component Strategies for Tomorrow

Evaluating the next generation of (Nano) Devices



- The next generation of nanodevices will be built on 450-mm wafers in a 28-nm and smaller feature sizes. This will increase device complexity tremendously.
- As the next-generation nano devices are developed, the candidates for infusion into the military standards should be identified and evaluated.
- The evaluation for reliability would follow the requirements as given in MIL-PRF-38535, Appendix H.
- The radiation hardness evaluation requirements are given in MIL-PRF-38535.
- It is anticipated that most of the new devices would be microcircuits. Such devices should be classified in one of the quality assurance levels as defined in MIL-PRF-38535.
- In case any of the devices is a hybrid circuit, the classifications for those devices should be per the quality assurance levels as defined in MIL-PRF-38534.
- Ref: S. Agarwal, "Infusion of Next-Generation Nano Devices into Military/Space Standards," Advanced Technology Workshop on Packaging Next Generation of Nano Devices, Albany, NY, April 30 – May 1, 2013.

Concluding Remarks



- **The Class Y experiment has shown that it takes a considerable amount of time and effort to infuse new technology into the QML system.**
- **The next step for Class Y would be the release of MIL-PRF-38535, Rev. K.**
- **As the next generation nano devices are developed, the candidates for infusion into the military standards should be identified, and evaluation of those candidates should be started as early as possible.**
- **The military standards should be reviewed on a periodic basis and updated to accommodate the unique features of the new devices.**

Future Challenges



- **Who knows? BUT it will be:**

- Smaller and lighter
- More efficient
- Faster
- Changing continuously
- Desirable BUT perhaps not space-worthy



- **And we need to be:**

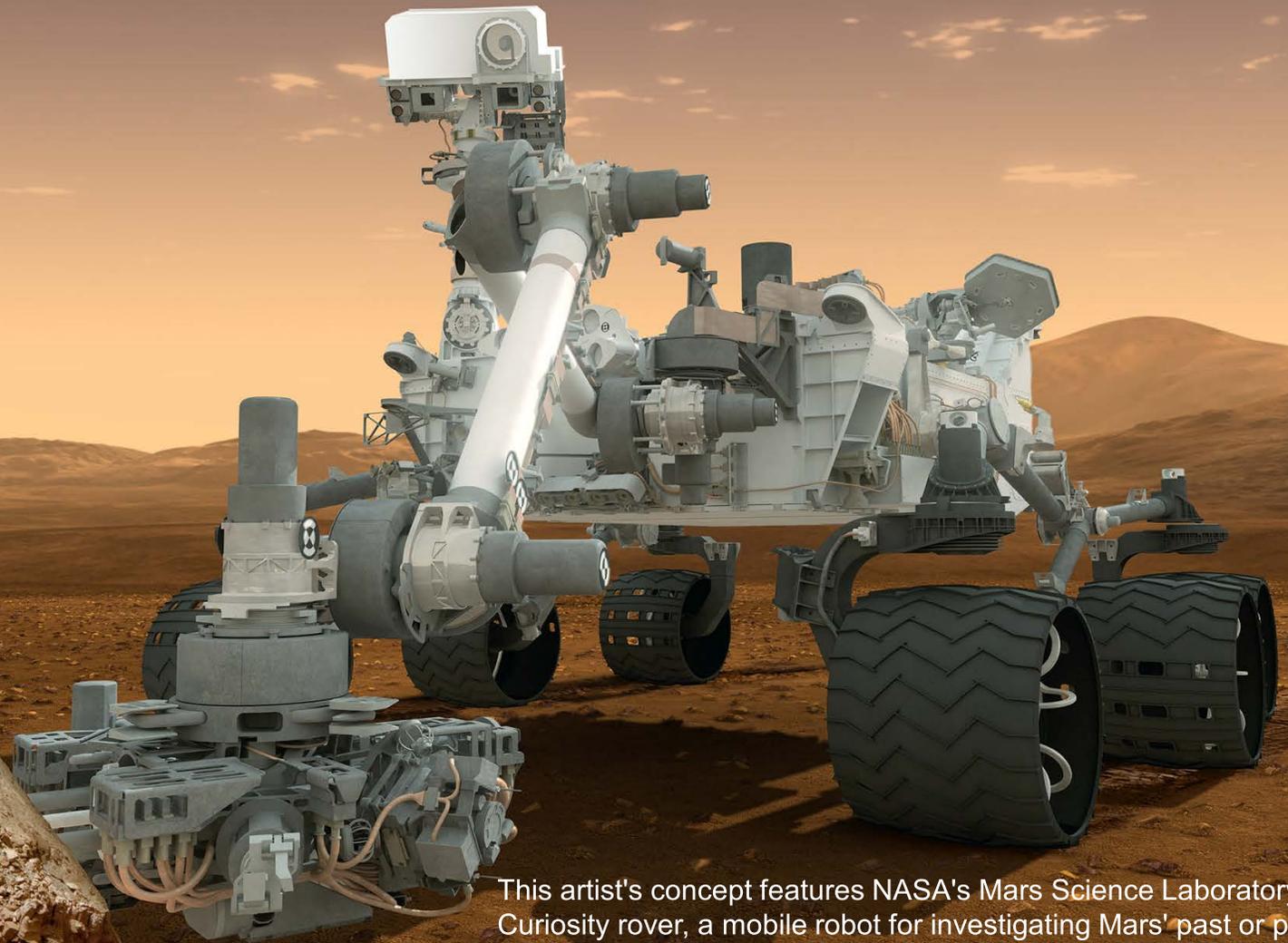
- Flexible and innovative
- Open-minded
- Willing to expand the definition of “part” as integration puts more system levels on a chip or in a package

Business as Usual – JUST EVEN MORE COMPLEX

Mars Science Laboratory (Curiosity rover)

Launched: Nov. 26, 2011

Landed : Aug. 5, 2012



This artist's concept features NASA's Mars Science Laboratory Curiosity rover, a mobile robot for investigating Mars' past or present ability to sustain microbial life. Image credit: NASA/JPL-Caltech

<http://nepp.nasa.gov>



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