Silicon Micromachining for Terahertz Component Development

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Abstract — Waveguide component technology at terahertz frequencies has come of age in recent years. Essential components such as ortho-mode transducers (OMT), quadrature hybrids, filters, and others for high performance system development were either impossible to build or too difficult to fabricate with traditional machining techniques. With micromachining of silicon wafers coated with sputtered gold it is now possible to fabricate and test these waveguide components. Using a highly optimized Deep Reactive Ion Etching (DRIE) process, we are now able to fabricate silicon micromachined waveguide structures working beyond 1 THz. In this paper, we describe in detail our approach of design, fabrication, and measurement of silicon micromachined waveguide components and report the results of a 1 THz canonical E-plane filter.

Index Terms — Filter, terahertz, silicon, micromachine, DRIE.

I. Introduction

Instruments at terahertz frequencies have made significant progress over the last several years. Their usage is now not primarily restricted to science applications from air-borne or space-based platforms. Very high speed-data rate communications [1], stand-off imaging of human-borne concealed contrabands [2], and early detection of skin cancer [3] is now a distinct possibility. With availability of silicon based devices with cut-off frequencies at the submillimeter-waves, it is now a real possibility of integrated instruments working near terahertz frequencies [4]. However, lack of available output power and detection sensitivity of silicon devices limit their usage as high performance instruments, which is the primary need in areas such as astrophysics, planetary science, and Earth sciences. GaAs and InP devices provide the required power for terahertz instruments [5], however, a high level of on-chip integration has remained a big challenge with these devices. In general, these semiconductor devices are assembled in metal-machined waveguide housings to provide low-loss integration,but this approach is not practical for multi-pixel instrumentation for imaging or communication applications. One alternative technique which is gaining ground in recent years is micromachined and gold coated silicon waveguides which uses precise photo-lithographic techniques achieving high precision, small feature sizes, and excellent tolerances [6].

Since silicon micromachining techniques is useful for building multi-pixel receivers at terahertz frequencies, it is important to consider the specific architecture for the receiver design. In a two-dimensional integration approach, instead of making individual waveguide components in separate blocks with traditional metal machining and then cascaded them to build up the instrument, multiple components are integrated on the same block to have high level of integration. This has been successfully demonstrated at terahertz frequencies with normal metal blocks as well as with silicon micromachining techniques [7]. One of the key difficulties with this design architecture, specifically with silicon micromachined blocks, is that the optical coupling elements such as horn antennas need to be assembled with the receivers laterally. This drives the system design parameters for the multi-pixel array such as how closely the pixels can be packed at the focal plane. The required minimum pixel separation is determined by a couple of factors such as the f/D ratio of the antenna optics, where f is the focal length of the antenna and D is the diameter, operating wavelength λ_0; and the type of focal plane sampling used – single sampling where the beams have a 3-dB cross over or the double sampling and its variations (twice the single sampling distance). Moreover, it has been a challenge to cascade different silicon micromachined waveguide components in a lateral configuration due to alignment tolerances and interface issues.

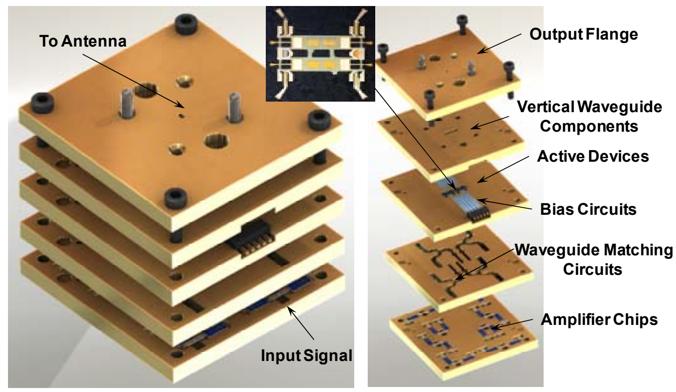

Fig. 1: (Left) Vertical stacking of silicon micromachined components leading to multi-pixel terahertz receiver systems. (Right) Exploded view of different layers of the integrated system.

On the other hand, in a three-dimensional (3-D) integration, the active and passive components are assembled with micromachined waveguides fabricated on silicon wafers in a vertically stacked configuration. Since the integration of the different front-end receiver components are done in a vertical architecture, this leads more naturally to multi-pixel array architecture. Fig. 1 shows the schematic of such a architecture where the essential heterodyne components such as frequency multipliers and mixers are integrated on a single silicon layer but couples to other components from different layers to form the terahertz receiver front-end. One of the major advantages of such a configuration is that we can have low frequency circuit elements in one layer which can couple through a vertical waveguide to the next layer where high frequency circuit elements can be assembled. This modular approach is very effective in designing multi-pixel terahertz receivers. The key to this configuration is the silicon micromachined waveguide housing as this cannot be accomplished with metal machined waveguides at terahertz frequencies.

In this paper, we present our approach of using silicon micromachining to fabricate terahertz waveguide components by utilizing deep reactive ion etching (DRIE) process. Specifically, we report an E-plane canonical filter designed, fabricated, and tested at 1 THz.

II. Silicon Micromachining

In conventional approaches, terahertz receiver components are fabricated using CNC milling machines using metal waveguide blocks. However, they are too massive and expensive for multi-pixel instruments. Moreover, as the frequency of operation goes beyond 1 THz, the feature sizes and tolerances required are too demanding. These metal blocks also incur higher losses as they need to be cascaded in a serial fashion to build up the instrument. Novel ultra-compact receiver architectures are needed to reduce loss as well as the mass and size of the receiver while increasing the circuit density of the device.

One approach for fabricating highly integrated and compact terahertz front-end components is to make all the waveguide components on silicon with sputtered gold where the power amplifiers, multipliers, and mixer chips can be integrated in a single silicon micromachined block, shown schematically in Fig. 1.

There are several different micromachining techniques one can use for fabrication of terahertz waveguide circuits. One process forms the waveguide and device structures directly from permanent resists such as SU-8 [8], [9]. This technique, while requiring a minimum of processing tools, suffers from significant process instabilities and delamination issues between the thick resist and carrier wafer. Moreover, SU-8 processes are very challenging to stabilize and the layer thickness is difficult to deposit uniformly, reducing the precision of each layer thickness or requiring an additional processing step such as lapping of each layer.

LIGA-based processes use thick resists forming a mold for electroplating [10]. This has the advantage of producing a metal structure and is therefore easier to couple to standard metal waveguide components. LIGA process also suffers from non-uniformity issues that require an additional processing step, such as lapping, to planarize the final device. Moreover, in LIGA processes electroplating a flat layer tens to hundreds of microns thick is very difficult. Similar problem persists in the PolyStrata sequential copper deposition process where the structural material is copper, which is grown after a photoresist is deposited to define the waveguide walls [11].

In silicon micromachining, silicon is removed with a laser (in laser micromachining) or with plasma (in deep reactive ion etching). Laser micromaching is a time consuming process as silicon atoms need to be removed layer by layer. On the other hand, silicon micromachining utilizing DRIE process removes silicon material with fluorine ion plasma. Generally, DRIE struggles to maintain straight sidewalls and as well as a uniform depth across the wafer for each etch depth.

Despite the progress made in the development of the various fabrication processes of micromachined components, there are other problem areas which hinder development of waveguide components at these frequencies. One such area is the lack of effective methods of characterizing circuits. Specifically, coupling between the micromachined waveguide and standard waveguide flanges suffers from misalignment problems due to the difficulty in aligning to non-metal machined waveguide components. Precision alignment between different wafer layers is a great challenge as well.

In our laboratory, we utilize silicon DRIE, a technique that we believe offers a wider range of possibilities in terms of structures, designs, and better resolutions. DRIE of bulk silicon wafers is a relatively well-established fabrication technique capable of etching high aspect ratio features [12]. We also developed a method where deep trenches with vertical side walls can be fabricated with DRIE [13].

A. Fabrication Using DRIE

Deep reactive ion etching (DRIE) of bulk silicon wafers is a relatively well-established fabrication process capable of etching high aspect ratio features [14]. It uses the Bosch process based on the alternative exposures to SF_6 and C_4F_8 gases; the SF_6 is used to etch the silicon, while the C_4F_8 passivates the etched surfaces [15]. Since the technique primarily removes materials based on etching, it struggles to maintain straight sidewalls; uniform depths across the wafer for each etch depth, and smooth etched patterns. All these are critical parameters for the fabrication of terahertz waveguide components and intensive work has been performed in our group and elsewhere to improve the process.

Initially, when we started silicon DRIE using Bosch process, we used AZ9260 and AZ5214 photoresists (PR) and UV photolithography defined patterns to test the various etch process parameters. However, the majority of circuit components at terahertz frequencies require multiple etch depths and the use of these so called “soft” masks are known to be inadequate because of non-uniformity issues during spin-coating of photoresist, especially at the edge of the microstructures. Another problem with soft mask process is that the etch selectivity between the photoresist and the silicon which is not sufficient for etching through the entire thickness of the wafer. Due to the low selectivity, it requires thicker photoresist etch mask which results in degradation of microstructure precision. To overcome these, we decided to use additional masks, so called "hard masks", using silicon dioxide (SiO_2) which addresses many of these shortcomings. For our fabrications, we used this new technique.

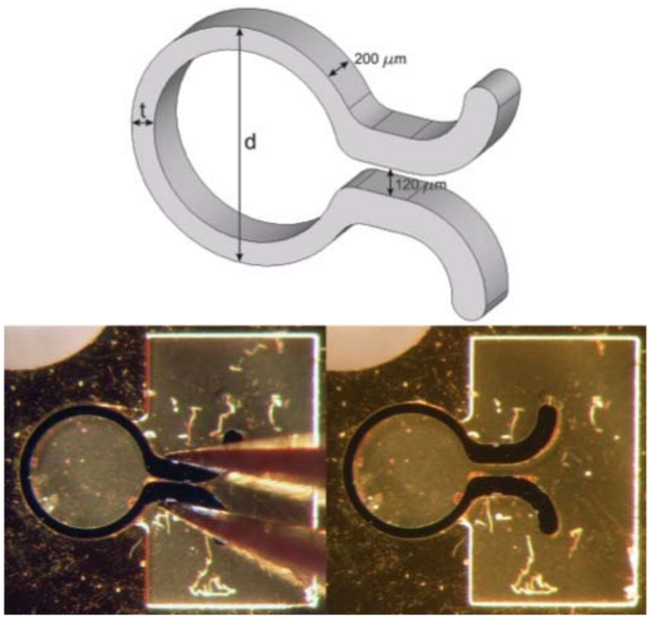

Fig. 2: A schematic diagram of the silicon compression pin showing the relevant dimensions (top). Photograph showing the compression pin during assembly squeezed by the tweezers to insert it into the alignment pocket (bottom left). Photograph of the compression pin released into the alignment pocket (bottom right) [6].

B. Assembly and Alignment of Micromachined Components

One of the key aspects which prevented silicon micromachining to be ubiquitous at terahertz frequencies is the difficulty to align the silicon pieces. In metal machined parts, metal pins in somewhat undersized holes are pushed in and that is used for alignment purposes. It has been very successful because in metal, the pins push materials out to achieve a very tight fitting which allows good tolerances for alignments. On the other hand, silicon is brittle and cracks when metal pins are used in tight openings. If somewhat larger openings are used, it becomes impossible to get the required alignment tolerances at these frequencies. Moreover, when the two split-halves of a machined terahertz component are mated, the metal block might be scratched or dented by the alignment pin but silicon will crack, often destroying the wafer.

To address this issue, we came up with a novel silicon compression pin based alignment process that has been found to work very well. Since the primary source of misalignment when using either metal or silicon pins for silicon micromachined pieces is the slop required to insert the pin into the pocket, a compliant silicon pin which is fabricated using the same fabrication process as that of silicon wafer, resolves those issues. Fig. 2 shows the schematic picture of the compression alignment pin along with a photograph of the pin when it is compressed with tweezers to fit into the alignment pocket. When released, the pin expands to fill the pocket. A tight fit is ensured by choosing the relaxed pin diameter to be greater than the pocket diameter. The spring constant of the pin is controlled by the thickness of the ring and must be designed to allow sufficient compression during assembly while generating as much force as possible to preserve the alignment between the two wafers [6].

III. Measurement and Results

We designed and fabricated a canonical bandpass filter working in the 1 THz frequency band. The canonical filters are based on direct coupled synchronous resonant circuits. This particular design was directly scaled from our previous work at WR 1.5 waveguide band [16].

The filter was fabricated using DRIE process described above. The filter is split at the middle of the rectangular waveguide into two equal halves with the same depth. Each of

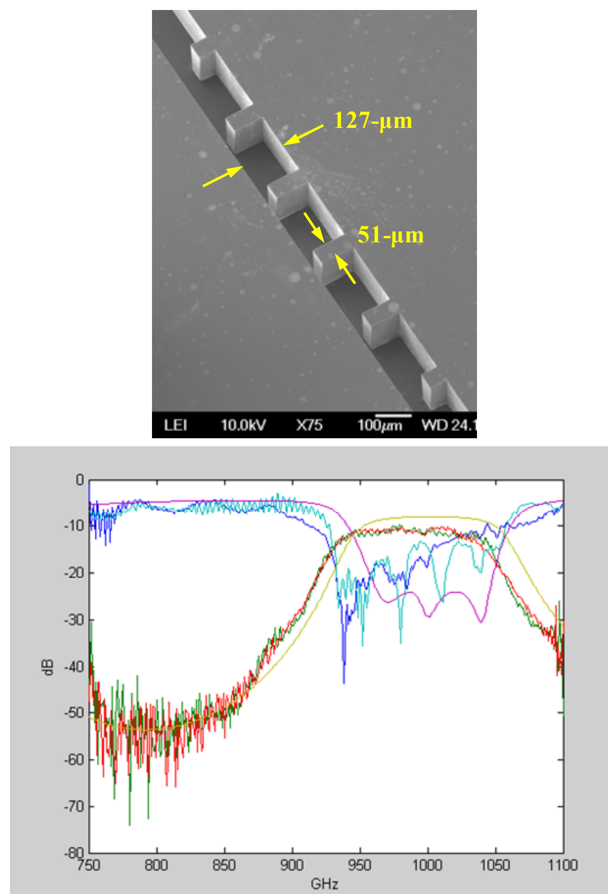

Fig. 3: SEM image of the E-plane canonical filter. The dimensions of the input rectangular waveguide are 254 x 127 µm. (top). S-parameters of the filter measured with a VNA. The yellow and magenta plots are simulated results and it can be seen that the measured results down-shifted by approximately 20 GHz.

the halves is sputtered with 2µm of gold. Once the pieces are metalized and released, the waveguide filter circuit is assembled with the silicon compression pins. We were able to achieve better than 1-µm alignment using these Ω-shaped compression pins. The measurements were carried out with Agilent PNA-X vector network analyzer (VNA) with Virginia Diodes Inc. (VDI) WR-1 frequency extenders and we used TRL calibration method for the measurements.

Fig. 3 shows a SEM photograph of the fabricated silicon micromachined filter before gold was sputtered on them. Fig. 3 (bottom) shows the measured results. We also plotted our simulation results for the filter on the same plot to comparison. It can be noticed that the measured results match very well with the simulated predictions except for approximately 2% (20 GHz) down-shift in frequency. It can also be seen that we measured approximately 1-dB of extra transmission loss compared to simulation. We noticed from the SEM photograph of the canonical filter is that the silicon posts has a slight tapering. From our experience detailed in [16], we believe that the frequency shift arises due to this tapering of the posts. Also, the extra loss could possibly be due to the gap between the silicon piece and the flange of the measurement equipment. To the best of our knowledge, this is the highest frequency silicon micromachined component fabricated with DRIE techniques and measured independently (as opposed to in a system along with other components where the performance of the component cannot be directly verified) using a vector network analyzer.

IV. Conclusion

Amongst various micro-fabrication techniques used to fabricate waveguide components at terahertz frequencies, we believe that DRIE based silicon micromachining provides the best possible solution. Using optimized Bosch process to achieve deep vertical etch and multiple etch depths, we are able to fabricate components in terahertz frequencies that can be easily integrated to design multi-pixel arrays. As a proof of concept, we designed, fabricated, and tested a canonical E-plane filter working in the 1 THz frequency band. The measured performance of the filter resembles closely with the simulated predictions. To the best of our knowledge, this is the highest frequency silicon micromachined waveguide component ever tested individually for its performance evaluation.

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