Jet Propulsion Laboratory
California Institute of Technology

Next Generation Space Processor (NGSP)
High Performance Spaceflight Computing (HPSC)
Next Steps at NASA and AFRL

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6th Meeting on
Fault-Tolerant Spaceborne Computing Employing New Technologies
Sandia National Laboratories

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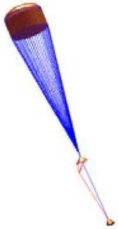
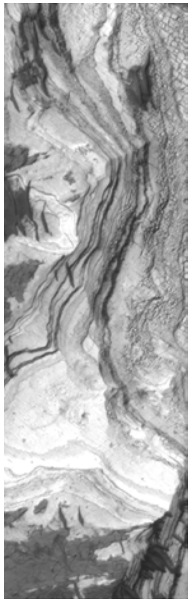
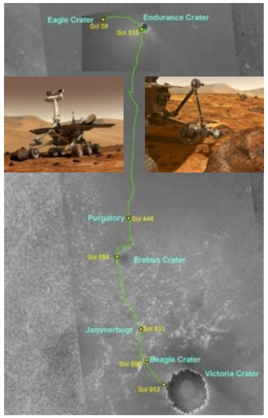
The NASA Need

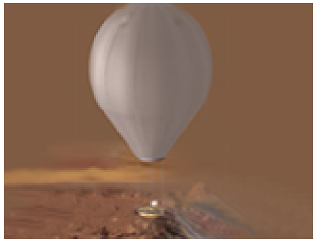
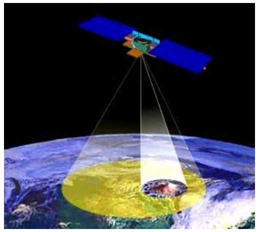
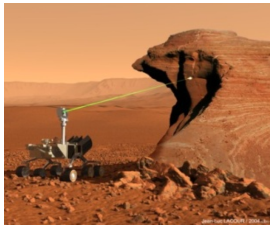
There are important mission scenarios that today cannot be accomplished robustly and cost-effectively

- Space-based computing has not kept up with the needs of current and future NASA missions
- Government and industry are developing high-performance space-qualifiable processors
- NASA continues to have unique requirements
  - Deep space, long duration, robotic and human missions
  - Higher performance, smaller spacecraft and lower cost
    - Onboard science data processing
    - Autonomous operations and greater resilience
  - Extreme needs for low power and energy management, efficiency, fault tolerance and resilience

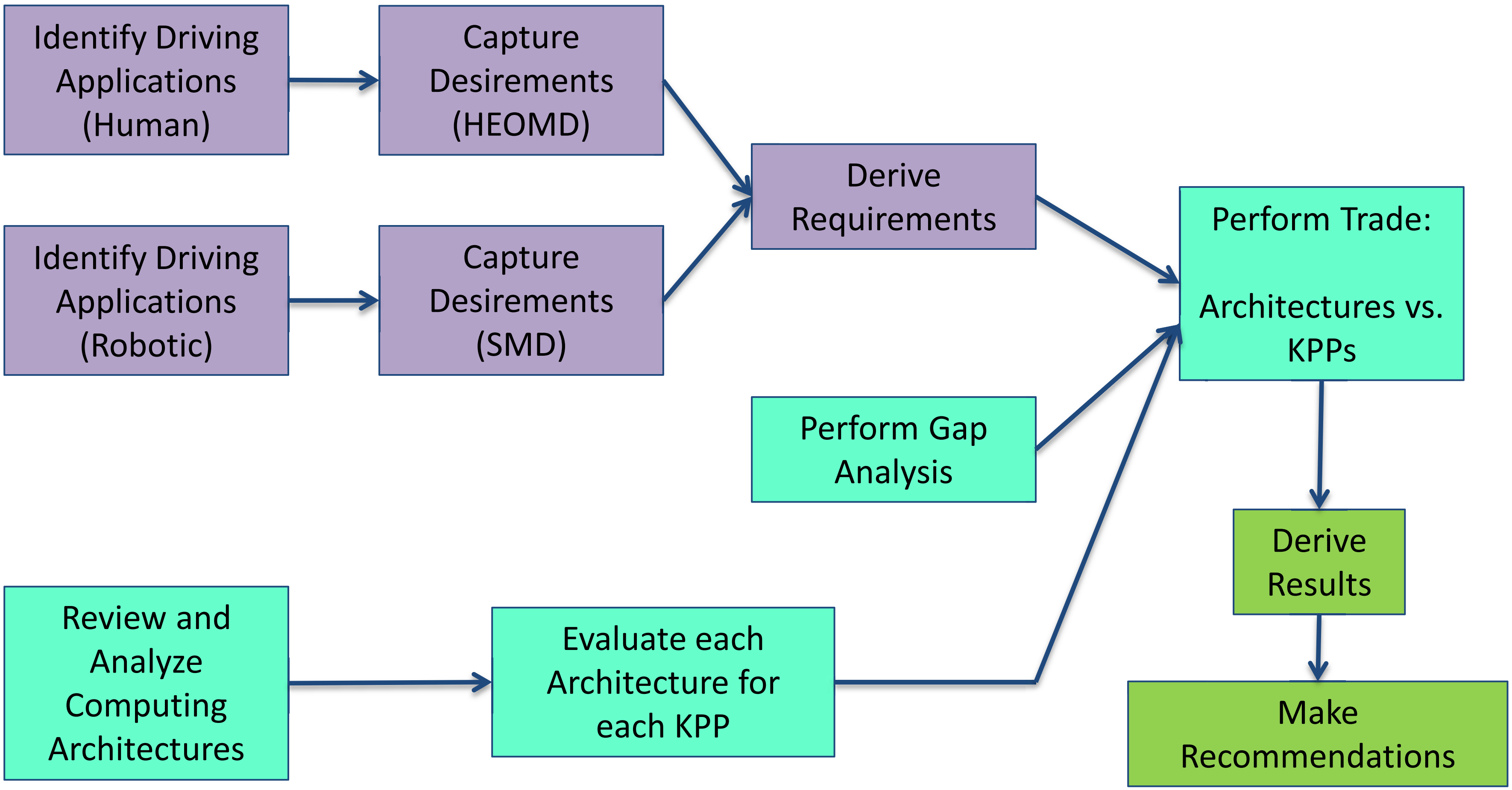




NASA Space Technology Proposal Result

Authorization of HPSC Program Formulation under GCDP



HPSC Formulation Phase Study Summary

GP multi/many-core provides optimum ROI for NASA

The Assignment	The Results
Identify relevant NASA use cases What are the paradigm-shifting NASA space-based applications that will drive next generation flight computing?	Developed 9 human spaceflight (HEOMD) and 10 science mission (SMD) use cases for future flight computing, spanning critical mission functions, high data rate instruments, and autonomy utilizing model-based reasoning techniques
Derive requirements What are the future onboard computing requirements?	100X performance increase, low power (down to 7W) with scaling, support for a range of fault tolerance, common programming languages, avoidance of additional V&V effort, interoperable with co-processors
Perform a gap analysis How/where do commercial and defense industry developments in computing fall short of NASA's unique requirements and architectural needs?	No existing or emerging spaceflight processors possess all necessary performance, power efficiency, reliability, and programmability attributes
Trade architectures against defined Key Performance Parameters (KPPs) Which computing architecture will make the most difference?	Rad-hard general-purpose multi-core best addresses the future flight computing requirements and presents the most affordable gap against the KPPs
Make a recommendation How can NASA best invest limited resources to meet the future needs of its space systems?	Competed/directed program plan for rad-hard general-purpose multi-core, with solutions for power/energy, fault tolerance and other NASA requirements, leveraging other agency and industry investments

Study specifics in following charts

NASA Applications

for High Performance Spaceflight Computing

HEOMD Use Cases

1. Cloud Services
2. Advanced Vehicle Health Management
3. Crew Knowledge Augmentation Systems
4. Improved Displays and Controls
5. Augmented Reality for Recognition and Cataloging
6. Tele-Presence
7. Autonomous & Tele-Robotic Construction
8. Automated Guidance, Navigation, and Control (GNC)
9. Human Movement Assist

SMD Use Cases

1. Extreme Terrain Landing
2. Proximity Operations / Formation Flying
3. Fast Traverse
4. New Surface Mobility Methods
5. Imaging Spectrometers
6. Radar
7. Low Latency Products for Disaster Response
8. Space Weather
9. Science Event Detection and Response
10. Immersive Environments for Science Ops / Outreach

High value and mission critical applications identified by NASA scientists and engineers

Science Mission Applications

10X improvement for existing applications

Enables new science and mission capabilities on future missions

SMD Use Cases

1. **Extreme Terrain Landing**
2. Proximity Operations / Formation Flying
3. **Fast Traverse**
4. New Surface Mobility Methods
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7. Low Latency Products for Disaster Response
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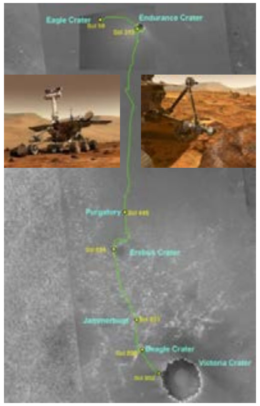
10. Immersive Environments for Science Ops / Outreach

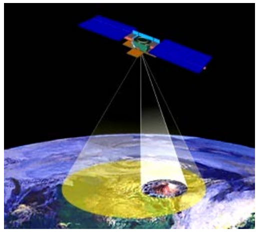
Benefits to Missions

- **Extreme Terrain Landing**

  - Enables reliable and safe landing in hazardous terrain: TRN and HDA algorithms benchmarked by Mars Program - required six (6) dedicated RAD750s



- **Fast Traverse**
  - Remove computation as a limiting factor to mobility – drive 10X faster and more, safely (wheel slip, obstacle detection)
- **Science Event Detection and Response**



  - Increase capture rate for dynamic, transient events from ~10% to >75%, with <5% false positives, for increased and more timely science return

No longer need to size science / mission scope to flight computing capability

Human Spaceflight Mission Applications

Enable autonomous human-assist capabilities in next generation crewed vehicles and missions

HEOMD Use Cases

1. Cloud Services
2. **Advanced Vehicle Health Management**
3. Crew Knowledge Augmentation Systems
4. Improved Displays and Controls
5. Augmented Reality for Recognition and Cataloging
6. Tele-Presence
7. **Autonomous & Tele-Robotic Construction**
8. **Automated Guidance, Navigation, and Control (GNC)**
9. Human Movement Assist

Benefits to Missions

- **Vehicle Health Management**
  - Continuous monitoring/analysis of large vehicle data sets: problem detection and response, crew workload reduction, and improved vehicle maintenance during untended operations

- **Crew / Robot Interaction**
  - Robots respond to high-level instructions from crew or ground personnel while maintaining safe operations and interactions with the crew

- **Automated GNC**
  - Move compute-intensive GNC applications onboard for faster, safer docking; close proximity operations; collision avoidance; and automated precision landing within an affordable power/propulsion budget

No longer need to size science / mission scope to flight computing capability

NASA Flight Computing High-Level Requirements

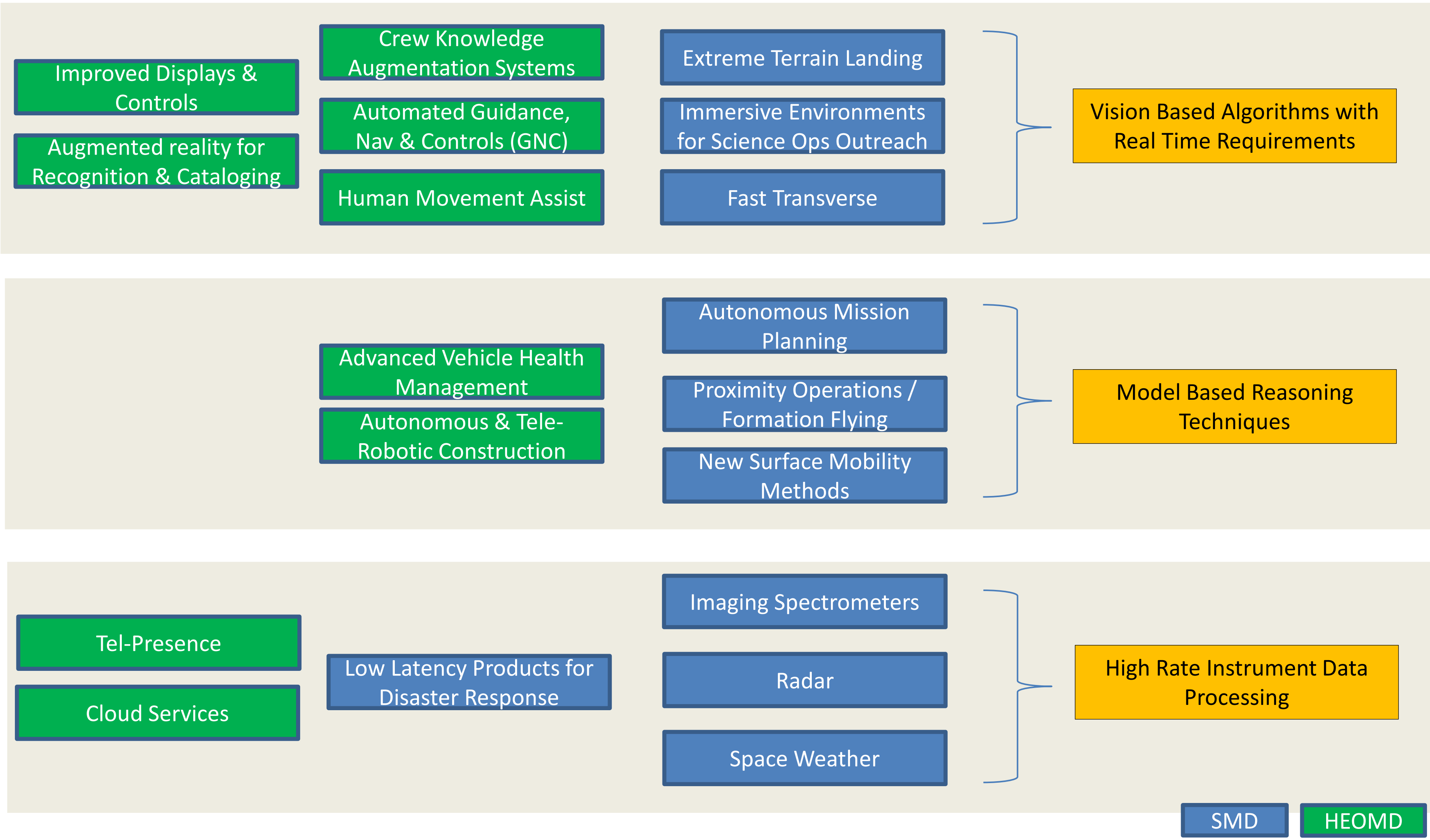
as derived from the NASA use cases

Computation Category	Mission Need	Objective of Computation	Flight Architecture Attribute	Processor Type and Requirements
Vision-based Algorithms with Real-Time Requirements	• Terrain Relative Navigation (TRN) • Hazard Avoidance • Entry, Descent & Landing (EDL) • Pinpoint Landing	• Conduct safe proximity operations around primitive bodies • Land safely and accurately • Achieve robust results within available timeframe as input to control decisions	• Severe fault tolerance and real-time requirements • Fail-operational • High peak power needs	**• Hard real time / mission critical** **• Continuous digital signal processing (DSP) + sequential control processing (fault protection)** **• High I/O rate** **• Irregular memory use** **• General-purpose (GP) processor (10's – 100's GFLOPS) + high I/O rate, augmented by co-processor(s)**
Model-Based Reasoning Techniques for Autonomy	• Mission planning, scheduling & resource management • Fault management in uncertain environments	• Contingency planning to mitigate execution failures • Detect, diagnose and recover from faults	• High computational complexity • Graceful degradation • Memory usage (data movement) impacts energy management	**• Soft real time / critical** **• Heuristic search, data base operations, Bayesian inference** **• Extreme intensive & irregular memory use (multi-GB/s)** **• > 1GOPS GP processor arrays with low latency interconnect**
High Rate Instrument Data Processing	High resolution sensors, e.g., SAR, Hyper-spectral	• Downlink images and products rather than raw data • Opportunistic science	• Distributed, dedicated processors at sensors • Less stringent fault tolerance	**• Soft real time** **• DSP/Vector processing with 10-100's GOPS (high data flow)** **• GP array (10-100's GFLOPS) required for feature ID / triage**

Future NASA use cases require dramatic improvement over RAD750 (~200 MOPS)

Mapping of Use Cases

to the Computation Categories



Eigen-Apps Summary

~60 application variants/derivatives reduced to 10 representative sets of requirements

App to Eigen-App Mapping	DSP	GP	P	Mission Critical	LP
Throughput = 1-10 GOPS					
Autonomous Mission Planning		X	X	X	X
Disaster Response	X	X			X
Hyspiri	X	X	X		
Throughput = 10-50 GOPS					
Fast Traverse	X	X	X	X	X
Extreme Terrain Landing	X	X	X	X	X
Adept		X	X		
Optimum Observation	X	X	X		X
Space Weather	X		X		X
Robotic Servicing	X	X	X	X	
Cloud Service	X	X	X		
Advanced ISHM		X	X		X
Autonomous and Telerobotic Construction		X	X	X	X
Througput = 50-100s GOPS					
Hyperspectral Imaging	X	X	X		X
RADAR Science	X	X	X		
RADAR EDL	X		X	X	X
Automated GN&C	X	X	X	X	
Human Movement Assist	X	X	X		X
Crew Knowledge Augmentation		X	X		
Improved Displays and Controls		X	X	X	X
Augmented Reality		X	X		X
Telepresence		X	X		X

- Requirements that represent groups of key cross cutting applications
- Derived by selecting low power applications from full applications set and grouping by throughput, processing type, mission criticality

Eigen-App	Throughput	DSP	GP	P	LP	MC
1	1-10 GOPS	X	X	X	X	
2	1-10 GOPS		X	X	X	X
3	10-50 GOPS	X	X	X	X	X
4	10-50 GOPS	X	X	X	X	
5	10-50 GOPS		X	X	X	X
6	10-50 GOPS		X	X	X	
7	50-100 GOPS	X	X	X	X	X
8	50-100 GOPS	X	X	X	X	
9	50-100 GOPS		X	X	X	X
10	50-100 GOPS		X	X	X	

KEY

- DSP – Digital Signal Processing
- GP – General Purpose Processing
- P – Parallelizable
- Mission Critical – Requires Additional Fault Tolerance
- LP – Max Power Available for Processor Chip <6W

Computing Architectures

Candidates evaluated under the HPSC task

- **General-purpose multi-core**
  - Rad-hardened
  - COTS
- **DSP multi-core**
  - Rad-hardened
  - COTS
- **Reconfigurable computing (e.g., FPGAs)**
  - Rad-hardened
  - COTS
- **Graphics processing units (GPUs)**
  - Rad-hardened
  - COTS
- Also: **Hybrid Architectures utilizing Co-Processors**
  - General Purpose Multicore + Reconfigurable Computing
  - General Purpose Multicore + GPU
  - General Purpose Multicore + DSP Multicore

Key Performance Parameters

Application-referenced KPPs

- Computational performance
- Radiation and fault tolerance
- Power and energy management
- Software verfication and validation

Architecture-referenced KPPs

- Software verification and validation (this is the single cross-over KPP)
- Programmability and flight software applicability
- Interoperability
- Extensibility and evolveability

Additional KPPs

- Non-recurring cost
- Recurring cost
- Cross-cutting applicability across the NASA mission set

Other Considerations

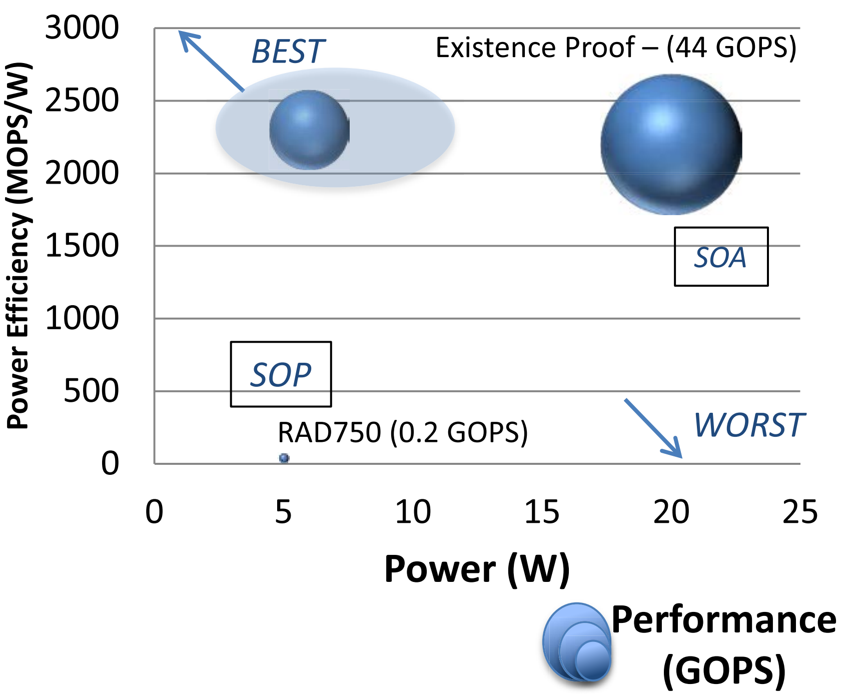
TRL 5-6 in 3 years within available budget

Study Recommendation

Rad-hard General Purpose Multi-core

Rad-hard General Purpose Multicore

- **Best overall fit to application requirements** – provides both general purpose and some DSP capability as well as interoperability with co-processors (DSP, Reconfigurable)
- **Conducive to Power Scaling at core-level**
  - **Power Dissipation** issues to address fit within available investment resource envelope
- **Conducive to thread-based Fault Tolerance**
  - Fault detection/correction/isolation
  - Ability to segregate failed cores from the pool of available cores in support of graceful degradation
- **Scalable to 10x increase in the number of cores**
  - Combined with Power Scaling, allows the increased cores to consume power only as thread-load dictates



Computational Performance, Efficiency, and Scalability of Multi-core redefines general-purpose computing for space systems

HPSC Formulation Task Recommendations

Investment Focus and Approach

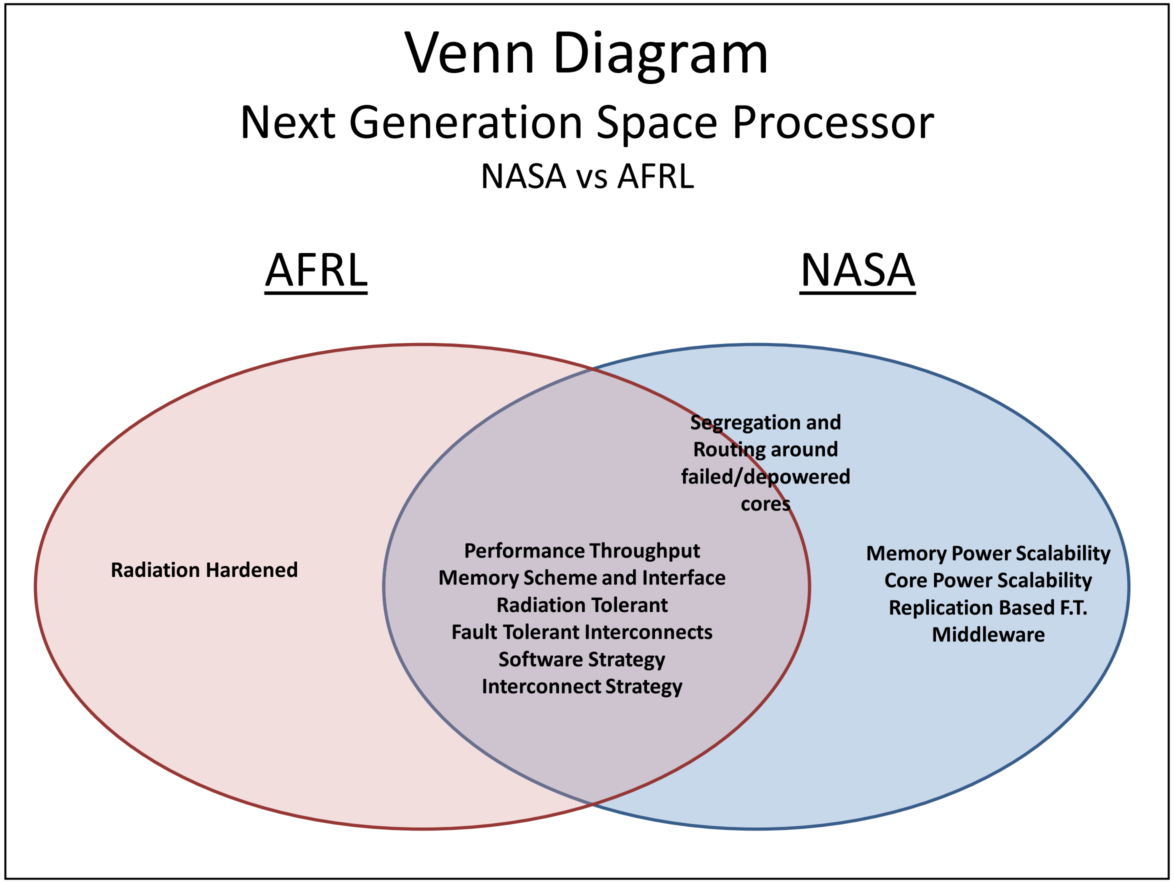
- Focus on **Rad-hard General Purpose Multi-core**
  - Leverage government and industry investments
- Issue a BAA for hardware in FY13
  - Solicit flight computing system concepts
  - Prepare NASA requirements and benchmarks for early evaluation of architectures
  - Include a competitive **Phase 0**, seeking innovative solutions and early risk retirement
- Include a directed software investment
  - Middleware elements for allocating/managing cores for varying operational objectives, working closely with the FSW community, driven by knowledge of the NASA applications
- Product of the investment
  - Multi-core hardware chip with bundled real-time operating system (RTOS), FSW development environment, and middleware elements, integrated on evaluation board

Challenge the community to develop an innovative, extremely high performance, low power, flexible, rad-hard GP multi-core processor within available budget and schedule

Enter AFRL!

Next-Generation Spaceflight Processor (NGSP)

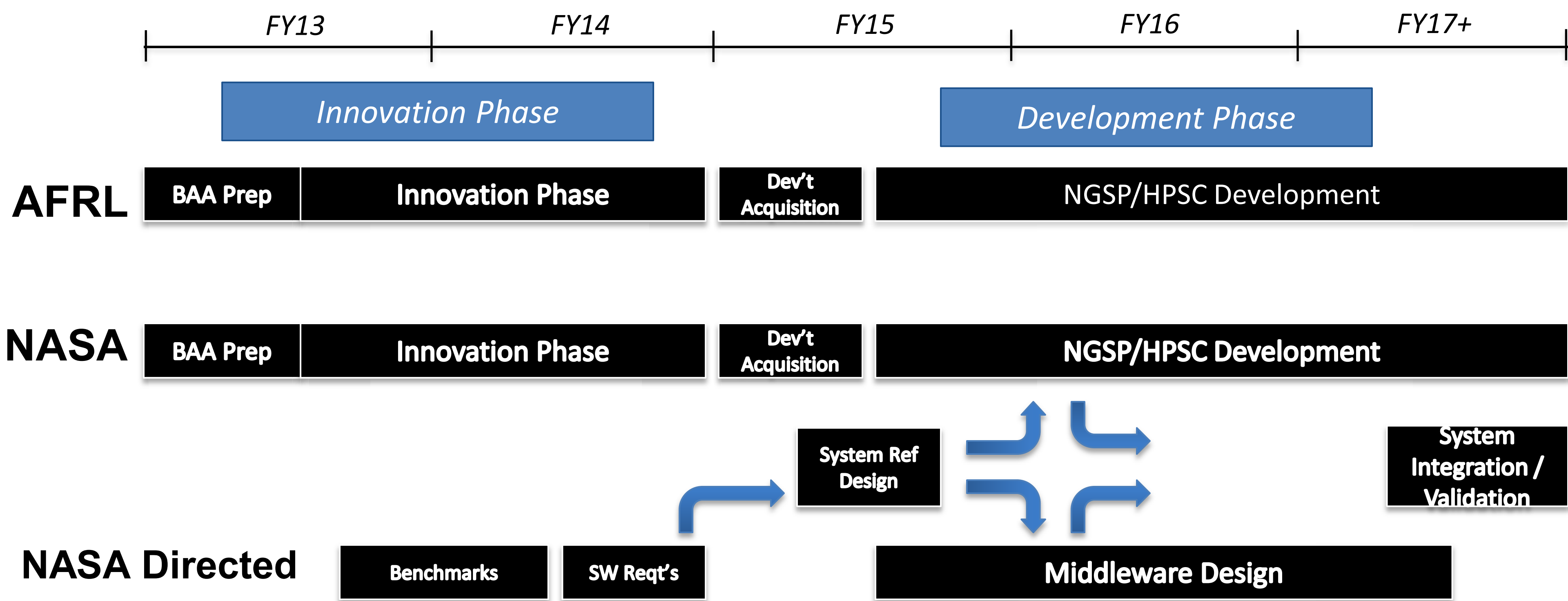
AFRL vs. NASA Requirements



There was sufficient common ground to justify a joint AFRL-NASA program

NGSP / HPSC Program

Joint NASA-AFRL program to develop a
High Performance Next Generation Spaceflight Computing Processor



Initial Joint Program Plan approved and funding allocated for Innovation Phase
BAA Issued and Benchmark Development initiated

NGSP / HPSC Program

Innovation Phase BAA – Top Level Objectives Summary

- 24 Cores providing 20 GOPS/10GFLOPS, multiple 10Gb/s I/O and DDR 3 Memory Ports at 7 Watts
- Dynamically power scalable at core level granularity by powering and depowering cores in real time without disrupting system operation, with very low idle power load (<<1W)
- Provides fault tolerant interconnects between cores and to external I/O and memory devices
- Natively supports multi-level replication based fault tolerance, e.g., N-Modular Redundancy where N=2, 3
- Supports segregation and routing around failed and depowered cores
- Radiation tolerant to at least 300kRad TID, Latch-up Immune, with Single Event Upset (SEU) rate of not greater than TBD/day in Adams 90% worst case GEO environment
- Interoperable with other high performance computing architectures, e.g., reconfigurable computing FPGAs
- System software and application development environment

*****Proposers encouraged to offer alternatives *****

AFRL BAA-RVKV-2013-02
Proposal Due Date 5/29/13

NGSP / HPSC Program

Innovation Phase – Top Level Summary of Desired Deliverables

- Identification of process and/or RHBD library to be used, along with test data to substantiate claims of radiation hardness
  - RHBD technology with test data showing TID tolerance to 300kral, SEL immunity to 70MeV
- Simulation/model results for a set of NASA-defined benchmarks (FFT, search algorithms, etc.)
  - Performance thresholds will be specific to each benchmark
- Simulate/model results of fault response and power management
  - Demonstrated ability to operate through faults and restore correct operation
  - Demonstrated ability to dynamically manage power under software control
- Management/Development plan that makes a credible case that TRL 5-6 can be achieved within BAA cost and schedule constraints
  - List of IP to be used, and agreements in place to acquire if selected
  - Detailed work breakdown structure provided to at least 3 levels
  - Complete device development schedule (including margin)
  - Detailed development cost estimate (including reserves)
  - Risks identified and risk management approach provided

AFRL BAA-RVKV-2013-02
Proposal Due Date 5/29/13

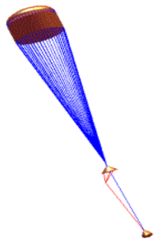
AFRL / NASA BAA

Status and FY13-14 Plans

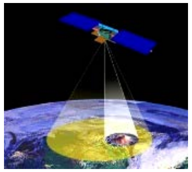
- **April 2013**: AFRL/NASA BAA posted
  - Next-Generation Space Processor BAA-RVKV-2013-02
- **May 2013:** Proposals due
- **August 2013**: Contract let
  - Up to four awards
- **September 2013:** Project Kickoff Meeting
- **November 2013:** Technical Interchange Meeting
  - Contractor derived USAF requirements documents delivered
  - Finalized joint AFRL/NASA requirements document published
- **May 2014**: Benchmarks for NASA applications delivered to contractors
- **August 2014**: Innovation Phase concludes
  - Draft final reports delivered to AFRL/NASA
  - Software derived requirements available
  - Evaluation and selection of architecture(s) for implementation

Transition Plan for Mission Use

First-user Infusion Pathways



- **Mars Exploration** – Future Mars missions (2020 and beyond)
  - **Landing Vision System** – TRN and HDA algorithms for pinpoint landing, for site access and sample return
  - **Fast Traverse** – Remove computation as a limiting factor for surface mobility, drive safely 10X+ faster
  - **Rover Science** – Perform science operations continuously during traverse: "Walk and chew gum"
  - *Discussions underway with NASA STMD and the Mars Exploration Program towards a Mars 2020 technology payload concept to demonstrate the above capabilities, supported by HPSC*



- **Earth Science** – Future Earth-observing missions will carry high data rate instruments (hyper-spectral, radar …) ongoing HyspIRI study

- **Human Spaceflight** – MPCV/Orion: Time/space and memory partitioning will be an important human rating requirement – multi-core can provide natural fault containment structure

- **AFRL** – Sensor Payload Processing: Future systems will generate large amounts of data (hyper-spectral, hyper-temporal, radar …)

Summary

Flight Computing for the Future

- Future NASA mission scenarios call out for significantly ***improved flight computing*** capability
- Several NASA OCT Roadmaps and the NRC report identify ***improved flight computing*** as a foundational technology
- AFRL independently identifies the need for ***improved flight computing***
- ***Improved flight computing*** means enhanced computational performance, energy efficiency, and fault tolerance
- Like power and propulsion, flight computing is a ***core flight capability***; a technology advance here will be a capability ***multiplier*** and will impact the return from all future missions

It is time to move beyond the 1990's technology of the RAD750 and *Redefine the role of computing in space systems*

Backup

Why Now?

Multi-core computing should be viewed as a foundation and amplifier for several roadmapped technologies

- (TA04) Advances in high performance low power onboard computers are central to more capable space robotics.
- (TA05) Many of the complex [objectives of] future missions…can be mitigated by making decisions closer to the platform…Clearly this goal is coupled with the need for increased autonomy and flight computing.
- (TA09) Landing challenges include highly capable and low power on-board dedicated compute elements…
- (TA11) Pinpoint landing, hazard avoidance, rendezvous-and-capture, and surface mobility are directly tied to the availability of high-performance space-based computing.

Without investment in a next-generation flight computing solution, the robotics, G&C and EDL systems developed in 2020 will be forced to use processors and FPGAs that are a decade old, ill suited to the task, and unable to provide the needed capabilities. Advanced capabilities such as autonomous mission planning, onboard data reduction and knowledge extraction from high data rate instruments will not be practical.

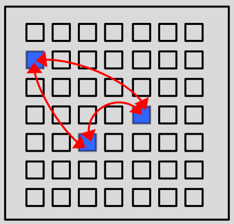
Fault Tolerance and Energy Management

- Beyond the performance advantages, multicore architectures support system-level scalability, flexibility and efficiency

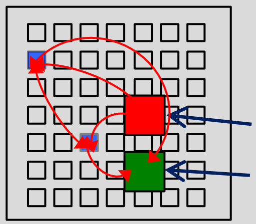
Note: View Animation

Software-based fault tolerance

Multiple cores allocated in a voting scheme



TMR (Detection)



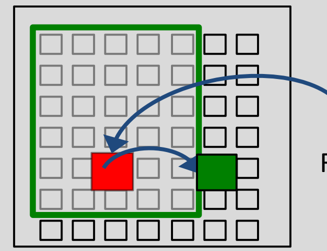
Failed core

Replacement core

TMR (Response)

Fail Operational

Many cores dedicated to parallel processing of image data



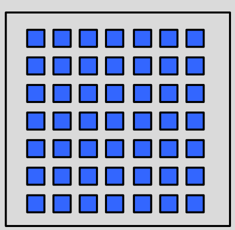
Failed core

Replacement core

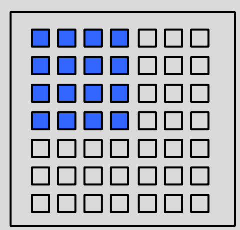
ABFT

Graceful Degradation

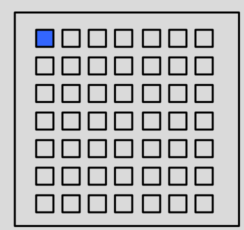
Energy management schemes



EDL



Surface Ops



Nighttime Ops

Redefining general-purpose computing for space systems

Gap Analysis

- ***There currently exists no spaceflight processor possessing:***
  - Processing performance and data rate consistent with needs of future HPSC applications (processing of at least 20 GOPS and 10Gbps I/O data rate)
  - Ability to accommodate a broad range of processing classes (DSP, matrix/vector math, general purpose control processing)
  - Low power dissipation (less than 7W for the processor)
  - Determinism suitable for use in real-time applications
  - Reliability and fault tolerance suitable for use in human life critical applications
  - Programmability with standard software languages and tools
- ***Some emerging computing architectures are very capable for specific applications, but:***
  - Non-rad-hardened architectures present a basic reliability concern
  - Low power budgets and power scaling ability are absent in most of the architectures

To obtain a flight computing solution with the above set of attributes for future NASA missions, an investment is needed

Scoring of the Architectures

vs. the KPPs

Key Performance Parameter (KPP)	Rad-hard General Purpose Multicore	Rad-hard DSP Multicore	Rad-hard Reconfigurable Computing	COTS-based Multicore	Rad-hard Graphics Processing Units
Cross-cutting Potential across NASA Missions	4.1	2.8	2.9	2.3	2.0
Computational Performance	5	2	4	5	5
Fault Tolerance	4	4	4	2	1
Power Dissipation	3	2	2	1	1
Power Scaling	5	3	5	1	2
Radiation Tolerance	4	4	4	2	3
Programmability and FSW Applicability	5	3	3	4	5
Flight Software V&V	4	3	3	4	5
Non-recurring cost	5	4	5	4	5
Recurring cost	4	3	2	5	2
Interoperability	4	3	2	5	4
Extensibility and Evolveability	5	4	4	4	3
Totals	**52.1**	**37.8**	**40.9**	**39.3**	**38.0**
# KPP scores above mean	**12/12**	**4/12**	**7/12**	**6/12**	**5/12**

Note: KPP scores above mean are shaded green

Ranking of the Architectures

The Runners-Up

Rad-hard DSP multicore

- Specialized processing provides insufficient support for **Cross-cutting Applicability**,
- Requires general-purpose co-processor or host processor

Rad-hard reconfigurable computing

- Lack of tools and poor testability present difficulties in FSW design (**Programmability**) and **V&V.**
- The **Non-Recurring Cost** to develop the underlying hardware is significant; without large investment presents large **Recurring Costs** for any new or mission-specific functionality.
- **Power Dissipation** is significant as the underlying hardware re-programmability fabric is power inefficient.

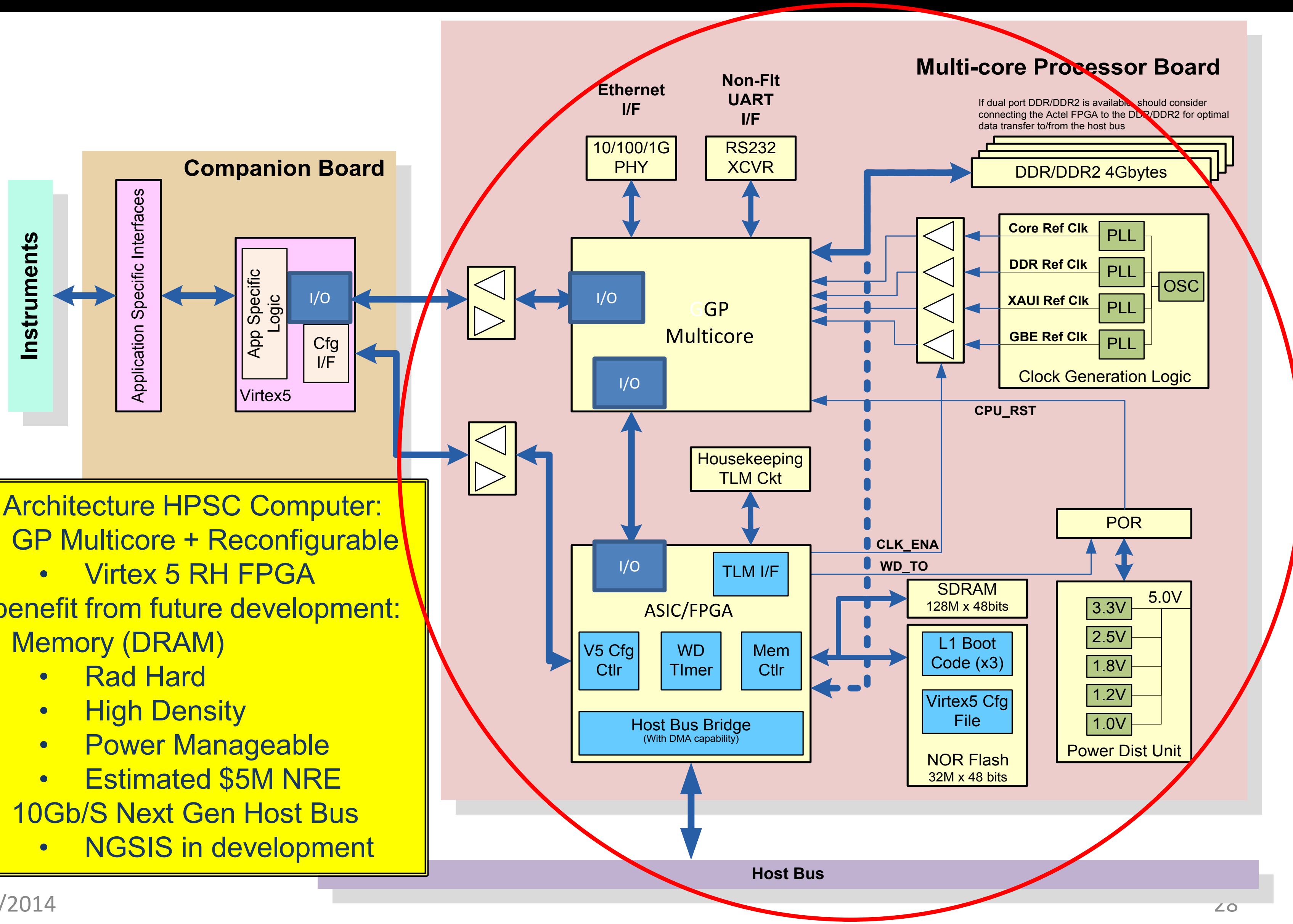
COTS-based multicore

- High **Power Dissipation** and poor **Power Scaling** capability in pursuit of high-performance is a persistent problem within the COTS class.
- A lack of **Radiation Tolerance** leads to complex and power hungry redundancy solutions for mission-critical applications.
- Because of the availability of **Non-Recurring Cost** leveraging, innovative solutions in this class bear watching.

Rad-hard graphics processing units

- Despite suitability for certain image processing applications, the challenge to bring **Power Dissipation, Power Scaling, Fault Tolerance, Non-Recurring Cost,** and **Recurring Cost** in-line make this solution inappropriate for a flight computer with **Cross-cutting Applicability**.

Flight Computer System Reference Design



- Dual Architecture HPSC Computer:
  - GP Multicore + Reconfigurable
    - Virtex 5 RH FPGA
- Will benefit from future development:
  - Memory (DRAM)
    - Rad Hard
    - High Density
    - Power Manageable
    - Estimated $5M NRE
  - 10Gb/S Next Gen Host Bus
    - NGSIS in development