# A Post-Processing Receiver for the Lunar Laser Communications Demonstration Project

Meera Srinivasan, Kevin Birnbaum, Michael Cheng, and Kevin Quirk

Jet Propulsion Laboratory, California Institute of Technology
4800 Oak Grove Dr., Pasadena, CA 91109, USA

## ABSTRACT

The Lunar Laser Communications Demonstration Project undertaken by MIT Lincoln Laboratory and NASA's Goddard Space Flight Center will demonstrate high-rate laser communications from lunar orbit to the Earth. NASA's Jet Propulsion Laboratory is developing a backup ground station supporting a data rate of 39 Mbps that is based on a non-real-time software post-processing receiver architecture. This approach entails processing sample-rate-limited data without feedback in the presence high uncertainty in downlink clock characteristics under low signal f ux conditions. In this paper we present a receiver concept that addresses these challenges with descriptions of the photodetector assembly, sample acquisition and recording platform, and signal processing approach. End-to-end coded simulation and laboratory data analysis results are presented that validate the receiver conceptual design.

**Keywords:** Optical communications, pulse position modulation, photon counting

## 1. INTRODUCTION

NASA's Lunar Laser Communications Demonstration Project (LLCD) will demonstrate high-rate laser communications from lunar orbit to a ground terminal on the Earth in order to prove the viability of optical communications concepts over a range ten times larger than those of near-Earth demonstrations to date, at data rates of up to 622 Mbps.[1,2] While the spacecraft terminal and ground receiver are being developed by MIT Lincoln Laboratory under the oversight of NASA's Goddard Space Flight Center, NASA's Jet Propulsion Laboratory is developing a backup ground station for LLCD supporting a data rate of 39 Mbps,[3] located at JPL's Optical Communications Telescope Laboratory (OCTL). The backup Lunar Laser OCTL Terminal (LLOT) receiver consists of a photon counting detector, data acquisition and storage hardware, and a suite of software for processing and returning LLCD data products.

The LLCD link requires a receiver capable of demodulating pulse-position modulation (PPM) signals under low photon f ux channel conditions. Depending upon the detector technology, the detection of individual photon arrivals is impaired to varying degrees by detector jitter and multiplicative pulse amplitude noise, as well as by thermal noise and detector output pulse distortion from detector output electronics. The detected photon arrivals must be converted into test statistics synchronized to specif c PPM time intervals, which are then used in the decoding process. In order to synchronize the PPM signal for proper demodulation and decoding, frame alignment sequences (FAS) that are periodically inserted into the LLCD signaling format must be acquired, and parameter estimates of the channel conditions must be made in the presence of background from scattered light and detector dark current, as well as a time varying frequency offset between the transmitter and receiver clocks.

In order to provide a cost effective backup receiver, LLOT employs a non-real-time software receiver architecture in which the downlink signal is sampled and stored using a commercial off-the-shelf (COTS) data acquisition system with a maximum sampling rate of approximately 1.25 Gsamples/sec, corresponding to four samples per slot at a data rate of 39 Mbps, or one sample per slot at 155 Mbps, which is the maximum data rate supportable by the current digitizer conf g-uration. Two separate software processing modes are provided: a concurrent channel estimator that periodically returns parameter estimates during the downlink pass, and a post-processing receiver/decoder that returns decoded telemetry data in addition to channel estimates after the pass is completed. In order to close the the LLOT link with this architecture, several signal processing algorithms were developed.[4] The architecture and algorithms were tested via Monte-Carlo simulation as well as through end-to-end detector hardware tests, demonstrating the viability of the system design.

In this paper we describe the LLOT receiver architecture, algorithms and performance results based upon simulations as well as limited laboratory testing. In Section 2 an overview of the receiver architecture is provided, including the signaling format, detector subassembly, and data capture and processing platform. A brief description of the signal processing

algorithms is given in Section 3, followed by results from Monte-Carlo simulations and laboratory end-to-end tests that illustrate the performance of the LLOT receiver in Sections 4.1 and 4.2, respectively.

## 2. ARCHITECTURE OVERVIEW

### 2.1 LLCD Downlink Signal Format

The LLCD data signaling format[5] is comprised of data from multiple sources that are transmitted on dedicated virtual channels multiplexed together to form a single subchannel. Each subchannel is independently encoded and interleaved prior to time-division multiplexing (TDM). This aggregate data signal is then pulse-position modulated to form the optical waveform for link transmission. While this general TDM framing is common to both the downlink and uplink, parameter values differ between the two links. We shall summarize the downlink specifications relevant to the LLOT receiver here.

LLCD data sources produce transfer frames consisting of header, information, and cyclic redundancy check (CRC) bits, which are multiplexed together to form a subchannel. Each downlink subchannel is protected by a rate $1/2$ serially-concatenated pulse-position modulation (SC-PPM) turbo code.[6] The subchannel bits are grouped into 4-bit symbols for periodic convolutional channel interleaving and an FAS is inserted prior to a specified number of interleaved coded symbols. This data processing is performed for each subchannel, after which the independently generated subchannels are multiplexed together to form TDM frames. The number of subchannels per TDM frame depends upon the downlink mode. The TDM frame bits are mapped to 16-ary PPM slots to modulate the downlink laser. The channel interleaver has a relative delay parameter that can be varied to accommodate channel conditions.

Given this signal format, the LLOT receiver must synchronize the received data to the LLCD TDM frame, pick out the desired subchannel, strip off its FAS, de-interleave the subchannel symbols, decode the data, and return the information bits.

### 2.2 Detector Subassembly

The detector subassembly must convert the downlink optical signal at 1550.12 nm into an electronic signal suitable for processing. Due to the low power incident upon the detector ($\sim$ 250pW), the detector should operate in the photon-counting regime with a detection efficiency of $\gtrsim$ 30% in order to support high data rates. In order to accommodate atmospheric blurring of the incident optical beam, the active area of the detector should be $\gtrsim 50\mu$m. Since the information is encoded in the timing of the optical pulses, the detector jitter should be a small fraction of the slot time. That is, the standard deviation in the time between when a photon strikes the detector and when the electrical signal is emitted should be $\lesssim$ 200ps. Furthermore, since a few photons will be detected in each signal slot, the detector should support instantaneous count rates $\gtrsim$ 500MHz. Several detector technologies were considered for LLOT including intensified photodiodes (IPDs), photomultiplier tubes (PMTs), avalanche photodiode (APD) arrays, and nanowire arrays.[7,8] Although the receiver algorithms discussed in this paper were initially designed with the IPD detector model in mind, they are flexible enough to accommodate other photon counting detectors provided that certain parameter modifications are made.

The arrival times of photoelectrons produced by the detector are characterized by a Poisson process governed by the PPM signal format and parameterized by the slot time, signal flux, and background flux (including scattered light, dark current flux, and signal laser modulation extinction ratio). Each photon arrival results in a detector output pulse with a Gaussian distributed timing jitter parameterized by its standard deviation, $\sigma_j$; this is an approximation, and a more accurate treatment of detector jitter may be found in Ref. 9. The current output of the the detector is proportional to charge carrier multiplication resulting from a detected photon or dark event; this is modeled as a Gamma distributed gain random variable whose variance is given by $F-1$, where $F$ is the detector excess noise factor. The post-detector amplifier and anti-aliasing filter will result in a lowpass filtered output pulse voltage that is modeled by a truncated sinc waveform whose main lobe width depends upon the output bandwidth of the post-detector electronics. Additive white Gaussian thermal noise with power spectral density $N_0$ is also contributed at this point. Depending upon the detector technology, multiple detector pixels may be combined in order to overcome blocking saturation effects. Rather than individually sample these multiple pixels (an option limited by digitizer capabilities), the detector pixel outputs are combined prior to sampling by the data capture and processing assembly. Figure 1 shows the detector assembly model used in algorithm development and for the numerical simulation results presented in this paper.

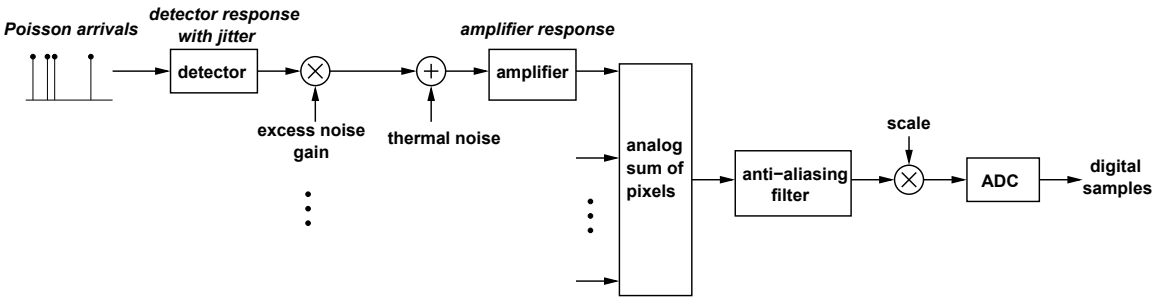


Figure 1. Detector Assembly Model

## 2.3 Data Capture and Processing Platform

The LLOT receiver assembly samples the PPM signal slots using a high-speed digitizer, stores the samples on a redundant array of independent disks (RAID), and post processes the sampled PPM signal in software. The downlink data volume for a 15 minute pass sampled at approximately 1.25 Gsamples/sec is 1.12 terabytes and the processed output per subchannel is 4.34 gigabytes.

### 2.3.1 Hardware Platform

High speed data capture and recording is performed by a Signatec signal acquisition system (Fig. 2), which is a COTS PC server running two Intel Xeon processors. The system hosts two PX1500 digitizer cards and each digitizer card can support a sampling rate of 1.5 Gsamples/sec using an 8-bit ADC. However, each card can only sustain a continuous transfer rate of 1.4 GB/sec to the PC via the PCI bus, and this effectively lowers the maximum sampling rate to 1.4 Gsamples/sec. This sampling rate is still suff cient to meet the sampling rate of approximately 1.25 Gsamples/sec, corresponding to one sample per slot at the 155 Mbps data rate. The PC server also hosts a RAID with forty-eight 500 GB drives totaling to a storage capacity of 24 terabytes and is equivalent to twenty 15 minute passes. The system is conf gured to RAID-0 to achieve the highest possible disk transfer rate. The Xeon processors are a perfect match for the computational demands of high volume data processing.

### 2.3.2 Data Processing

There are two data processing phases during operations. Concurrent processing (Fig. 3) takes place during recording; in this mode, statistics such as slot frequency estimate, frame detection f ag, mean photons per signal slot, and mean photons per background slot are generated by software processing of the samples as they are being recorded. Since the data acquisition rate is much higher than the software throughput, the statistics are generated in periodic intervals and the reporting rate is limited to 1 Hz. These statistics are forwarded to a Monitor and Control subassembly via ethernet where the information is stored in a database and relayed to the mission operations center. Post-processing (Fig. 4) begins after a signal pass completes and all of the signal samples in a pass are recorded onto the RAID. Demodulation, de-interleaving, and decoding are all performed in software on the recorded samples read back from the RAID. The post-processing throughput depends on the channel conditions but is on the order of few hundred kbps.

# 3. DATA PROCESSING ALGORITHMS

The LLOT receiver must form slot likelihood ratio statistics that can be used in the decoding algorithm[6] from the sampled detector output. Our approach to forming these statistics is to use a modif ed version of the sample-decision photon counting (SDPC) algorithm[4,10] to recover the number of photon arrivals from the sampled detector output, and then to form Poisson-channel log-likelihood ratios (LLR) from the estimated number of photons arrivals in each slot. Formation of the LLRs also requires slot synchronization as well as estimation of the mean number of signal and background counts. All of these functions must be performed in a low photon f ux regime with as little as one sample per slot, leading to large potential losses. An overview of the algorithms needed to accomplish these functions follows.

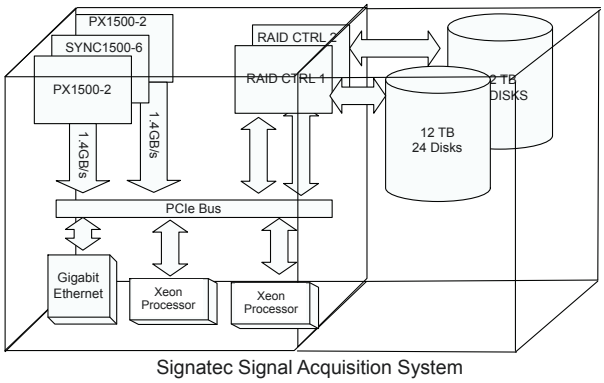


Figure 2. Data capture and processing platform (Signatec).

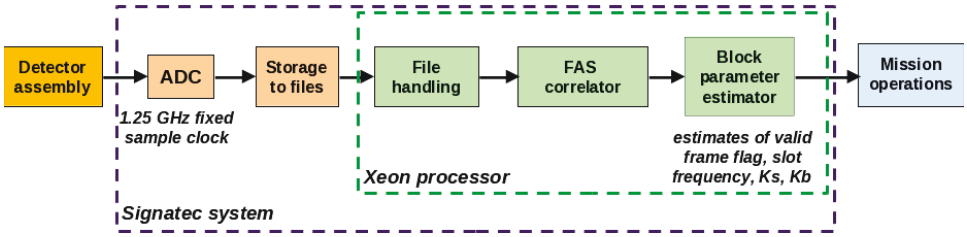


Figure 3. Concurrent channel estimation block diagram.

- Sample decisions photon counting: The detector output samples are converted into estimated photon counts by re-quantizing the ADC samples into a set of non-negative integers representing the number of detector output pulses superimposed in one sample interval. As the detector output pulse may extend over multiple samples, a decision feedback mechanism is used to prevent overcounting of pulses.[4] As the eff cacy of this algorithm depends upon the characteristics of the detector output, various sample decision parameters may be pre-selected and optimized for the various photon-counting detector technologies listed in Section 2.2.

- Slot synchronization: In order to accurately form the slot statistics, the sample decision counts must be allocated to the correct slots. This requires estimation of the slot times $\tau_n$, which are changing non-linearly due to the frequency offset and drift between the transmit and receive clocks. The presence of synchronization symbols, such as the FAS in the LLCD format, can be used to periodically estimate the slot phase. The synchronization task is complicated

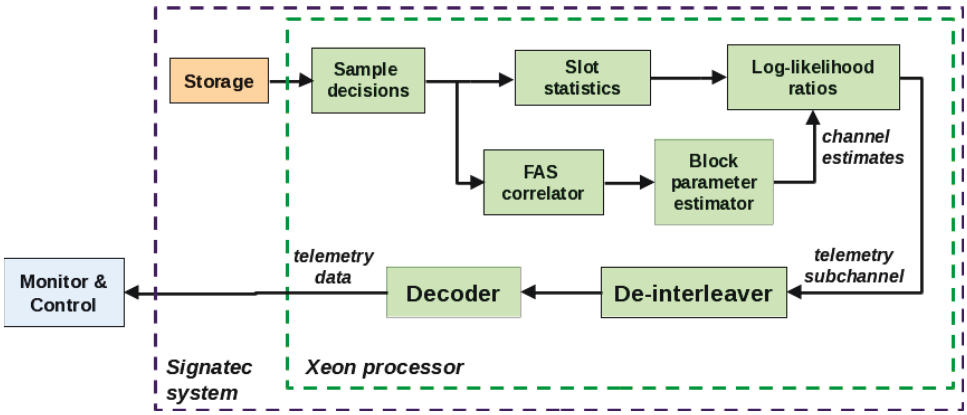


Figure 4. Post-processing receiver block diagram.

by high slot clock frequency offsets and drift rates originating from oscillator instability and motion between the transmitter and receiver. Due to the post-processing nature of the LLOT receiver with its fixed ADC clock, an open-loop block-based synchronization algorithm without feedback was developed.

In the LLOT synchronization algorithm, a block of $L$ slot phase estimates is obtained by correlating the sampled time series against $L$ consecutive periods of the FAS. The parameter $L$ is set to be within the coherence time of the channel where the relative clock drift between the transmitter and receiver is nearly constant, and the slot times are approximately linearly varying. Given the low signal photon flux conditions of the LLOT link, this block of $L$ slot phase estimates is not of sufficient quality to achieve reliable demodulation; hence, a novel linear least squares with outlier pruning (LLS-OP) algorithm has been developed to produce more refined estimates of the fractional frequency error and initial timing offset for each block.[4] These parameters are then used to properly align sample decisions with slots and form the LLRs.

- Signal and background estimation: The sample offset corresponding to the highest FAS correlation value identifies the locations of the signal slots in the FAS. As this correlation value is a function of the mean signal photons per symbol $K_s$ and the mean background photons per slot $K_b$, it may be used to form estimates of these quantities. These estimates are ad-hoc and depend upon the sample decision algorithm settings. Modifications to these estimators to more accurately account for channel impairments may result in improved performance.

- Interpolated log-likelihood ratios: The slot likelihood ratio is the ratio of the conditional probabilities that a given slot is or is not a signal slot, and is used in the SC-PPM decoding algorithm. For an ideal Poisson counting channel, the likelihood ratio is a function of the slot statistics (detected counts per slot), $K_s$, and $K_b$. In addition, although the slot synchronization algorithm described above assigns samples to slots, the low number of samples per slot results in significant signal pulse energy being split across adjacent slots due to the subsample timing offset. In order to compensate for this, the LLR for slot $k$ can be modified to interpolate across adjacent slot statistics with weights that incorporate the estimated $k$-th slot phase offset $\Delta_k$. In addition, knowledge of detector jitter parameters can also be incorporated into the probability model for the log-likelihood ratio in order to further mitigate losses.[4]

- De-interleaving and decoding: Once the LLRs have been formed, they are de-interleaved and decoded in software using an iterative decoding algorithm for SC-PPM.[6] The software decoding algorithm is implemented in parallel using multiple processor threads.

## 4. RESULTS

### 4.1 Monte-Carlo Simulation

In order to validate the receiver architecture and algorithms, extensive simulations were run over a variety of data rates and channel conditions. These simulations include the LLCD modulation and coding format, signal and background photon arrival process, photodetector modeling including detector jitter, excess noise, and output waveform bandlimiting, transmitter slot clock offset and linear drift, and all receiver estimation, synchronization, de-interleaving and decoding algorithms. Simulations were primarily run to ensure that the receiver meets the LLCD downlink requirement of $10^{-5}$ codeword error rate, but additional simulations were run to evaluate the performance of the estimation algorithms.

Although the LLOT implementation targets 39 Mbps, the receiver can process up to 155 Mbps with its existing digitizer configuration. In fact, greater performance gains are obtained from the interpolated log-likelihood ratio at higher data rates, as the slot width is shorter and more susceptible to the effect of detector jitter, and because fewer samples per slot leads to higher losses from slot misalignment. Figures 5 and 6 show codeword error rate as a function of the mean signal photons per symbol $K_s$ for the conditions listed in Table 1. These simulations were run for a detector model based upon data sheet parameters for an InGaAs IPD with an excess noise factor of 1.05, RMS jitter of 200 ps, dark rate of 4.5 Mphotons/sec, and detection efficiency of 30%. The results demonstrate link closure with more than 3 dB margin given the assumed detector model. Note that a larger $K_s$ is needed to close the link at 39 Mbps than at 155 Mbps; this is due to the much higher value of $K_b$ at 39 Mbps. However, note that the link margin at 39 Mbps is also higher than at 155 Mbps.

While the codeword error rate metric validates the performance of the post-processing receiver mode, the concurrent processing estimation mode performance may be judged based upon its ability to detect the presence of the LLCD signal structure as well as by the accuracy of its estimates of the slot frequency, and mean signal and background levels. In Figs. 7 through 11, the simulated performance of these estimators is shown at both 39 Mbps and 155 Mbps.

| Data Rate | $K_b$ | RMS Detector Jitter | Slot Frequency Offset | Slot Frequency Drift | Integration Time |
|---|---|---|---|---|---|
| 155 Mbps | 0.04632 | 200 ps | 350 kHz | 250 Hz/s | 3.2 ms |
| 39 Mbps | 0.3072 | 200 ps | 87.5 kHz | 62.5 Hz/s | 12.8 ms |

Table 1. LLOT simulation parameters

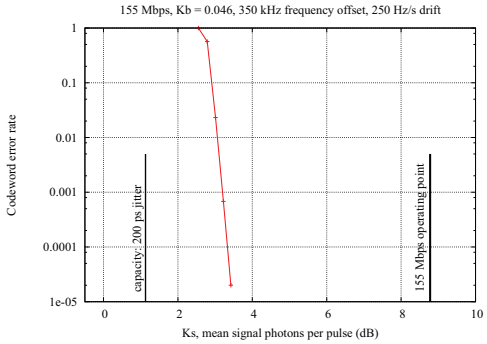


Figure 5. Simulated LLOT codeword error rates at 155 Mbps, with maximum frequency offset and drift.

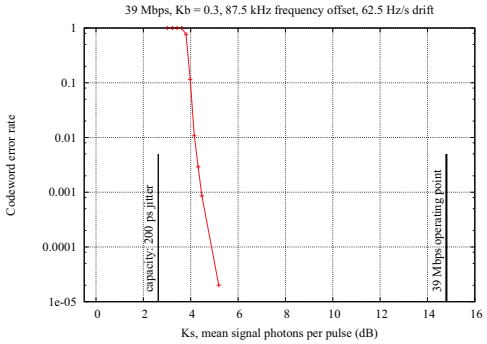


Figure 6. Simulated LLOT codeword error rates at 39 Mbps, with maximum frequency offset and drift.

In Fig. 7 we plot the simulated LLCD frame detection probability as a function of $K_s$. A frame here consists of the $L$ FAS periods that are used in making parameter estimates, and a frame is declared to be detected if more than a specif ed percentage of the $L$ timing offset estimates are determined to be valid. For the simulations shown here, $L$ was set to 64, and the minimum number of valid estimates was set to 10, leading to a threshold percentage of approximately 16%. We observe that at the $K_s$ values for which the link is closed, the frame detection probability is one.

In Figs. 8 and 9, the mean estimate of the slot frequency offset is plotted along with its $\pm 2\sigma$ errorbars as a function of $K_s$. The true slot frequency offset is set to a value of 280 ppm, i.e., 350 kHz at 155 Mbps, and 87.5 kHz at 39 Mbps. We observed that the residual slot frequency error diminishes to less than a quarter of a slot over the estimation interval in our expected region of operation ($K_s > 5$ dB).

Finally, in Figs. 10 and 11, the mean estimates of $K_s$ and $K_b$ are shown as a function of $K_s$. These f gures show a trend of underestimating the true values of $K_s$, and mixed results for estimating $K_b$. Of relevance here is the fact that the sample decision algorithm parameters were chosen to optimize codeword error rate rather than estimator performance. In practice, biases in the estimation algorithms may be corrected during testing of the f nalized detector subassembly through optimization of the sample decision parameters for the concurrent processing mode.

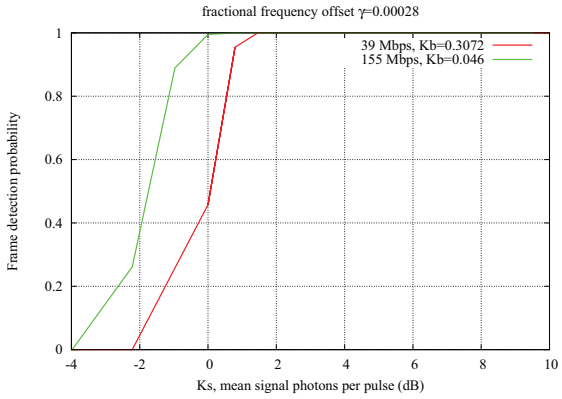


Figure 7. Simulated LLOT frame detection probability as a function of $K_s$ for 39 and 155 Mbps, $L = 64$.

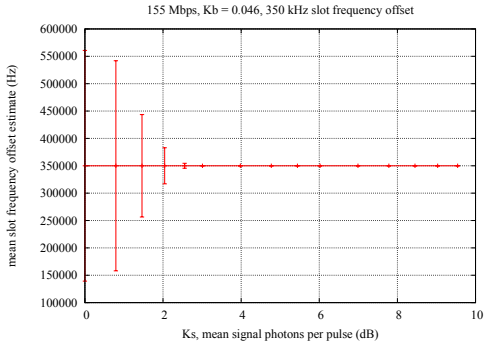


Figure 8. Simulated LLOT frequency estimator performance at 155 Mbps, 350 kHz slot frequency offset.

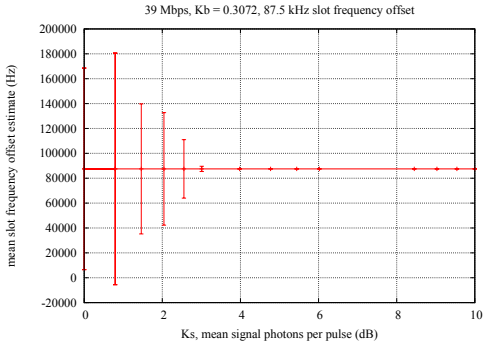


Figure 9. Simulated LLOT frequency estimator performance at 39 Mbps, 87.5 kHz slot frequency offset.

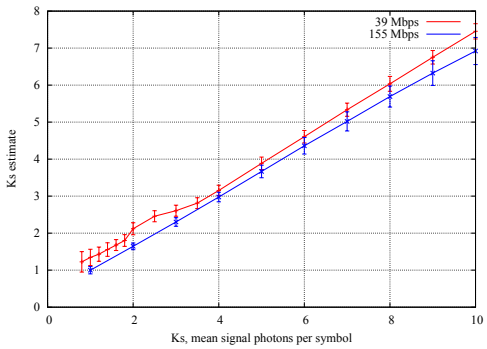


Figure 10. Simulated mean signal photon count estimator performance as a function of $K_s$ at 39 Mbps and 155 Mbps.

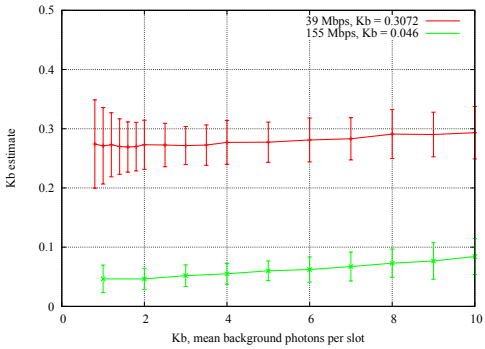


Figure 11. Simulated mean background photon count estimator performance at 39 Mbps (true $K_b = 0.3072$) and 155 Mbps (true $K_b = 0.046$) as a function of $K_s$.

### 4.2 End-to-end Laboratory Testing

A block diagram of the generic end-to-end laboratory test setup is shown in Fig. 12. The transmit emulator shown in this f gure consists of a waveform playback system that can generate LLCD signals at the data rates supported by the data acquisition system (39, 78, and 155 Mbps), including the periodic convolutional interleaving and SC-PPM encoding. It can also emulate transmit clock frequency offset and drift via a frequency synthesizer input. The output of the transmit emulator is used to modulate a laser with the 16-PPM signal. The output of the photodetector in response to this incident signal, as well as light from separately injected background laser, is amplif ed, f ltered, and sent to the Signatec system for sampling, storage, and processing.

Initial testing was performed with the InGaAs IPD at 1550 nm that was baselined for LLOT. However, these detectors were found to fail prematurely and to suffer from afterpulsing, rendering them incapable of meeting link requirements. Other detector options were then pursued; however, in order to progress with validation of the software receiver algorithms

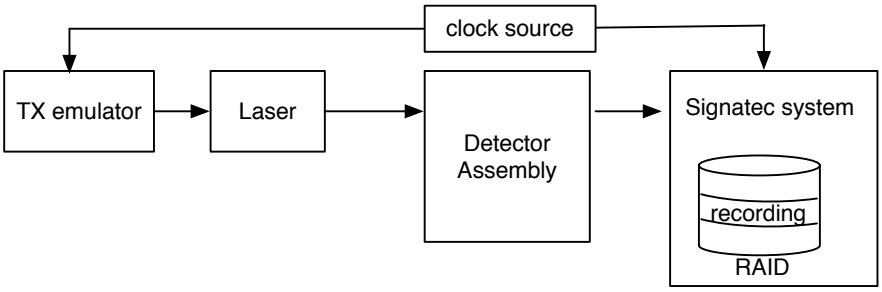


Figure 12. End-to-end laboratory test setup.

in a photon counting channel, an InGaAsP IPD operating at 1064 nm was tested at 39 Mbps. For these tests, the expected value of $K_s$ was 2.08. Incident background was not injected, but the maximum slot clock frequency offset and drift values were applied. Table 2 shows the results of these tests, demonstrating that the recorded data could be synchronized and processed, resulting in no codeword errors, even in the presence of signif cant clock offset and drift.

| Data Rate | Frequency Offset | Frequency Drift | Frequency Offset Estimation Error | $K_s$ Estimated | $K_b$ Estimated | Codeword Error Rate | Mean Decoder Iterations |
|---|---|---|---|---|---|---|---|
| 39 Mbps | 0 | 0 | -0.225 Hz | 1.973 | 0.018 | 0 | 3.002 |
| 39 Mbps | -87.5 kHz | 0 | -0.335 Hz | 1.952 | 0.019 | 0 | 3.041 |
| 39 Mbps | -87.5 kHz | 62.5 Hz/s | 0.252 Hz | 1.951 | 0.019 | 0 | 3.021 |
| 39 Mbps | 87.5 kHz | 0 | 0.143 Hz | 1.959 | 0.019 | 0 | 3.066 |
| 39 Mbps | 87.5 kHz | 62.5 Hz/s | -1.002 Hz | 1.95 | 0.019 | 0 | 3.027 |

Table 2. Estimator and decoder performance for 1064 nm IPD end-to-end tests.

Once it was determined that the IPD could not be used, other detector options were investigated.[3] In particular, tungsten-silicide (WSi) superconducting nanowire arrays[7,8] that are currently under development at JPL for free space optical communications appear to be very promising. A WSi device at 1550 nm with 7 pixels followed by discriminators and analog combining was tested at 39 Mbps with a target $K_s \sim 4$ and various background levels, but without slot clock frequency offset or drift. The results in Table 3 show that the link at 39 Mbps can be closed in nominal background cases, but not in the worst case with the 7-pixel device. Note that the estimates of $K_s$ and $K_b$ are signif cantly lower than the expected values. While part of this may be due to sample decision threshold selection, it is also likely due to the effect of blocking. More testing of WSi detectors is ongoing; with more pixels and additional optimization of detector electronics, blocking losses may be further overcome, potentially resulting in link closure in the worst case background conditions.

| Test Case | $K_s$ Expected | $K_b$ Expected | $K_s$ Estimated | $K_b$ Estimated | Codeword Error Rate | Mean Decoder Iterations |
|---|---|---|---|---|---|---|
| No background | 3.93 | 0 | 1.467 | 0.006 | 0 | 3.399 |
| Nominal signal-to-background ratio (SBR) | 3.97 | 0.0135 | 1.404 | 0.011 | 0 | 4.518 |
| 3 dB below nominal SBR | 3.94 | 0.0269 | 1.367 | 0.015 | 0 | 6.014 |
| Worst case SBR | 3.99 | 0.0385 | 1.35 | 0.018 | 0.019 | 9.307 |

Table 3. Estimator and decoder performance for 1550 nm WSi 7-pixel array end-to-end tests.

## 5. CONCLUSIONS

A post-processing software receiver concept for the LLCD backup ground station was presented. Descriptions of the detector and data acquisition assemblies were given, along with overviews of the signal processing algorithms needed to deliver channel estimates and decoded telemetry data. Monte-Carlo simulation results showing receiver performance were presented, and it was shown via simulation that the post-processing receiver concept is capable of closing the LLST-LLOT link with just one sample per slot in the presence of signif cant downlink slot clock dynamics. The minimum data rate requirement of 39 Mbps was shown to be achievable in the laboratory under nominal background conditions by using the tungsten-silicide superconducting nanowire detector array currently under development at JPL.

## 6. ACKNOWLEDGMENTS

The authors would like to acknowledge William Farr and Matt Shaw for assistance with the laboratory testing of the detector subassembly. The work described here was carried out at the Jet Propulsion Laboratory, California Institute of Technology, under contract with the National Aeronautics and Space Administration.

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