A Post-Processing Receiver for the Lunar Laser Communications Demonstration Project

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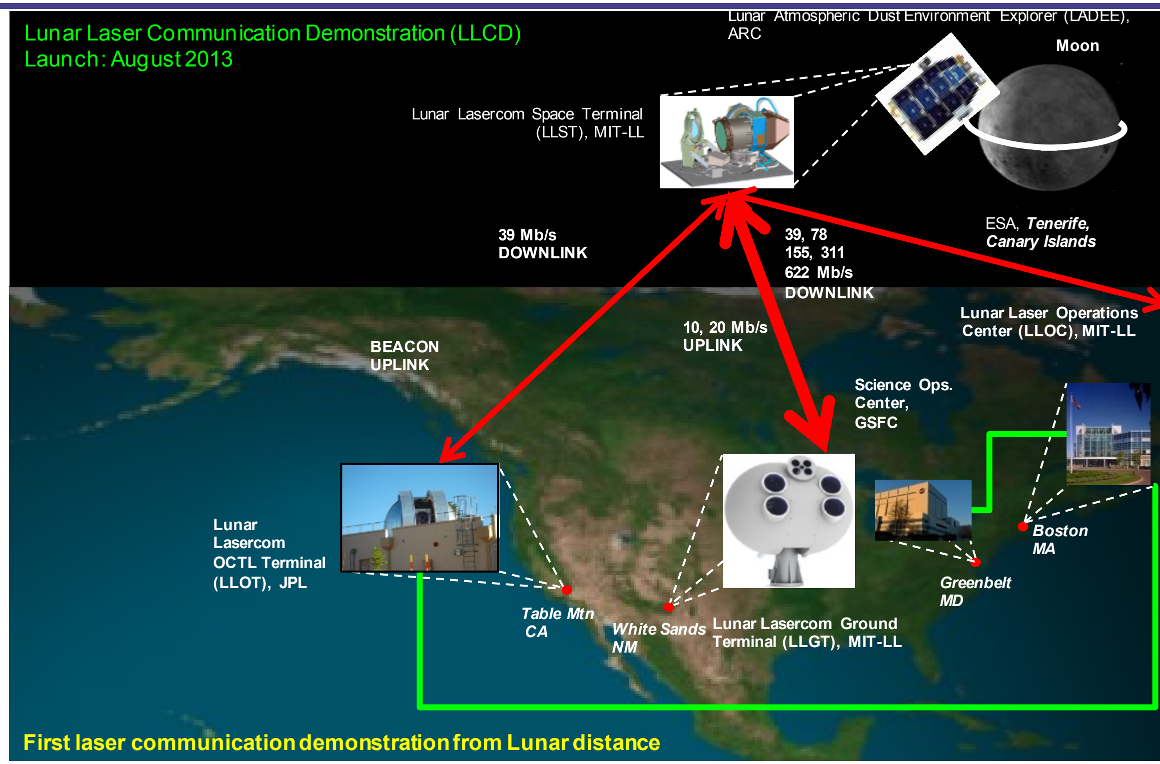
Outline

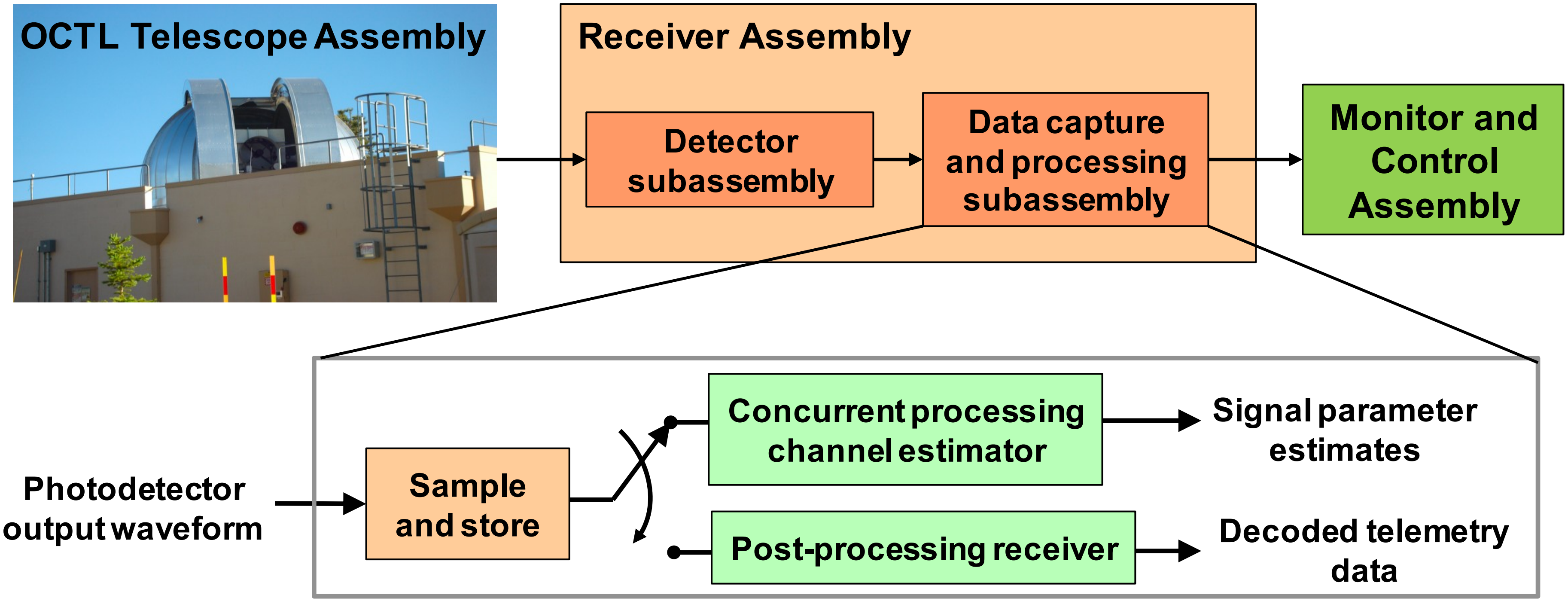
- Lunar laser OCTL terminal (LLOT)
- Architecture overview
    - Detector subassembly
    - Data capture and processing platform
    - Operation modes
- Data processing algorithms
- Test results
    - Monte-Carlo simulation
    - End-to-end laboratory testing

Lunar Laser OCTL Terminal



- **LLOT is a backup ground station for the Lunar Laser Communication Demonstration (LLCD).**
  - **16 day demonstration (August-October, 2013)**
  - **Link support at Sun-Earth-Probe (SEP) >10°**
  - **Transmit laser beacon to assist link acquisition**
  - **Receive downlink at 39 Mbps @ code-word error rate < 1E-5**
  - **Transmit limited real-time channel and link diagnostics to operations center**
  - **Process downlink in non-real time to extract information**

LLOT Receiver Overview



- **LLOT employs software receiver architecture**
  - Downlink signal is sampled and stored using COTS data acquisition system
  - Two software processing modes
    - Concurrent channel estimation: parameter estimates returned during pass
    - Post-processing receiver: after pass is completed, telemetry data is decoded
  - Architecture is transparent to detector options

LLOT Detector Subassembly

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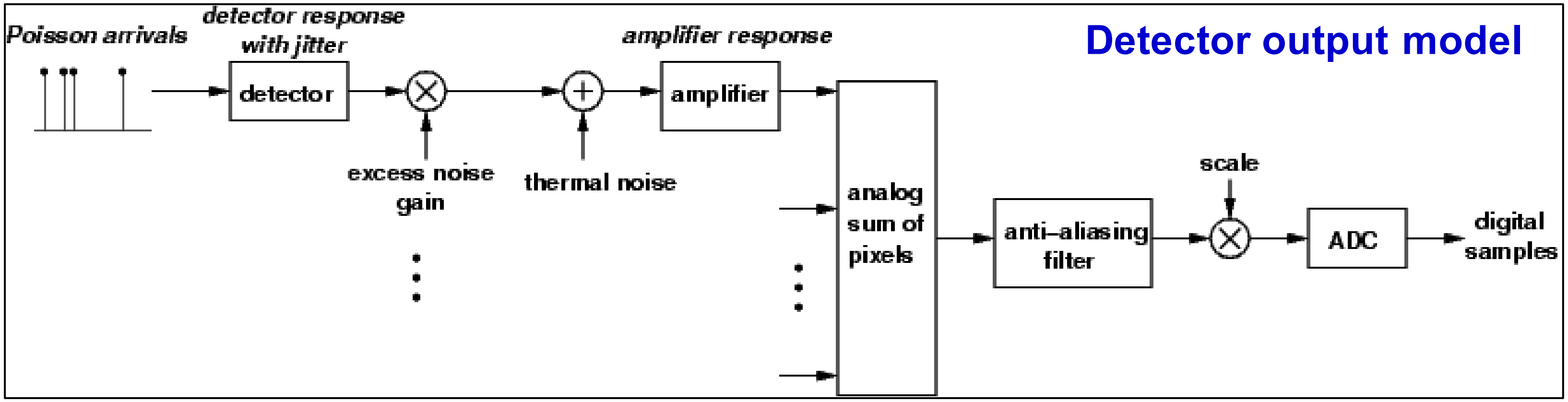
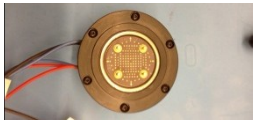


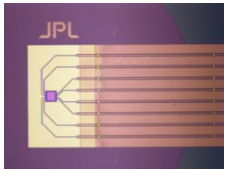
- Desired photodetector characteristics
  - Operates in photon counting regime (2 - 30 photons/bit).
  - Supports >500 MHz instantaneous photon count rates.
  - Detection efficiency >30% for data rates higher than 155 Mbps.
  - Active area > 50 µm.
  - Detector jitter < 200 ps.
  - Low excess and thermal noise.
- Several technologies considered
  - Intensified photodiodes (IPD)
  - Photomultiplier tubes (PMT)
  - Avalanche photodiodes (APD)
  - Nanowire arrays



Intevac IPD

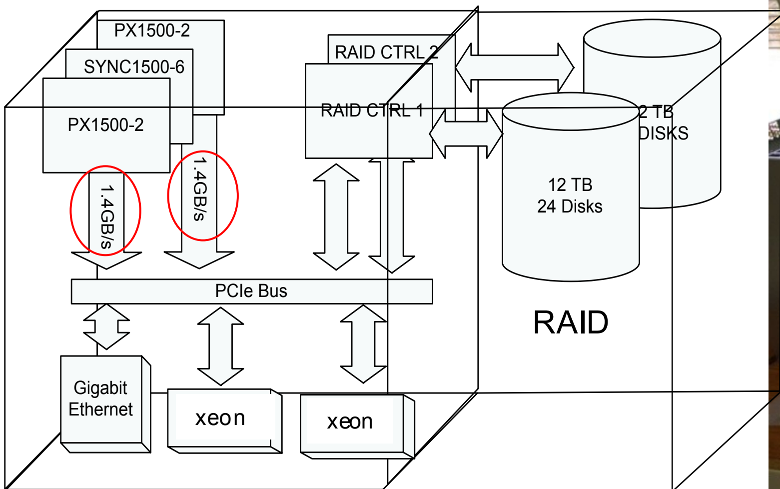
Hamamatsu PMT

Amplification Technologies DA-APD

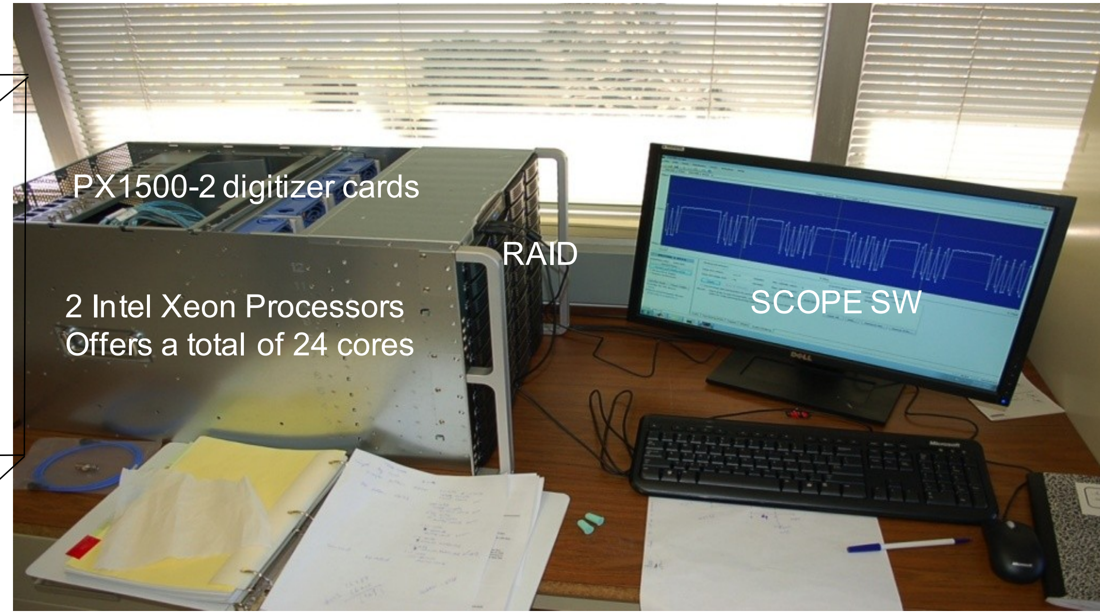


JPL WSi nanowire array

Data Capture and Processing Subassembly



Signatec Signal Acquisition System



- **Signatec signal acquisition system**
  - **COTS PC server running two Intel Xeon processors**
  - **Two PX1500 digitizer cards**
  - **24 TB RAID**
- **One digitizer card sampling at ~1.25 GHz can support**
  - **155 Mbps at 1 sample/slot**
  - **39 Mbps at 4 samples/slot**
- **RAID can store ~20 LLCD downlink passes (each pass ~15 minutes)**

Post-Processing Receiver Mode

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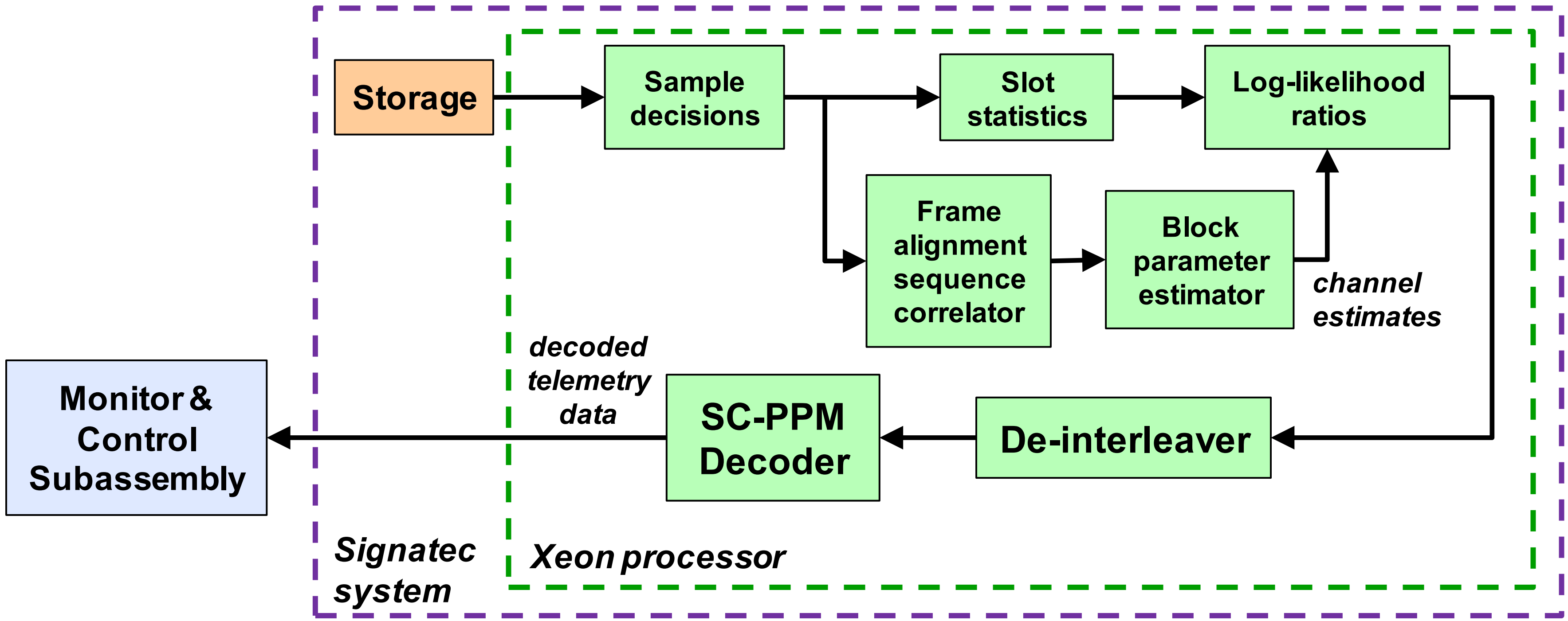
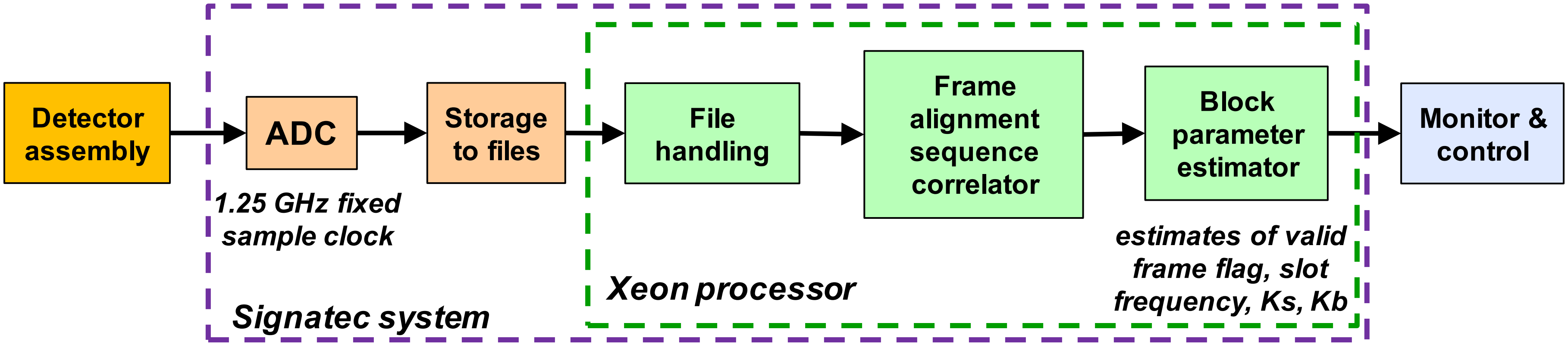


- **Full receiver processing starts after entire pass has been recorded**
- **Fixed sample clock - no frequency or phase adjustment**
- **Entire recording and software processing system implemented on single COTS platform.**

Concurrent Channel Estimation Mode



- Software operating on files during recording of downlink pass
- Signal parameters are estimated periodically during track (1 Hz rate)
  - Valid frame flag
  - Slot frequency
  - Ks (signal counts per symbol), Kb (background counts per slot)
- Indicates channel conditions and detection of LLCD signal format in recorded data
- Channel estimation algorithms are identical to post-processing algorithms.

Data Processing Algorithms

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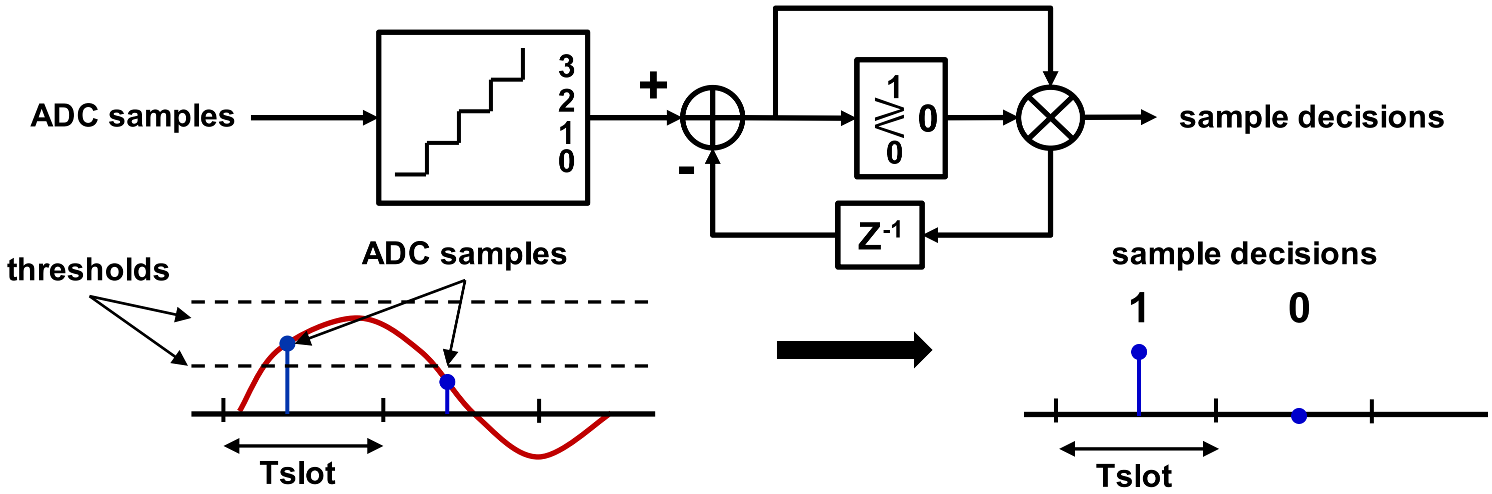
- **Demodulation and decoding must be performed in the presence of significant signal impairments.**

Issue	Algorithm Solution
Bandlimited detector pulse with thermal noise • Samples must be converted to photon counts.	***Sample decision photon counting***
Detector pulse arrival time jitter (100-200 ps) • Signal intensity spread over multiple slots at high data rates • Inter-slot and inter-symbol interference	***Modified log-likelihood ratio***
Fixed sampling clock with low samples/slot • Samples are not synchronized to slot timing, splitting signal intensity across slots	***FAS block parameter estimation + Modified log-likelihood ratio***
Free-running downlink slot clock • Significant dynamics between downlink slot clock and receiver sample clock • Misalignment of samples with slots causes decoding failure	***FAS block parameter estimation***

FAS = frame alignment sequence

Data Processing Algorithms: Sample Decision Photon Counting



- **Multi-level sample decision thresholding**
  - Converts ADC samples into estimates of photon counts.
  - Approximates Poisson sample statistics..
  - Memory parameter prevents overcounting of pulses.
  - Decision thresholds and memory adjusted for different detectors

Data Processing Algorithms: Open Loop Estimation and Slot Synchronization

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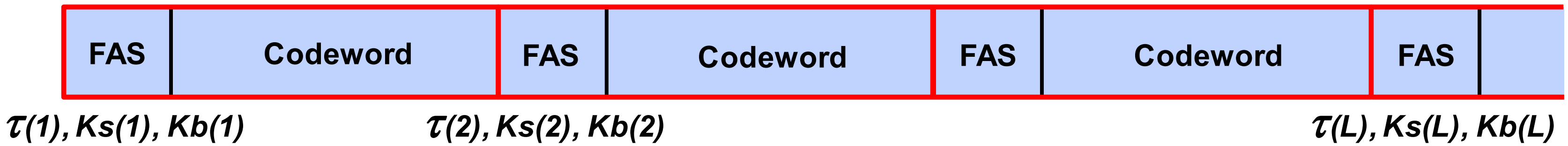
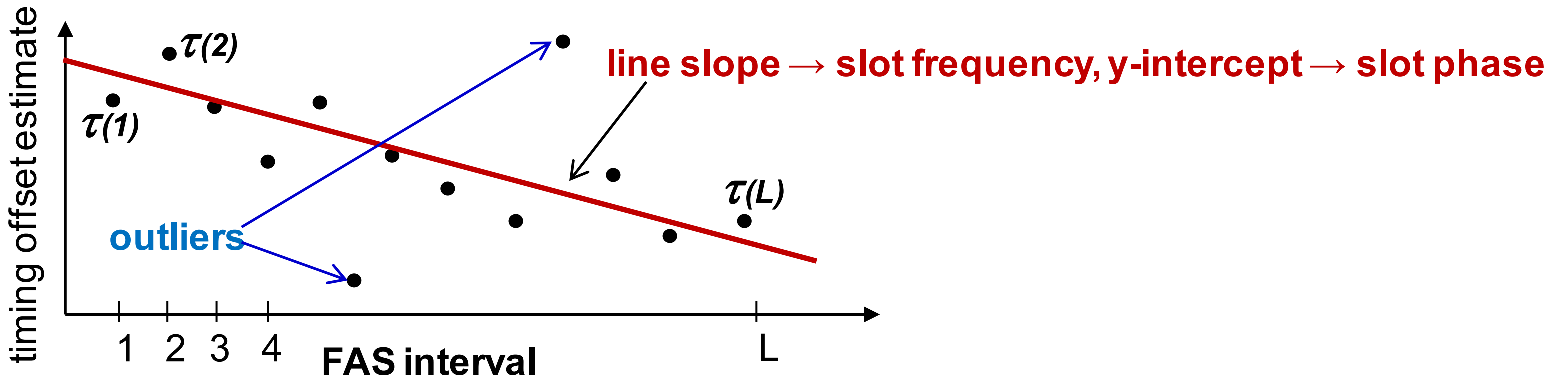
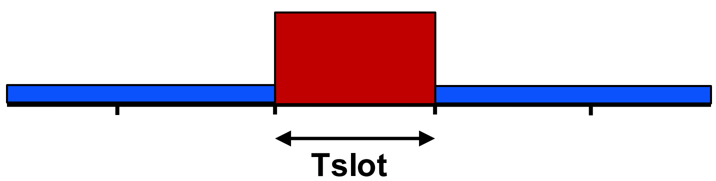


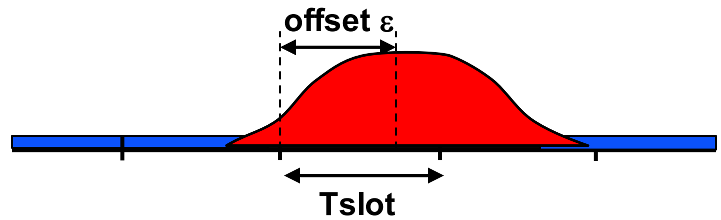
- **Sample decision counts must be correctly aligned with slots for demodulation.**
- **Downlink clock dynamics result in time-varying slot phase offsets.**
- **Frame alignment sequences allow periodic parameter estimation over linear phase intervals.**



- **Linear fit to block of *L* estimates → single slot frequency and phase estimate over block.**
- **Outlier pruning limits impact of spurious estimates.**
- **Signal (Ks) and background (Kb) estimates also made over block.**
- **Estimates are used in decoder log-likelihood ratio calculation.**
- **Frame declared valid if number of non-outliers exceeds specfied threshold.**

Data Processing Algorithms: Modified Log-likelihood Ratio





- **Interpolated log-likelihood ratio with detector jitter compensation**
  - Log-likelihood ratio (LLR) used in decoding algorithm.
  - Pulse jitter spreads average signal intensity over multiple slots at 155 Mbps.
  - LLR modified to recover signal energy in adjacent slots.
  - Parameter estimates needed for modified LLR.

$$LLR(i) = \sum_{j=i-2}^{i+2} \log\left(1 + f(i,j,\hat{\epsilon},\sigma_j)\frac{\hat{K}_s}{\hat{K}_b}\right)Y_j - \hat{K}_s$$

function of slot offset, rms detector jitter

estimates of mean signal and background photons per slot

  - Recovers ~2 dB of loss due to timing error and 200 ps pulse jitter at 155 Mbps

Simulated Decoding Performance

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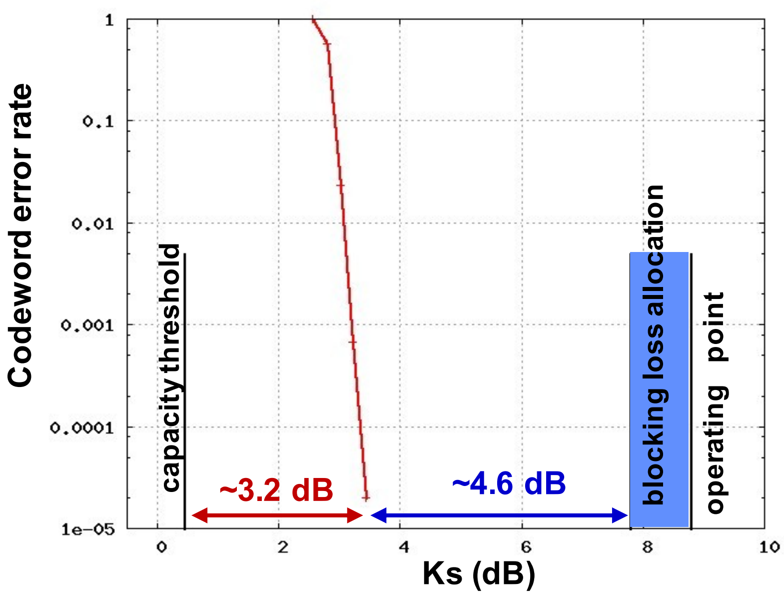
- Algorithms were validated via simulation under worst case conditions:

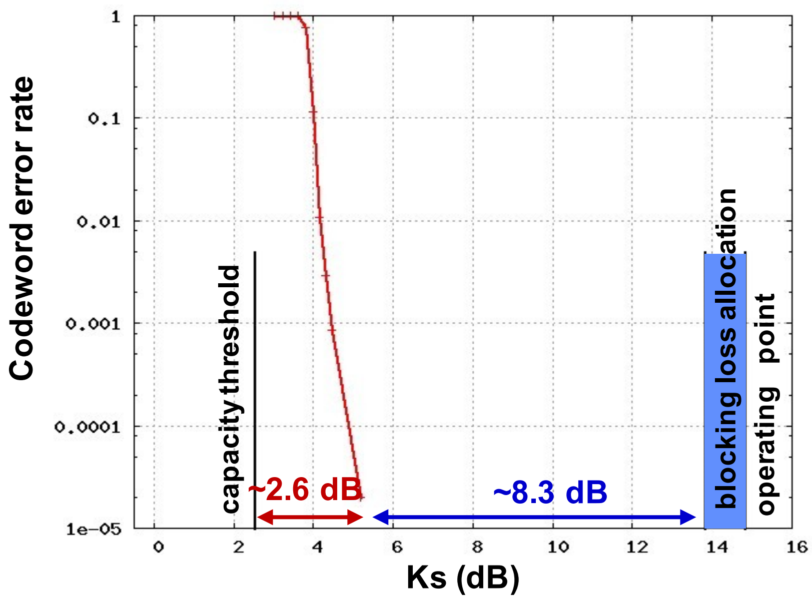
Data rate	Kb	detector jitter	frequency offset	frequency drift	integration time
155 Mbps	0.04632	200 ps	350 kHz	250 Hz/s	3.2 ms
39 Mbps	0.3072	200 ps	87.5 kHz	62.5 Hz/s	12.8 ms

- Simulation models coded signal, detector, clock dynamics, and data processing.
- Receiver software tracks maximum clock offset and decodes codewords.

Codeword Error Rate at 155 Mbps



Codeword Error Rate at 39 Mbps

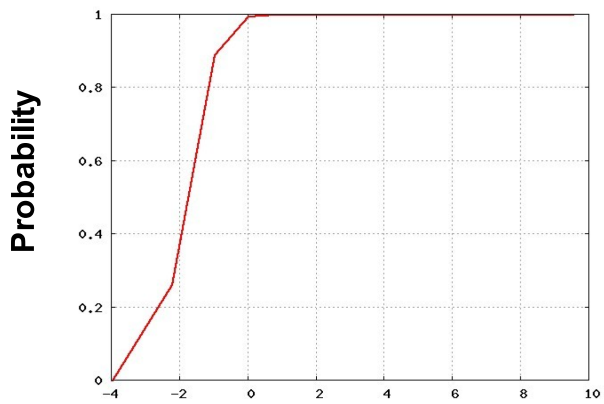


Simulated Channel Estimation: 155 Mbps

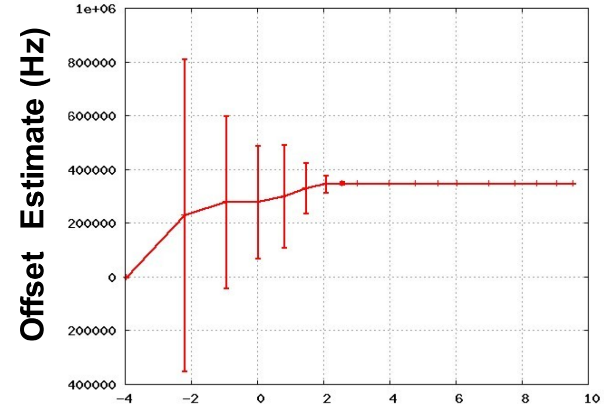
- Channel estimator tested on simulated bandlimited detector data at 155 Mbps with slot frequency offset of 350 kHz, Kb = 0.046 background photons/slot

- **Frame detection probability**
  - Empirical probability of high valid flag
  - Pd = 1 for CWE<1e-5
  - Pd → 0 as Ks → 0
- **Slot clock frequency estimate**
  - Residual error ±0.15 slots over estimation block in expected operating region
- **Ks, Kb estimates**
  - Dependent on sample decision parameters
  - Will be degraded by blocking

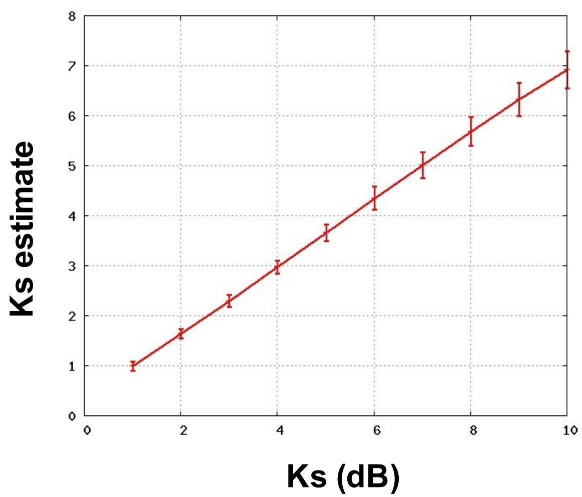
Frame detection probability



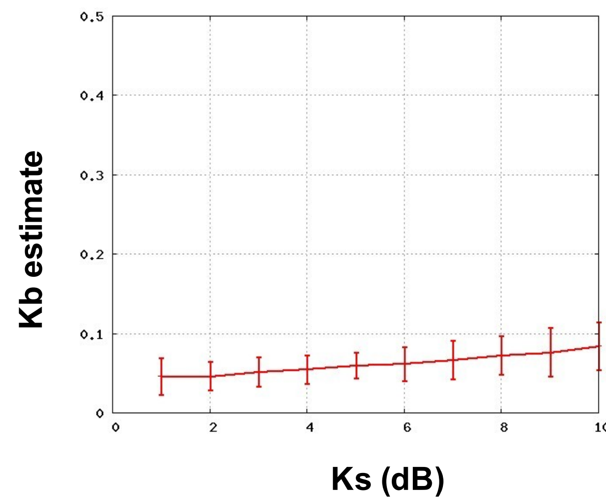
Frequency estimation



Ks estimate



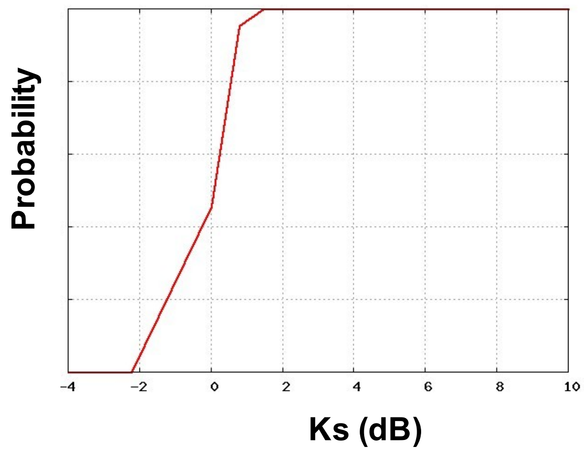
Kb estimate



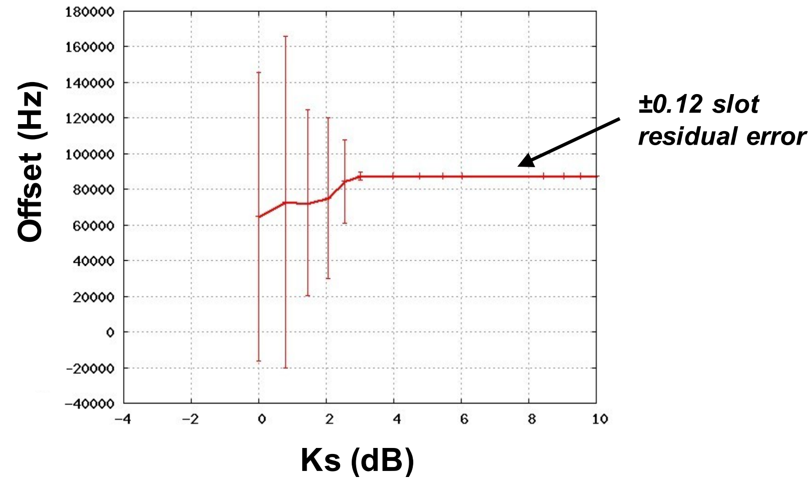
Simulated Channel Estimation: 39 Mbps

- 39 Mbps, with 87.5 kHz slot frequency offset, Kb = 0.3 background photons/slot

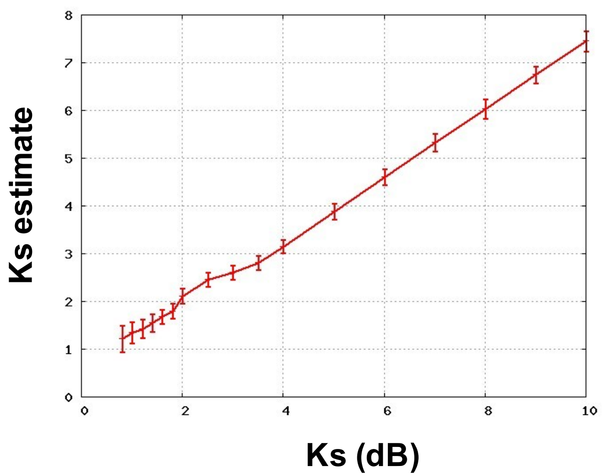
Frame detection probability



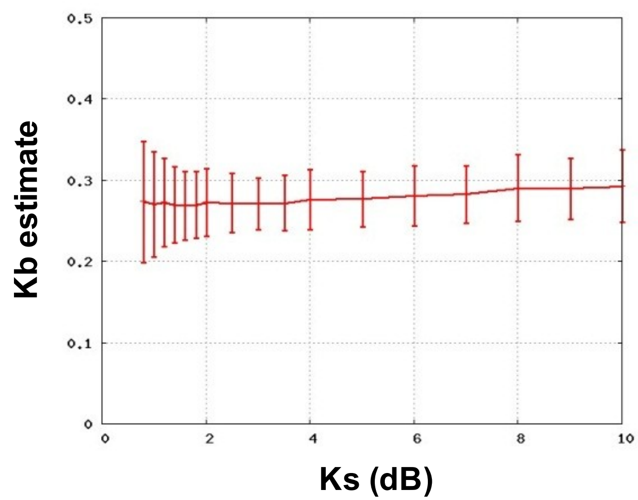
Frequency estimation



Ks estimate



Kb estimate



End-to-End Laboratory Testing

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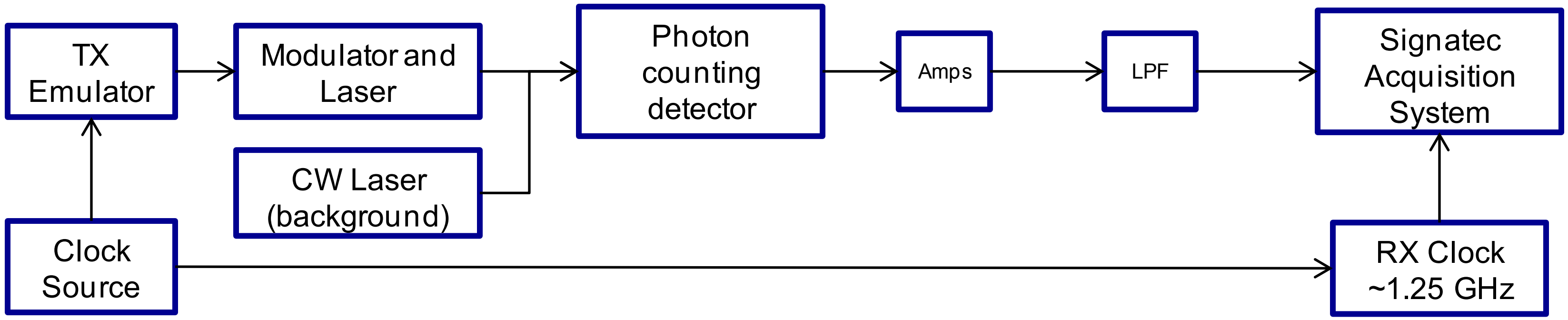

- **Conducted end-to-end optical testing with a 1550 nm detector**
  - **TX emulator plays encoded LLCD signals.**
  - **Detector output data recorded and processed with software receiver.**
  - **Background and slot clock frequency dynamics injected.**
- **IPD initially baselined for detector subassembly**
  - **Failed prematurely and suffered from afterpulsing**
- **PMT test device also unable to close link due to afterpulsing**
- **1064 nm IPD (no afterpulsing) tested to validate receiver software**
- **Tungsten silicide (WSi) superconducting nanowire array testing in progress**

1064 nm IPD Results

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Data Rate (Mbps)	Frequency (Hz)		Estimated Frequency Offset (Hz)	Estimated Ks	Estimated Kb	CWER	E[I]
	Offset	Drift					
39	0	0	0.188	1.973	0.018	0	3.002
	-87.5k	0	-87.526k	1.952	0.019	0	3.041
	-87.5k	62.5	-87.526k	1.951	0.019	0	3.021
	87.5k	0	87.464k	1.959	0.019	0	3.066
	87.5k	62.5	87.464k	1.95	0.019	0	3.027

- 1064 nm IPD tested to validate algorithms in optical channel
- 39 Mbps test data
  - No incident background
  - Maximum expected slot clock dynamics
- No codeword errors

1550 nm WSi Array Results

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39 Mbps Test Case	Expected Ks	Expected Kb	Estimated Ks	Estimated Kb	CWER	E[I]
No background	3.93	0	1.467	0.006	0	3.399
Nominal SBR	3.97	0.0135	1.404	0.011	0	4.518
3 dB below nominal SBR	3.94	0.0269	1.367	0.015	0	6.014
Worst case SBR	3.99	0.0385	1.35	0.018	0.019	9.307

- 1550 nm WSi 7-pixel array tested at 39 Mbps
  - 1 K operating temperature
  - Aggregate 29% detection efficiency
  - Discriminators after each pixel to reject thermal noise, followed by analog combining
  - Nominal to worst case signal-to-background ratio
  - No clock dynamics
- Low estimated photon counts due to blocking from detector reset time.
- No codeword errors at nominal SBR
- Additional testing in progress

Conclusions

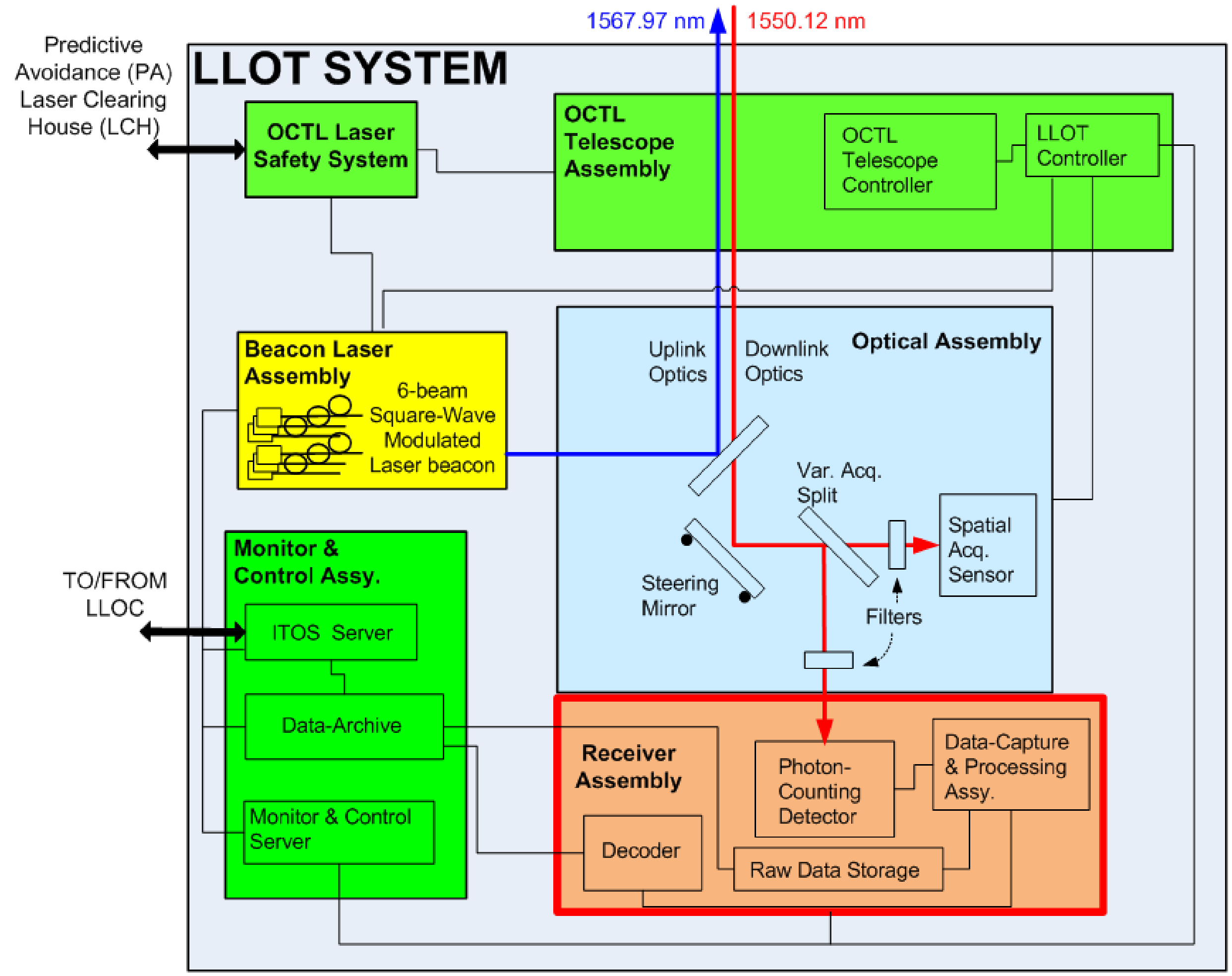
- Post-processing software receiver developed for Lunar Laser OCTL Terminal.
- Algorithms developed to perform channel estimation and telemetry decoding with few samples per slot, in low signal photon flux conditions, with significant downlink clock dynamics.
- Simulations and laboratory tests have validated algorithm performance.
- Tungsten-silicide nanowire detector array closes link at 39 Mbps in laboratory with nominal signal-to-background conditions.

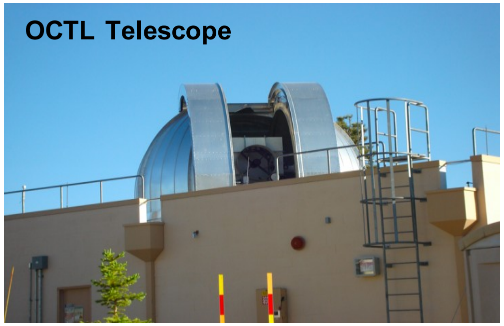
The work described here was performed at the Jet Propulstion Laboratory, California Institute of Technology ,under contract with the National Aeronautics and Space Administration (NASA).

Backup

Functional Block Diagram

- **LLOT System Block Diagram**





Data Processing Algorithms: Signal and Background Estimation

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- **Let the slot correlation statistic of the received slot counts $\{Y\}$ against the *j*th shift of the SFAS slot sequence $\{s\}$ accumulated over L SFAS periods be given by $\{C_L(j)\}$**
- **Let the shift corresponding to the maximum correlation statistic be $k^* = \arg\max_j \{C_L(j)\}$**
- **Estimates of the channel parameters and timing offset are given by**

mean background photons per slot
$$\hat{K}_b = \frac{1}{16L} C_L(k^* - (M-1))$$

mean signal photons per pulse
$$\hat{K}_s = \frac{C_L(k^*-1) + C_L(k^*) + C_L(k^*+1)}{16L(1-1/K)} - \hat{K}_b$$

time offset from start of subchannel i
$$\hat{\tau}_i = \left[k^* + \frac{C_L(k^*+1) - C_L(k^*-1)}{16L\hat{K}_s}\right] T_{slot}$$

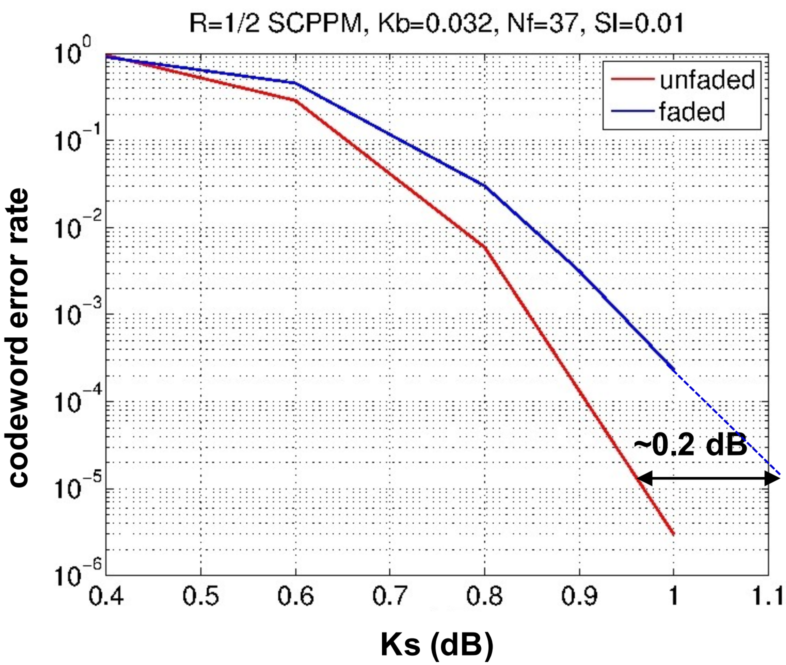
L-block slot offset (from slope of linear least-squares fit to $\{\hat{\tau}_i\}$)
$$\hat{\tau} = \frac{\sum_i \hat{\tau}_i - \sum_i i^2 - \sum_i i \sum_i \hat{\tau}_i^2}{L\sum_i i^2 - \left(\sum_i i\right)^2}$$

L-block normalized frequency offset (from slope of linear least-squares fit to $\{\hat{\tau}_i\}$)
$$\hat{\gamma} = \frac{L\sum_i i\hat{\tau}_i - \sum_i i \sum_i \hat{\tau}_i}{L\sum_i i^2 - \left(\sum_i i\right)^2}$$

FADING ANALYSIS

- **Fading caused by atmospheric scintillation was analyzed at 155 Mbps (Moision)**
- **Predicted performance losses due to scintillation and finite interleaver depth**

Scintillation index	Coherence time	Interleaver parameters	Interleaver depth	Fading loss	Finite interleaver loss	Total loss
0.01	10 ms	N=84, B=2070	0.74 s	0.02 dB	0.19 dB	0.21 dB



- **Stand-alone fading simulation shows ~0.2 dB loss relative to unfaded case**
- **Tests planned to verify additive fading loss**
  - **Simulation**
    - **Subchannel interleaver/de-interleaver and fading simulation code written**
    - **Run time limited by computing resources**
  - **End-to-end fading test**
  - **Pointing-induced fading process not analyzed**

PARAMETER ESTIMATION ALGORITHM FLOWCHART

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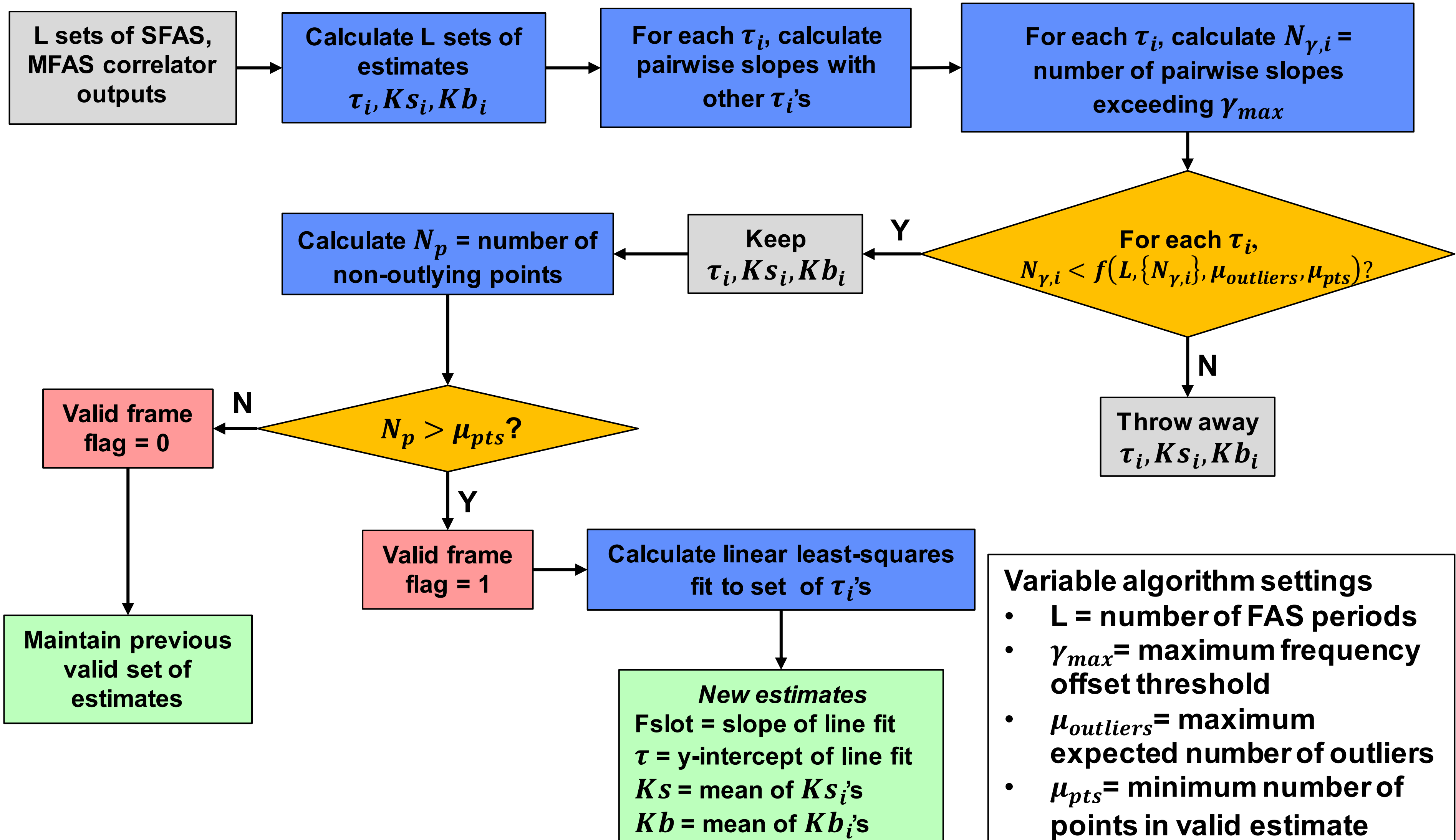

Variable algorithm settings

- L = number of FAS periods
- γ_{max}= maximum frequency offset threshold
- $\mu_{outliers}$= maximum expected number of outliers
- μ_{pts}= minimum number of points in valid estimate

EFFICACY OF OUTLIER PRUNING

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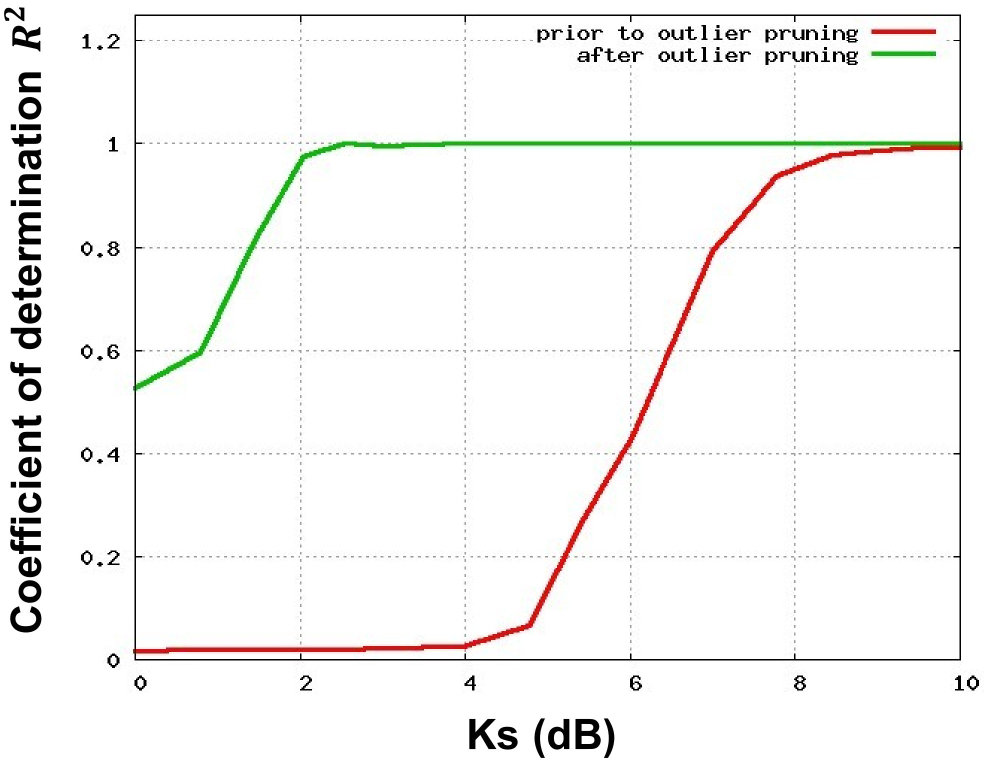
- Ultimate performance metric for slot frequency and phase estimation algorithm using linear least-squares fitting is frequency estimation error.
- Pruning algorithm eliminates outliers prior to linear fit, and is based on maximum expected frequency offset and expected number of outliers
- Coefficient of determination (R^2) metric can be used to evaluate linearity of data set prior to and after pruning



- 155 Mbps
- Kb = 0.04632 ph/slot
- Algorithm parameters
  - L = 64
  - γ_{max} = 0.001
  - $\mu_{outliers}$ = 28
  - μ_{pts} = 10