A Post-Processing Receiver for the Lunar Laser Communications Demonstration Project

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• Lunar laser OCTL terminal (LLOT)
• Architecture overview
  • Detector subassembly
  • Data capture and processing platform
  • Operation modes
• Data processing algorithms
• Test results
  • Monte-Carlo simulation
  • End-to-end laboratory testing
Lunar Laser OCTL Terminal

- LLOT is a backup ground station for the Lunar Laser Communication Demonstration (LLCD).
  - 16 day demonstration (August-October, 2013)
  - Link support at Sun-Earth-Probe (SEP) >10°
  - Transmit laser beacon to assist link acquisition
  - Receive downlink at 39 Mbps @ code-word error rate < 1E-5
  - Transmit limited real-time channel and link diagnostics to operations center
  - Process downlink in non-real time to extract information
• LLOT employs software receiver architecture
  – Downlink signal is sampled and stored using COTS data acquisition system
  – Two software processing modes
    • Concurrent channel estimation: parameter estimates returned during pass
    • Post-processing receiver: after pass is completed, telemetry data is decoded
  – Architecture is transparent to detector options
LLOT Detector Subassembly

- Desired photodetector characteristics
  - Operates in photon counting regime (2 - 30 photons/bit).
  - Supports >500 MHz instantaneous photon count rates.
  - Detection efficiency >30% for data rates higher than 155 Mbps.
  - Active area > 50 μm.
  - Detector jitter < 200 ps.
  - Low excess and thermal noise.

- Several technologies considered
  - Intensified photodiodes (IPD)
  - Photomultiplier tubes (PMT)
  - Avalanche photodiodes (APD)
  - Nanowire arrays

Detector output model

Intevac IPD
Hamamatsu PMT
Amplification Technologies DA-APD
JPL WSi nanowire array
**Data Capture and Processing Subassembly**

- **Signatec signal acquisition system**
  - COTS PC server running two Intel Xeon processors
  - Two PX1500 digitizer cards
  - 24 TB RAID

- **One digitizer card sampling at ~1.25 GHz can support**
  - 155 Mbps at 1 sample/slot
  - 39 Mbps at 4 samples/slot

- **RAID can store ~20 LLCD downlink passes (each pass ~15 minutes)**
Post-Processing Receiver Mode

- Full receiver processing starts after entire pass has been recorded
- Fixed sample clock - no frequency or phase adjustment
- Entire recording and software processing system implemented on single COTS platform.
Concurrent Channel Estimation Mode

- Software operating on files during recording of downlink pass
- Signal parameters are estimated periodically during track (1 Hz rate)
  - Valid frame flag
  - Slot frequency
  - Ks (signal counts per symbol), Kb (background counts per slot)
- Indicates channel conditions and detection of LLCD signal format in recorded data
- Channel estimation algorithms are identical to post-processing algorithms.
Data Processing Algorithms

- Demodulation and decoding must be performed in the presence of significant signal impairments.

<table>
<thead>
<tr>
<th>Issue</th>
<th>Algorithm Solution</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bandlimited detector pulse with thermal noise</td>
<td>Sample decision photon counting</td>
</tr>
<tr>
<td>• Samples must be converted to photon counts.</td>
<td></td>
</tr>
<tr>
<td>Detector pulse arrival time jitter (100-200 ps)</td>
<td>Modified log-likelihood ratio</td>
</tr>
<tr>
<td>• Signal intensity spread over multiple slots at high data rates</td>
<td></td>
</tr>
<tr>
<td>• Inter-slot and inter-symbol interference</td>
<td></td>
</tr>
<tr>
<td>Fixed sampling clock with low samples/slot</td>
<td>FAS block parameter estimation + Modified log-likelihood ratio</td>
</tr>
<tr>
<td>• Samples are not synchronized to slot timing, splitting signal intensity across slots</td>
<td></td>
</tr>
<tr>
<td>Free-running downlink slot clock</td>
<td>FAS block parameter estimation</td>
</tr>
<tr>
<td>• Significant dynamics between downlink slot clock and receiver sample clock</td>
<td></td>
</tr>
<tr>
<td>• Misalignment of samples with slots causes decoding failure</td>
<td></td>
</tr>
</tbody>
</table>

FAS = frame alignment sequence
Multi-level sample decision thresholding

- Converts ADC samples into estimates of photon counts.
- Approximates Poisson sample statistics.
- Memory parameter prevents overcounting of pulses.
- Decision thresholds and memory adjusted for different detectors
Data Processing Algorithms: 
Open Loop Estimation and Slot Synchronization

- Sample decision counts must be correctly aligned with slots for demodulation.
- Downlink clock dynamics result in time-varying slot phase offsets.
- Frame alignment sequences allow periodic parameter estimation over linear phase intervals.

- Linear fit to block of $L$ estimates → single slot frequency and phase estimate over block.
- Outlier pruning limits impact of spurious estimates.
- Signal ($K_s$) and background ($K_b$) estimates also made over block.
- Estimates are used in decoder log-likelihood ratio calculation.
- Frame declared valid if number of non-outliers exceeds specified threshold.
Interpolated log-likelihood ratio with detector jitter compensation

- Log-likelihood ratio (LLR) used in decoding algorithm.
- Pulse jitter spreads average signal intensity over multiple slots at 155 Mbps.
- LLR modified to recover signal energy in adjacent slots.
- Parameter estimates needed for modified LLR.

\[ LLR(i) = \sum_{j=i-2}^{i+2} \log \left( 1 + f(i, j, \hat{\epsilon}, \sigma_j) \frac{\hat{K}_s}{\hat{K}_b} \right) Y_j - \hat{K}_s \]

- Recovers ~2 dB of loss due to timing error and 200 ps pulse jitter at 155 Mbps
Simulated Decoding Performance

- Algorithms were validated via simulation under worst case conditions:

<table>
<thead>
<tr>
<th>Data rate</th>
<th>Kb</th>
<th>detector jitter</th>
<th>frequency offset</th>
<th>frequency drift</th>
<th>integration time</th>
</tr>
</thead>
<tbody>
<tr>
<td>155 Mbps</td>
<td>0.04632</td>
<td>200 ps</td>
<td>350 kHz</td>
<td>250 Hz/s</td>
<td>3.2 ms</td>
</tr>
<tr>
<td>39 Mbps</td>
<td>0.3072</td>
<td>200 ps</td>
<td>87.5 kHz</td>
<td>62.5 Hz/s</td>
<td>12.8 ms</td>
</tr>
</tbody>
</table>

- Simulation models coded signal, detector, clock dynamics, and data processing.
- Receiver software tracks maximum clock offset and decodes codewords.

Codeword Error Rate at 155 Mbps

Codeword Error Rate at 39 Mbps
Simulated Channel Estimation: 155 Mbps

- Channel estimator tested on simulated bandlimited detector data at 155 Mbps with slot frequency offset of 350 kHz, $K_b = 0.046$ background photons/slot

- Frame detection probability
  - Empirical probability of high valid flag
  - $P_d = 1$ for $CWE < 1e^{-5}$
  - $P_d \to 0$ as $K_s \to 0$

- Slot clock frequency estimate
  - Residual error $\pm 0.15$ slots over estimation block in expected operating region

- $K_s$, $K_b$ estimates
  - Dependent on sample decision parameters
  - Will be degraded by blocking

![Frame detection probability graph]

![Frequency estimation graph]

![Ks estimate graph]

![Kb estimate graph]
Simulated Channel Estimation: 39 Mbps

- 39 Mbps, with 87.5 kHz slot frequency offset, $K_b = 0.3$ background photons/slot
End-to-End Laboratory Testing

- Conducted end-to-end optical testing with a 1550 nm detector
  - TX emulator plays encoded LLCD signals.
  - Detector output data recorded and processed with software receiver.
  - Background and slot clock frequency dynamics injected.
- IPD initially baselined for detector subassembly
  - Failed prematurely and suffered from afterpulsing
- PMT test device also unable to close link due to afterpulsing
- 1064 nm IPD (no afterpulsing) tested to validate receiver software
- Tungsten silicide (WSi) superconducting nanowire array testing in progress
1064 nm IPD Results

<table>
<thead>
<tr>
<th>Data Rate (Mbps)</th>
<th>Frequency (Hz)</th>
<th>Estimated Frequency Offset (Hz)</th>
<th>Estimated Ks</th>
<th>Estimated Kb</th>
<th>CWER</th>
<th>E[I]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Offset Drift</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0.188</td>
<td>1.973</td>
<td>0.018</td>
<td>0</td>
<td>3.002</td>
</tr>
<tr>
<td>-87.5k</td>
<td>0</td>
<td>-87.526k</td>
<td>1.952</td>
<td>0.019</td>
<td>0</td>
<td>3.041</td>
</tr>
<tr>
<td>-87.5k</td>
<td>62.5</td>
<td>-87.526k</td>
<td>1.951</td>
<td>0.019</td>
<td>0</td>
<td>3.021</td>
</tr>
<tr>
<td>87.5k</td>
<td>0</td>
<td>87.464k</td>
<td>1.959</td>
<td>0.019</td>
<td>0</td>
<td>3.066</td>
</tr>
<tr>
<td>87.5k</td>
<td>62.5</td>
<td>87.464k</td>
<td>1.95</td>
<td>0.019</td>
<td>0</td>
<td>3.027</td>
</tr>
</tbody>
</table>

- 1064 nm IPD tested to validate algorithms in optical channel
- 39 Mbps test data
  - No incident background
  - Maximum expected slot clock dynamics
- No codeword errors
1550 nm WSi Array Results

<table>
<thead>
<tr>
<th>39 Mbps Test Case</th>
<th>Expected Ks</th>
<th>Expected Kb</th>
<th>Estimated Ks</th>
<th>Estimated Kb</th>
<th>CWER</th>
<th>E[I]</th>
</tr>
</thead>
<tbody>
<tr>
<td>No background</td>
<td>3.93</td>
<td>0</td>
<td>1.467</td>
<td>0.006</td>
<td>0</td>
<td>3.399</td>
</tr>
<tr>
<td>Nominal SBR</td>
<td>3.97</td>
<td>0.0135</td>
<td>1.404</td>
<td>0.011</td>
<td>0</td>
<td>4.518</td>
</tr>
<tr>
<td>3 dB below nominal SBR</td>
<td>3.94</td>
<td>0.0269</td>
<td>1.367</td>
<td>0.015</td>
<td>0</td>
<td>6.014</td>
</tr>
<tr>
<td>Worst case SBR</td>
<td>3.99</td>
<td>0.0385</td>
<td>1.35</td>
<td>0.018</td>
<td>0.019</td>
<td>9.307</td>
</tr>
</tbody>
</table>

- 1550 nm WSi 7-pixel array tested at 39 Mbps
  - 1 K operating temperature
  - Aggregate 29% detection efficiency
  - Discriminators after each pixel to reject thermal noise, followed by analog combining
  - Nominal to worst case signal-to-background ratio
  - No clock dynamics
- Low estimated photon counts due to blocking from detector reset time.
- No codeword errors at nominal SBR
- Additional testing in progress
Conclusions

• Post-processing software receiver developed for Lunar Laser OCTL Terminal.

• Algorithms developed to perform channel estimation and telemetry decoding with few samples per slot, in low signal photon flux conditions, with significant downlink clock dynamics.

• Simulations and laboratory tests have validated algorithm performance.

• Tungsten-silicide nanowire detector array closes link at 39 Mbps in laboratory with nominal signal-to-background conditions.

The work described here was performed at the Jet Propulsion Laboratory, California Institute of Technology, under contract with the National Aeronautics and Space Administration (NASA).
Backup
• LLOT System Block Diagram

LLOT SYSTEM

OCTL Laser Safety System

OCTL Telescope Assembly

OCTL Telescope Controller

LLOT Controller

Beacon Laser Assembly

6-beam Square-Wave Modulated Laser beacon

Optical Assembly

Uplink Optics

Downlink Optics

Var. Acq. Split

Steering Mirror

Filters

Spatial Acq. Sensor

Receiver Assembly

Photon-Counting Detector

Data-Capture & Processing Assy.

Decoder

Raw Data Storage

Monitor & Control Assy.

ITOS Server

Data-Archive

Monitor & Control Server

TO/FROM LLOC

Predictive Avoidance (PA) Laser Clearing House (LCH)
Data Processing Algorithms:
Signal and Background Estimation

- Let the slot correlation statistic of the received slot counts \( \{Y\} \) against the \( j \)th shift of the SFAS slot sequence \( \{s\} \) accumulated over \( L \) SFAS periods be given by \( \{C_L(j)\} \)

- Let the shift corresponding to the maximum correlation statistic be \( k^* = \arg \max_j \{C_L(j)\} \)

- Estimates of the channel parameters and timing offset are given by

  \[
  \hat{K}_b = \frac{1}{16L} C_L(k^* - (M - 1)) \\
  \hat{K}_s = \frac{C_L(k^* - 1) + C_L(k^*) + C_L(k^* + 1)}{16L(1 - 1/K)} - \hat{K}_b \\
  \hat{\tau}_i = \left[ k^* + \frac{C_L(k^* + 1) - C_L(k^* - 1)}{16L\hat{K}_s} \right] T_{\text{slot}} \\
  \hat{\tau} = \frac{\sum_i \hat{\tau}_i - \sum_i i^2 - \sum_i i \sum_i \hat{\tau}_i^2}{L \sum_i i^2 - (\sum_i i)^2} \\
  \hat{\gamma} = \frac{L \sum_i i \hat{\tau}_i - \sum_i i \sum_i \hat{\tau}_i}{L \sum_i i^2 - (\sum_i i)^2}
  \]
FADING ANALYSIS

- Fading caused by atmospheric scintillation was analyzed at 155 Mbps (Moision)
- Predicted performance losses due to scintillation and finite interleaver depth

<table>
<thead>
<tr>
<th>Scintillation index</th>
<th>Coherence time</th>
<th>Interleaver parameters</th>
<th>Interleaver depth</th>
<th>Fading loss</th>
<th>Finite interleaver loss</th>
<th>Total loss</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.01</td>
<td>10 ms</td>
<td>N=84, B=2070</td>
<td>0.74 s</td>
<td>0.02 dB</td>
<td>0.19 dB</td>
<td>0.21 dB</td>
</tr>
</tbody>
</table>

- Stand-alone fading simulation shows ~0.2 dB loss relative to unfaded case
- Tests planned to verify additive fading loss
  - Simulation
    - Subchannel interleaver/de-interleaver and fading simulation code written
    - Run time limited by computing resources
  - End-to-end fading test
  - Pointing-induced fading process not analyzed
PARAMETER ESTIMATION
ALGORITHM FLOWCHART

L sets of SFAS, MFAS correlator outputs
Calculate L sets of estimates $\tau_i, Ks_i, Kb_i$
For each $\tau_i$, calculate pairwise slopes with other $\tau_i$'s
For each $\tau_i$, calculate $N_{y,i} = \text{number of pairwise slopes exceeding } \gamma_{max}$

Calculate $N_p = \text{number of non-outlying points}$
Keep $\tau_i, Ks_i, Kb_i$
For each $\tau_i$, $N_{y,i} < f(L, \{N_{y,i}\}, \mu_{outliers}, \mu_{pts})$?
Y
N

Valid frame flag = 0
$N_p > \mu_{pts}$?
Y
N

Valid frame flag = 1
Calculate linear least-squares fit to set of $\tau_i$'s
New estimates
Fslot = slope of line fit
$\tau = y$-intercept of line fit
$Ks = \text{mean of } Ks_i$'s
$Kb = \text{mean of } Kb_i$'s

Maintain previous valid set of estimates
Throw away $\tau_i, Ks_i, Kb_i$

Variable algorithm settings
• $L = \text{number of FAS periods}$
• $\gamma_{max} = \text{maximum frequency offset threshold}$
• $\mu_{outliers} = \text{maximum expected number of outliers}$
• $\mu_{pts} = \text{minimum number of points in valid estimate}$

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EFFICACY OF OUTLIER PRUNING

- Ultimate performance metric for slot frequency and phase estimation algorithm using linear least-squares fitting is frequency estimation error.
- Pruning algorithm eliminates outliers prior to linear fit, and is based on maximum expected frequency offset and expected number of outliers.
- Coefficient of determination ($R^2$) metric can be used to evaluate linearity of data set prior to and after pruning.

155 Mbps
$K_b = 0.04632 \text{ ph/slot}$
Algorithm parameters
- $L = 64$
- $\gamma_{\text{max}} = 0.001$
- $\mu_{\text{outliers}} = 28$
- $\mu_{\text{pts}} = 10$