DESDynI* Quad First Stage Processor – A Four Channel Digitizer and Digital Beam Forming Processor

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*Proposed Mission – Pre-decisional – for Planning and Discussion Purposes Only

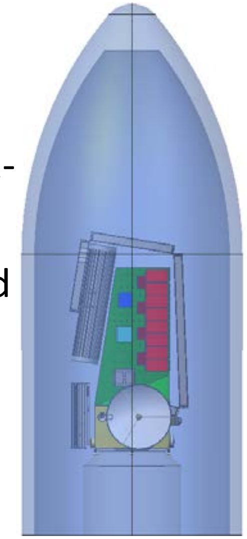
DESDynI-SAR Concept

Proposed Science Objectives

- Predict the response of ice masses to climate change and impact on sea level
- Characterize global distribution and changes of aboveground biomass and ecosystem structure related to the global carbon cycle, climate, and biodiversity
- Measure surface deformation to characterize geo-hazards (earthquakes, volcanic eruptions, and landslides)

Mission Concept

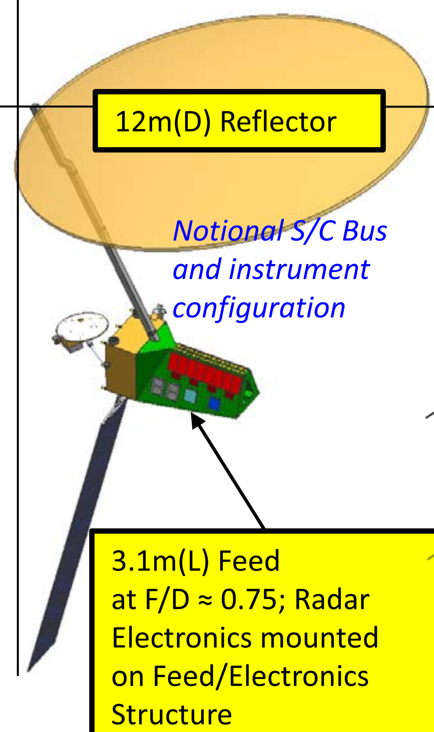
- Altitude: 747 km circular, 98º inclination, sun-synchronous, 12-day repeat
- Pointing control ±150 arcsec and stability 100 arcsec
- Repeat orbit within ±250m



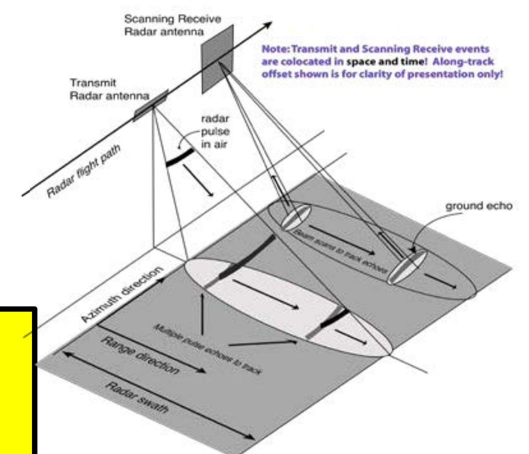
DESDynI-SAR in Launch Configuration*

Instrument Concept

- Repeat-pass interferometric SAR
- Fully polarimetric radar with SweepSAR technique for quad-pol full swath coverage
- Reflector with arrayed feed, boresighted at 35º from nadir, transmitting a fan beam and receiving with multiple pencil beams
- Active front-end electronics modules, with high-efficiency T/R and high-rate ADC



Sweep SAR Concept



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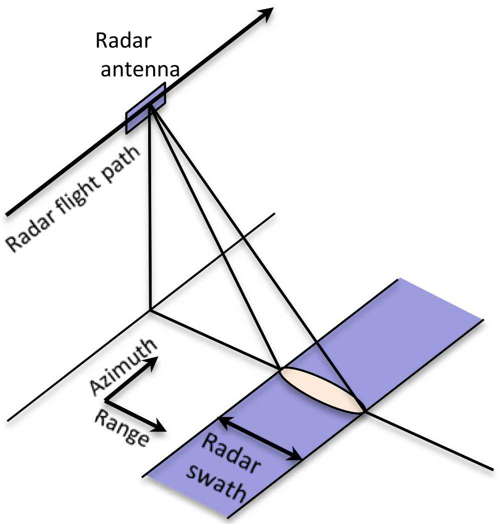
Proposed DESDynI SAR Instrument (DSI)

- DESDynI stands for Deformation, Ecosystems and Dynamics of Ice
- Repeat Period requirement for Deformation science would drive the Radar Swath
  - 12-day Repeat Period => 232km Swath Width
- Sensitivity requirement for Biomass measurement would drive Antenna Size and Radar Power
- Accuracy requirements for Deformation and Biomass would drive Electronics & Mechanical Stability and Calibration
- A new SweepSAR technique was adopted as a means to achieve much wider swath than conventional SAR strip-mapping, without the performance sacrifices associated with the older ScanSAR technique

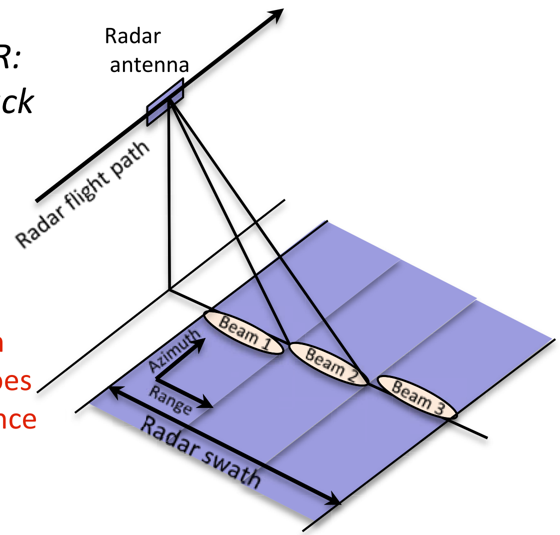
Conventional StripMap:
<~70km Swath

Resulting ~40 day repeat does *NOT* meet Deformation and Ice Science Requirements



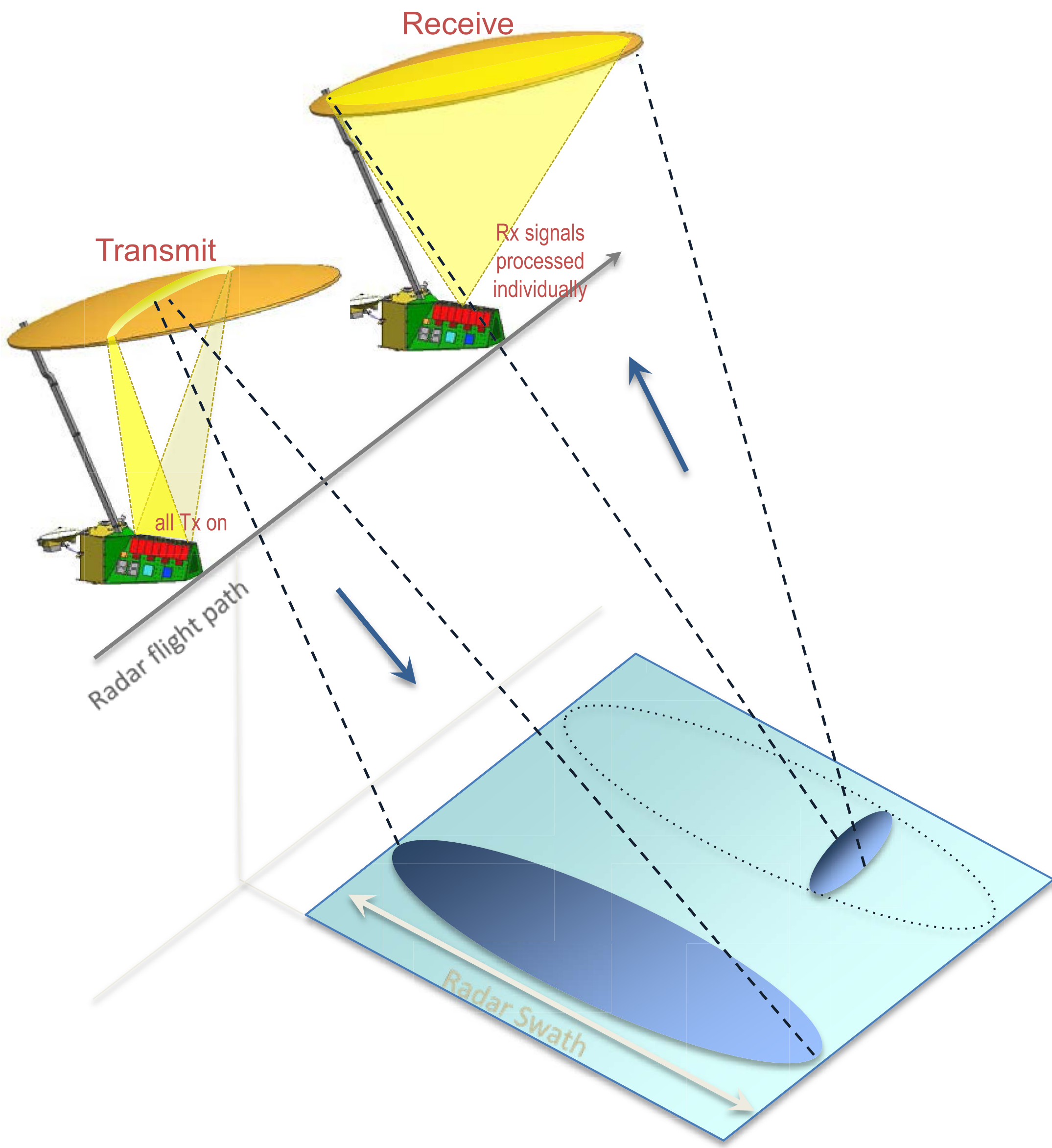
Conventional ScanSAR:
non-uniform along-track sampling

Resulting degradation in effective azimuth looks does *NOT* meet Ecosystem Science Requirements



SweepSAR Implemented with Array-Fed Reflector

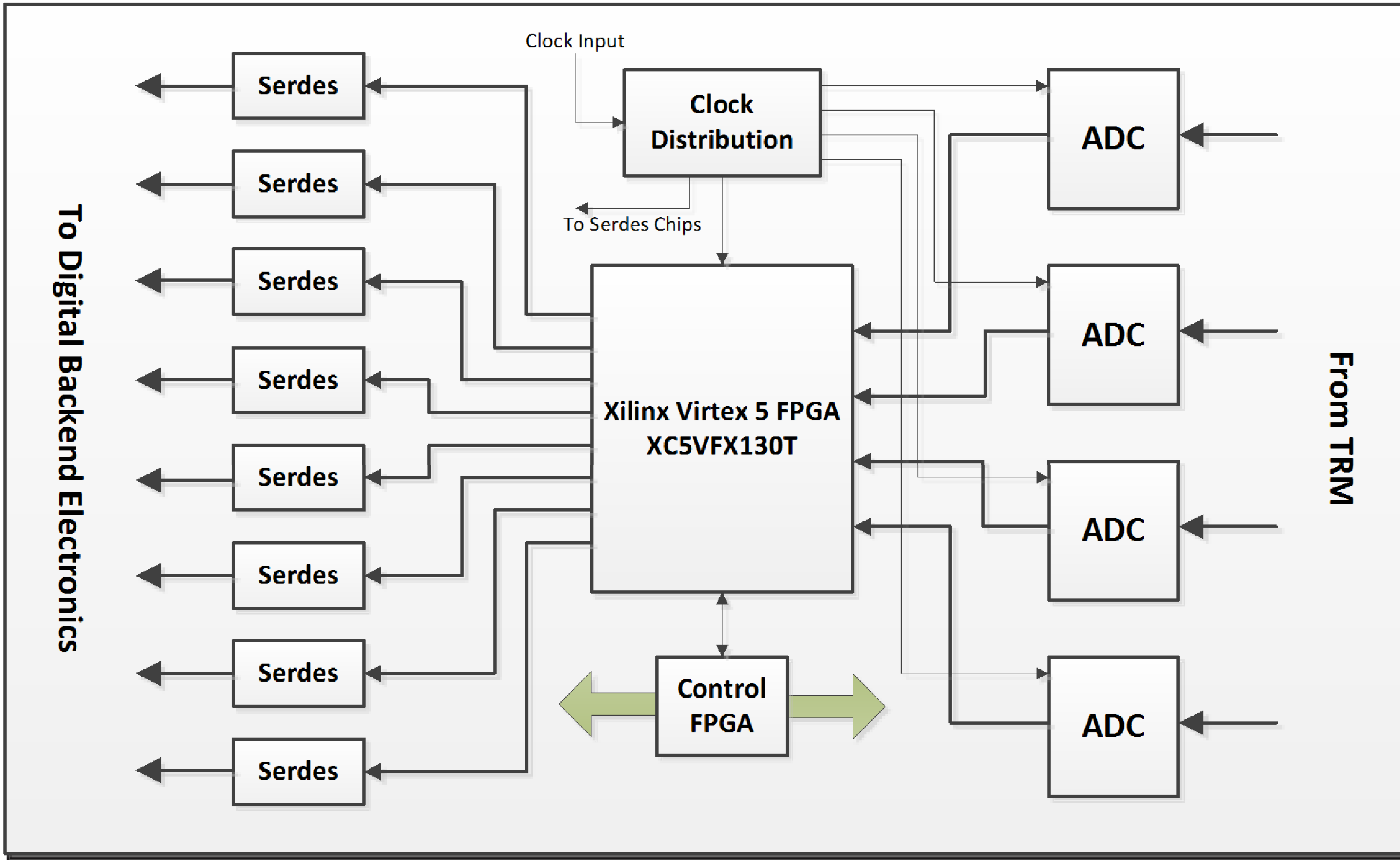
- Implementing the SweepSAR technique using an Array-Fed Reflector Antenna has these benefits:
  - On Transmit, all Feed Array elements are illuminated *(maximum Transmit Power)*, creating the wide elevation beam
  - On Receive, the Feed Array element echo signals are processed individually, taking advantage of the full Reflector area *(maximum Antenna Gain)*



Motivation for qFSP

- In order to enable SweepSAR, receive beams need to be digitized individually which leads to a significant increase in channel count
- Digital beam forming is needed to smooth out the antenna response
- Other digital signal processing is needed to reduce the exorbitant data rates
- 4 channel architecture maximizes resource utilization on the FPGA while reducing board count required for the proposed DESDynI radar system

Block Diagram

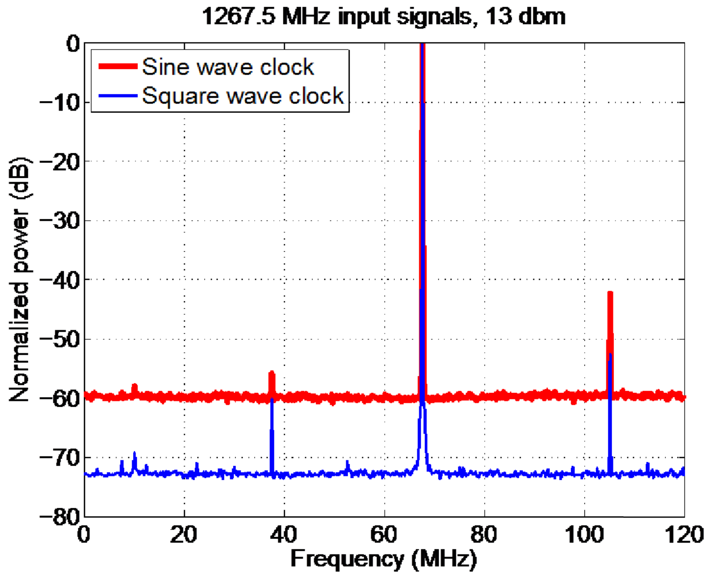


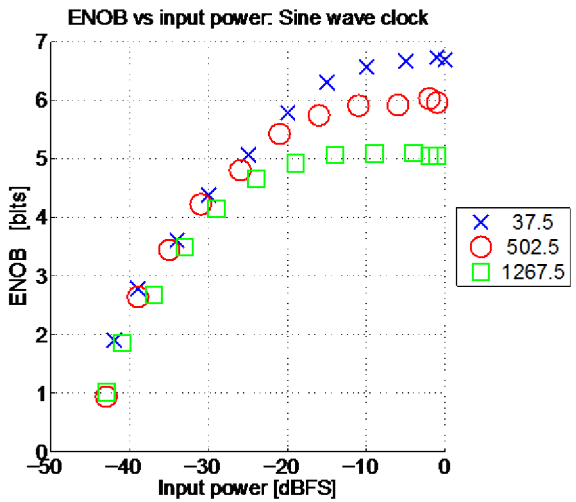
Testing

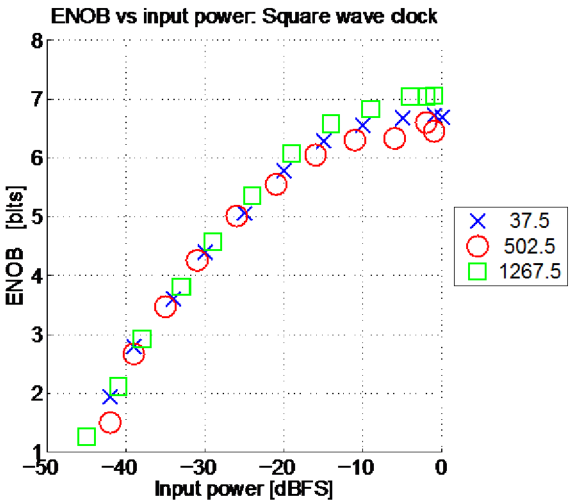
- We have validated all of the interfaces of this prototype version of the qFSP
- Preliminary testing shows that clock jitter is the primary limitation to ADC performance
- Initial characterization shows close to 50dB channel to channel isolation
- Spurious free dynamic range was measured to be at least 52dB
- Conducted single channel algorithm validation from analog input to high speed serial output

Clock Jitter

- Using sine wave clock input, data analysis of captured ADC data showed 3ps clock jitter
- Switching to a square wave clock input reduced noise floor by 12dB and improved clock jitter to about <800fs
- Our conclusion is that single ended to differential conversion in the clock distribution has a high contribution to clock jitter
- Work is ongoing to develop a better clock input stage to minimize the effect of clock jitter
- Currently the best performance, limited by input clock jitter, is 7 bits ENOB







Future Work

- Implement improved clock input circuit design to reduce clock jitter
- Complete full multi-channel algorithm validation in hardware
- Design and validate mechanical enclosure and thermal relief system
- Reduce area and improve efficiency for EM design