

# SKA CSP Consortium: Capabilities and Interests of JPL

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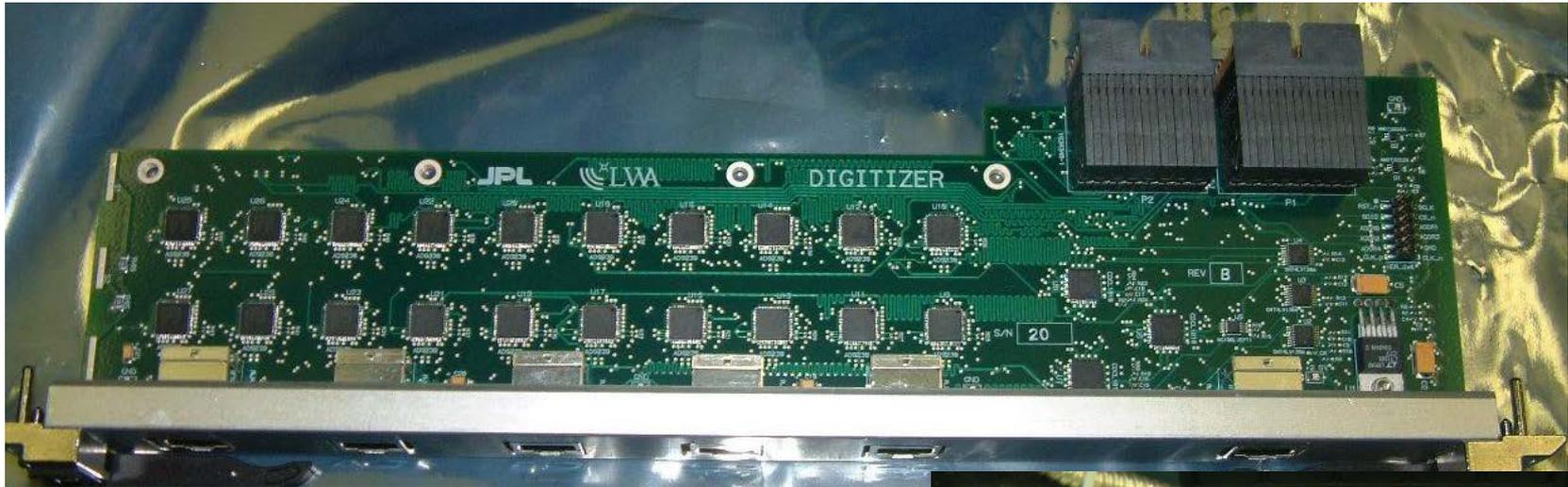
- High speed PCB design
- Analog and mixed-signal PCB design
- FPGA programming
- Radio telescope system design, all aspects and levels
- Real-time and embedded software
- ASIC design and testing
  - Synthesis from standard-cell libraries; incorporation of external IP
  - Subsidized prototyping via TAPO for US-government sponsored work
  - Normally outsource physical design

- Architecture and requirements definition for all sub-elements
  - Tradeoff studies
  - Low power strategies
- Design of low-power electronics
- ASIC designs for
  - Correlators
  - Beam formers
  - Filter banks
- Chip-level and board-level prototyping and testing during pre-construction [1]
- Full production of one or more sub-elements during phase 1 construction [2]

[1] Would require more funding than is currently envisioned.

[2] Would require US becoming a member of the SKA Organization.

# Example: LWA Station (New Mexico)

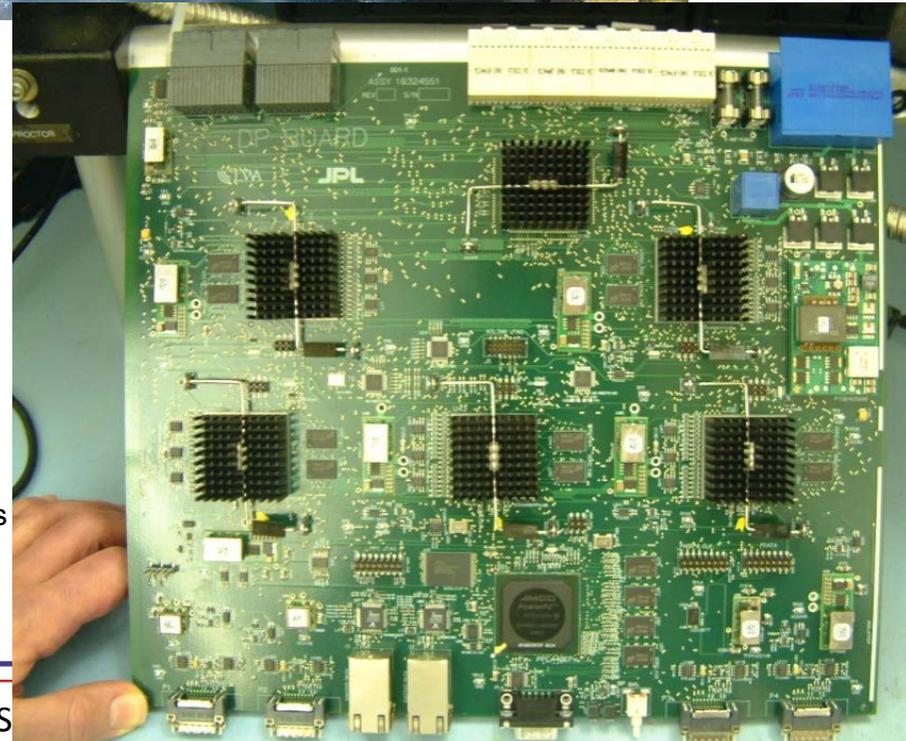


## Digitizer Board (above)

- 16 layer custom printed circuit board
- 20 Analog Devices AD9230 ADCs digitize 20 input signals
- Signals are sampled at 196 MHz with 12 bit resolution
- Provides 1 Hz and 196 MHz clocks for Digital Processing Board
- Interface to ADC chips implemented using an I2C to Serial Peripheral Interface (SPI) converter chip

## Digital Processing Board (right)

- 20 layer custom printed circuit board
- PPC440EPx embedded processor
- 5 Xilinx Virtex-5 XC5VSX50T FPGAs
- 14 64-MB RAM modules
- 2 1 GbE physical interface chips
- 4 10 GbE CX4 connectors



# More Examples of Recent Projects

Portable Radio Science Receiver  
(in Shipping Container)



Very Long Baseline Interferometer  
(VLBI) Processor Racks



Entry Descent and Landing  
Data Analysis System



Site Test Interferometers



IF to Digital Converter Board  
for DSN Downlink Array



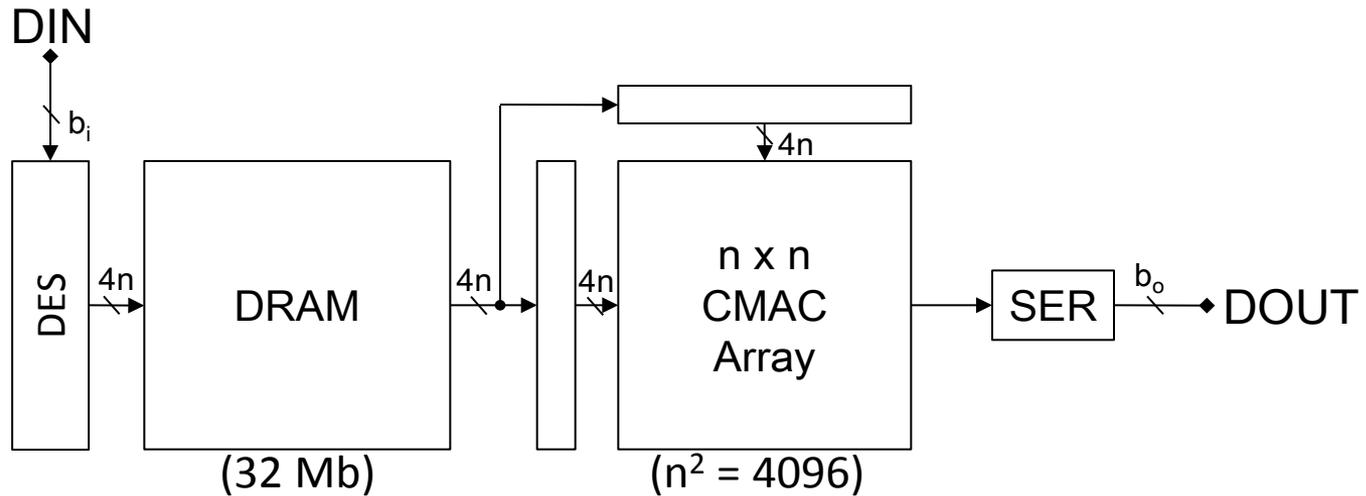
# More Examples

Uplink Array Demonstration



Deep Space Network Downlink Array





- Basic idea:
  - A fairly large embedded RAM buffers samples of all  $2N$  signals from  $N$  antennas of a large telescope. Enough samples are buffered for one integration.
  - An array of complex multiply-accumulate (CMAC) modules is re-used multiple times to compute all cross- and self-correlations among the  $2N$  signals.
  - Signals are broken into channels by frequency, and each correlator chip handles part of the bandwidth. Each sample goes to one and only one chip.

- For  $N = 256$ ,  $B \sim 60$  MHz (LWA)
- LEDA design: 24x Nvidia Kepler GPUs w/ host CPUs [Greenhill 2012]
  - Each GeForce GTX690 card: 281W ("typ 3D"; 329W at "max 3d")  
<http://forums.atomicmpc.com.au/index.php?showtopic=264>
  - Host CPU and I/O at least 100W
  - Total for 57.26 MHz bandwidth **9,144W**
- Proposed ASIC: Single board, 16 ASICs and 1 Virtex 7 FPGA
  - Each ASIC does 3.1 MHz bandwidth, uses 0.44 W (estimate from scaling)
  - Total ASIC power 7.03 W
  - FPGA for board-level I/O 3.41 W (Xilinx Power Estimator)
  - Overhead for power supplies, cooling 100%
  - Net power for entire 62 MHz BW **20.9 W**

- For  $N = 256$ ,  $B \sim 60$  MHz (LWA-OVRO, under construction)
- LEDA design: 24x Nvidia Kepler GPUs w/ host CPUs [Greenhill 2012]
  - Each GeForce GTX690 card: 281W ("typ 3D"; 329W at "max 3d")  
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# Proposed CSP Contributions

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- Internally funded projects are doing relevant investigations
  - Low power architectures for large-N telescopes
  - ASIC design (architectural level) for critical functions: correlation, filter banks, beam formers
  - Detailed logical level design for demo correlator ASIC already complete
    - efficient for  $N=32$  to  $N=1024$
    - very low power
  - Low frequency array optimization (HERA II)
- Can contribute to these CSP deliverables in Stage 1:
  - Architecture Definition Documents for all three correlators
  - ADD for SKA1-mid beamformer
  - ADD for SKA1-low station beamformer (not CSP)
  - High level design of filter bank ASIC (feasibility demo)
  - High level design of beam former ASIC (feasibility demo)
- Service on review, advisory, and inter-task panels is possible.
- Contributions small, only  $\sim 0.5$  FTE total, but hopefully useful.

# Mechanism of Contributions

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- Obviously, we cannot lead any important work packages, even if that were allowed.
  - Can contribute only as a participant
  - NRC's rules require us to collaborate with a work package leader
- I am not authorized to make any commitment for JPL at this time.
- Discussions of a collaborative agreement to contribute via NRC-Canada will occur this week.
- If any other work package leaders would like contributions from JPL, we are open to such discussions.