A 2x2 W-Band Reference Time-Shifted Phase-Locked Transmitter Array in 65nm CMOS Technology

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***Abstract* — This paper presents a complete 2x2 phased array transmitter system operating at W-band (90-95 GHz) which employs a PLL reference time-shifting approach instead of using traditional mm-wave phase shifters. PLL reference shifting enables a phased array to be distributed over multiple chips without the need for coherent mm-wave signal distribution between chips. The proposed phased array transmitter system consumes 248 mW per array element when implemented in a 65 nm CMOS technology.**

Index Terms — PLL Reference Time-Shifting, W-band, Phased Array Transmitter

I. Introduction

Phased array transmitter systems have appeared in CMOS technology at frequencies up to W-band for applications including raster scanning for mm-wave imaging, scanning for radar systems, and beam-steering for wireless communications [1,2,3]. Phased array transmitters offer many advantages including the elimination of mechanical scanning for imaging, and the ability to improve the SNR of a wireless link with the same amount of transmitted power.

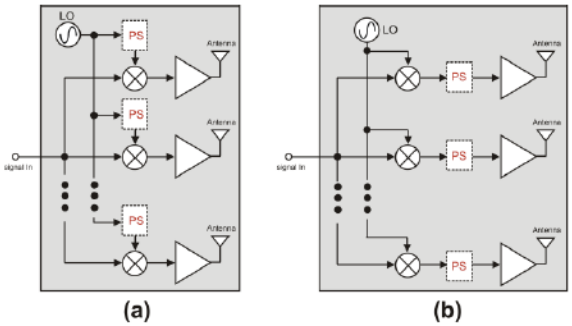

Fig. 1. Conventional phased-array transmitter system showing LO distribution with a phase shifter placed in: (a) LO path. (b) RF path.

As shown in Fig. 1, existing phased array transmitters use a mm-wave phase shifter placed on either the LO path or RF path to achieve phase control of the carrier for each element in the array. While this technique works well for smaller array sizes with a limited number of elements, one requirement is that the mm-wave frequency LO must be distributed to each element from a single source to retain phase coherence. For small arrays where all the elements can be placed on the same die this is less critical as mm-W carriers are relatively easy to distribute on-chip. As the number of elements is increased the die size will also increase, leading to lower yields and in turn, higher costs. The obvious solution is to separate the array into multiple chips, each containing one or more transmit elements in order to limit the required die size. While this approach seems intuitive, it is actually extremely difficult to implement as the mm-wave LO would need to be distributed to multiple chips in the array. Advanced low-loss mm-wave packaging is quite expensive, and conventional low cost wire-bonding exhibits high losses at mm-wave frequencies.

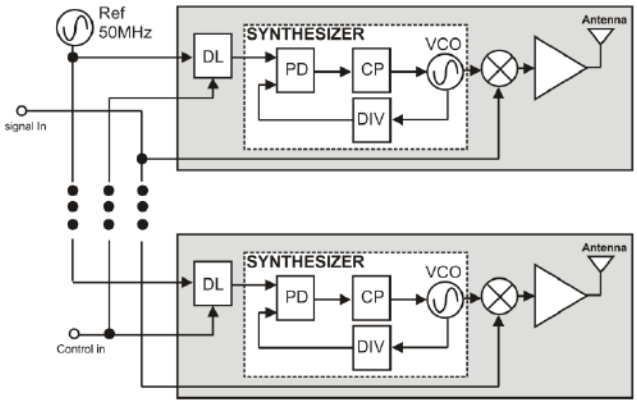

Fig. 2. Block diagram of the reference time-shifted phase-locked transmitter array with frequency synthesizers in each element.

To overcome the challenge of mm-wave LO distribution in multi-chip phased arrays, we propose the reference time-shifted phase-locked transmitter array with block diagram shown in Fig 2. Each die in the array contains both a transmitter chain and a frequency synthesizer in order to provide phase coherence. Instead of directly distributing the mm-wave LO between each chip of the array, we instead distribute a low frequency (54 MHz) reference signal to each chip's PLL, which then synthesizes a coherent mm-wave carrier at W-band. Unlike mm-wave frequencies, distribution of a 50 MHz reference signal is relatively easy on a conventional FR-4 PCB board. While including a synthesizer in each array element seems costly, the area and power overhead is actually quite reasonable. Of the measured 248 mW for each element the synthesizer only accounts for 85 mW (34% overhead). Also the entire element chip occupies 2.25mm^2 of silicon area while the synthesizer itself only

occupies 0.21 mm^2 (11% overhead). In order to provide the required phase control a digitally controlled delay line (denoted DL) is introduced at the reference input of each chip. This delay line allows for the phase of each transmitter to be adjusted relative to the rest of the array through a digital control system. Beyond beam-steering and beam-forming operations, the delay line also allows for the suppression of systematic delays in the reference signal between elements due to asymmetric PCB routing.

II. ARRAY ELEMENT DESIGN

Each element of the proposed reference time-shifting array is itself a small system-on-chip (SOC) containing digital, RF, and mixed-signal circuits. Figure 3 shows a general block diagram of the array element chip.

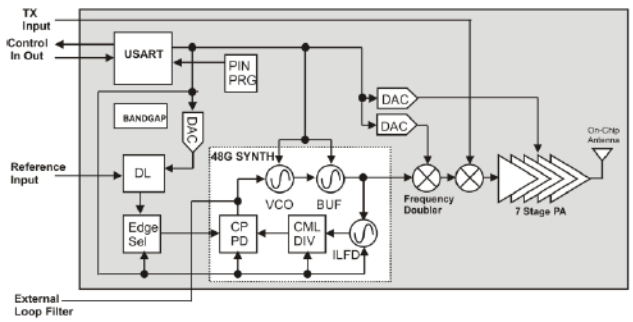

Fig. 3. Block diagram of reference time-shifting phased array transmitter element chip.

The frequency synthesizer design was previously presented in [4]. It delivers a carrier between 42 and 50 GHz and is cascaded with a frequency doubler to provide the final W-band carrier. The doubler itself is a rectification based frequency multiplier which converts an odd-mode tone at f_o into an even mode tone at $2f_o$. A gilbert-cell mixer is used to modulate this 100 GHz carrier before passing it to the power amplifier and on-chip dipole antenna.

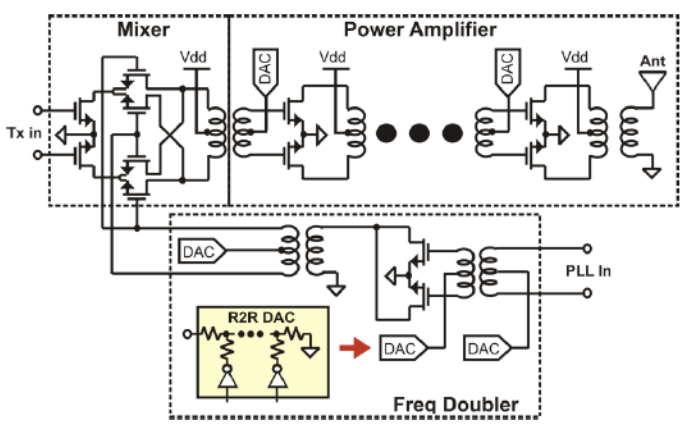

Fig. 4. Detailed schematic of W-band front-end for the reference time-shifting phased-array transmitter.

Low speed R2R DACs are used to control the biasing conditions of the frequency doubler, power amplifier, and synthesizer components. The power amplifier itself is a fully differential transformer-coupled structure. Figure 4 contains a detailed schematic of the W-band front-end.

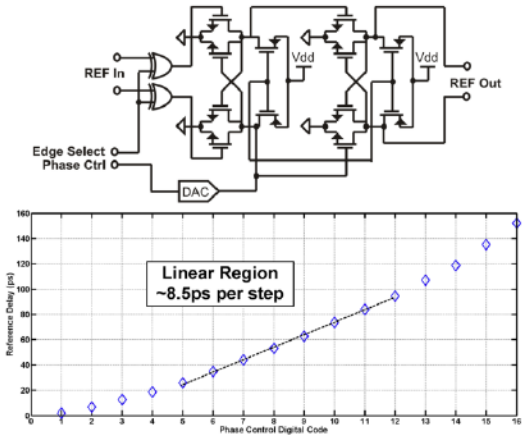

Fig. 5. Digitally controlled delay line and simulated delay for each digital code.

The digitally controlled delay line is implemented as a two-stage voltage-controlled cross–coupled diff-pair as shown in Fig 5. Two XOR gates pre-select which edge the phase detector within the frequency synthesizer will lock to. Also shown in Fig. 5 is the simulated absolute delay vs. digital code. In the linear region of the delay line the slope is approximately 8.5 ps per step which corresponds to 30° of phase at the 90-100 GHz output of the frequency doubler.

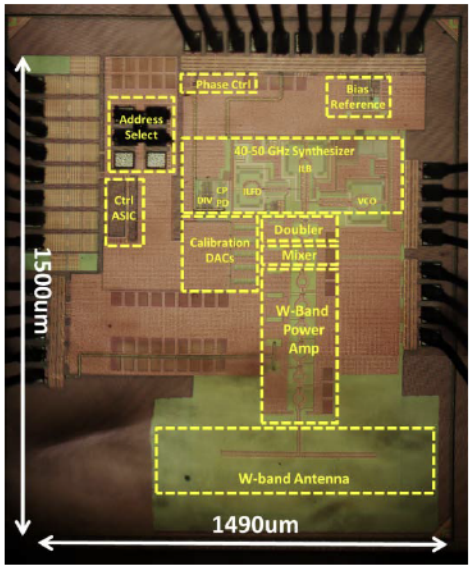

Fig. 6. Chip micro-photograph of the reference time-shifting phased-array transmitter SOC-element showing major circuit blocks.

As there are multiple identical elements in the same array, the control ASIC uses 3 sets of internal pads to program the chip address (unique out of 2^3) on the array control bus as seen in the die photo (Fig. 6). Adding more address bits for digital control is relatively trivial but in this prototype only 3 bits

were used to save die space. The control bus is a serial USART which interfaces to a PC. USART packets carry the settings for each calibration DAC and PLL adjustment in the SOC, as well as the phase control selection.

III. MEASUREMENTS

In order to measure the reference time-shifting array, a PCB module containing four elements was constructed. A W-band mixer (Agilent 11970W) and W-band horn were positioned so that equal power was received from each of the 4 chips in the array (this was determined by disabling each PLL and changing the horn position to balance the power captured from each individual chip). The setup is shown in Fig 7a.

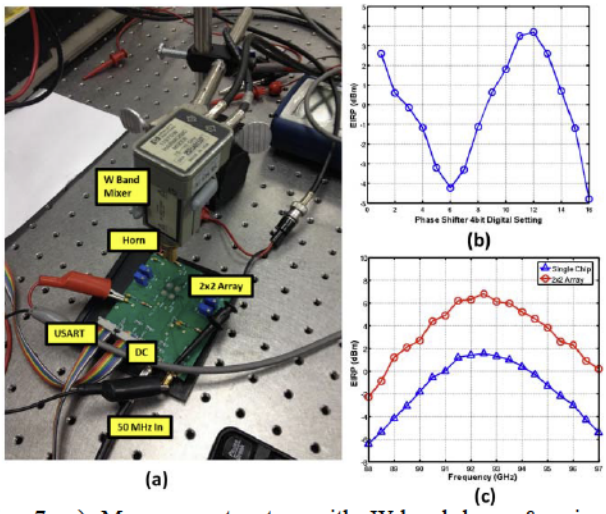

Fig. 7. a) Measurement setup with W-band horn & mixer. b) Estimated EIRP with two chips enabled as the phase shifter setting is varied. C) Optimized power of one chip vs. power of full 2x2 array.

First we enabled only two elements of the array and monitored the received power as the delay control code was swept on one chip. Using the known horn gain and known distance from the array surface the EIRP is estimated as shown in Fig. 7b. Interesting to note the minimum and maximum power occur 6 digital codes apart, which agrees with the delay simulation in Fig. 5, where each code step is 8.5 ps and corresponds to approximately 30° at W-band. Since 180°/30° = 6 we would expect 6 codes between the in-phase (maximum) and anti-phase (minimum) combining. The combined power is not exactly double the single element power (or exactly zero), as the phase is not perfect and the delay line will exhibit some INL and DNL (step size errors). Next we measure the maximum power from both a single element and the full array across the frequency band from 88-97 GHz. At each step the phases were re-optimized for maximum power. The frequency was adjusted by changing the reference frequency (50-54 MHz). As seen in Fig. 7c, the combined power of the phased array is approximately 5.5 dB above the single element power. While the ideal 4-way power combining should be 6 dB the non-linearity and step errors of the delay line will again cost some combining efficiency. This result however shows that the power is indeed combining in-phase and that phased array operation has been achieved through time-shifting the reference signal of the PLL.

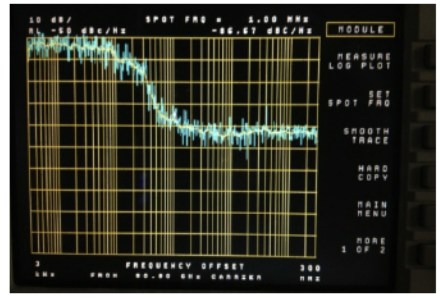

Fig. 8. Measured phase noise at the output of one element of the phased array.

The phase noise at one element was measured through the W-band mixer and shown in Fig 8. In [4] a phase noise of -93 dBc/Hz at 1 MHz offset was reported at 48 GHz. With the doubling operation, a 6 dB phase noise increase is expected, so we anticipate a phase noise of -87 dBc/Hz at the same offset. This agrees well with the measurement of -86.67 dBc/Hz. Note the measurement is not valid beyond 3 MHz as the phase noise intercepts the mixer's thermal floor.

IV. CONCLUSIONS

We have demonstrated that phased-array operation can be achieved by incorporating a frequency synthesizer into each element and time-shifting the incoming reference signal. This overcomes the problem of having to distribute high frequency mm-wave LO's between multiple chips in large arrays. The prototype chip consumes 248 mW of power (PLL 85 mW, doubler 31 mW, PA 132 mW) and occupies 2.25 mm^2 of chip area when implemented in 65 nm technology.

ACKNOWLEDGEMENT

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