

The DUV stability of superlattice-doped CMOS detector arrays

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JPL and Alacron have recently demonstrated a high-speed CMOS camera capable of deep ultraviolet (DUV) imaging with high quantum efficiency (QE) and exceptional stability and long-term reliability (Figure 1). Eight-inch wafers comprising 64 CMOS detector arrays were bonded to a silicon wafer for mechanical support and back-thinned at JPL to expose the 5 μm epilayer (Figure 2). JPL processed the thinned detector for back-illumination at full 8-inch wafer scale using a production-scale Veeco molecular beam epitaxy (MBE) and atomic layer deposition (ALD) systems. DUV-stable surface passivation was achieved using JPL's newly-developed superlattice doping technology. The antireflection (AR) coating was comprised of a single layer of ALD-grown Al_2O_3 . Superlattice doped, AR-coated CMOS detectors achieved 64% peak QE at 263 nm, and are the only imaging detectors known to have survived direct, long-term irradiation by DUV excimer lasers with no measurable degradation in performance.

In this paper, we present experimental results and band structure calculations that illuminate the unique properties of superlattice-doped detectors. Numerical band structure calculations are presented to analyze the dependencies of surface passivation on dopant profiles and interface trap densities (Figure 3). Experiments and calculations show that quantum-engineered surfaces, grown at JPL by low temperature molecular beam epitaxy, achieve a qualitative as well as quantitative uniqueness in their near-immunity to high densities of surface and interface traps.

Also in this paper, we briefly describe the physics and chemistry of doped silicon surfaces, and lay out the principles of quantum engineering that underlie the unique capabilities of superlattice doped detectors. Due to its importance to the semiconductor industry, the Si-SiO₂ interface has been exhaustively studied for the last fifty years. Surface passivation is required for stable and reliable performance of virtually all semiconductor devices, and yet even Si-SiO₂ interfaces formed at high temperatures are riddled with vacancies and dangling bonds. Low interface trap densities are only possible because hydrogen prevents such defects from being electrically active. Exposure to deep ultraviolet light injects energetic carriers into the oxide, which degrades the oxide by causing hydrogen to be released from defect sites. Back-illuminated detectors are more susceptible to this type of damage, because process constraints limit back surface passivation processes to relatively low temperatures. The surface and interface traps thus formed are subject to time and temperature dependent charging and discharging phenomena, which give rise to both temporary and permanent changes in quantum efficiency and dark current in back-illuminated imaging detectors. Surface passivation technologies that depend on low surface/interface defect densities, including ion implantation and chemisorption, are therefore vulnerable to DUV-induced damage and device failure. The DUV stability of superlattice doped detectors is predicted by the insensitivity of the surface band structure to DUV-induced interface traps and confirmed experimentally.

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Figure 1: Alacron CMOS imaging camera with front-illuminated CMOS imaging array.



Figure 2: Eight inch diameter wafer in silicon molecular beam epitaxy system during superlattice passivation process. Each wafer comprises ~64 CMOS imaging arrays, each having 1500x2000 resolution.

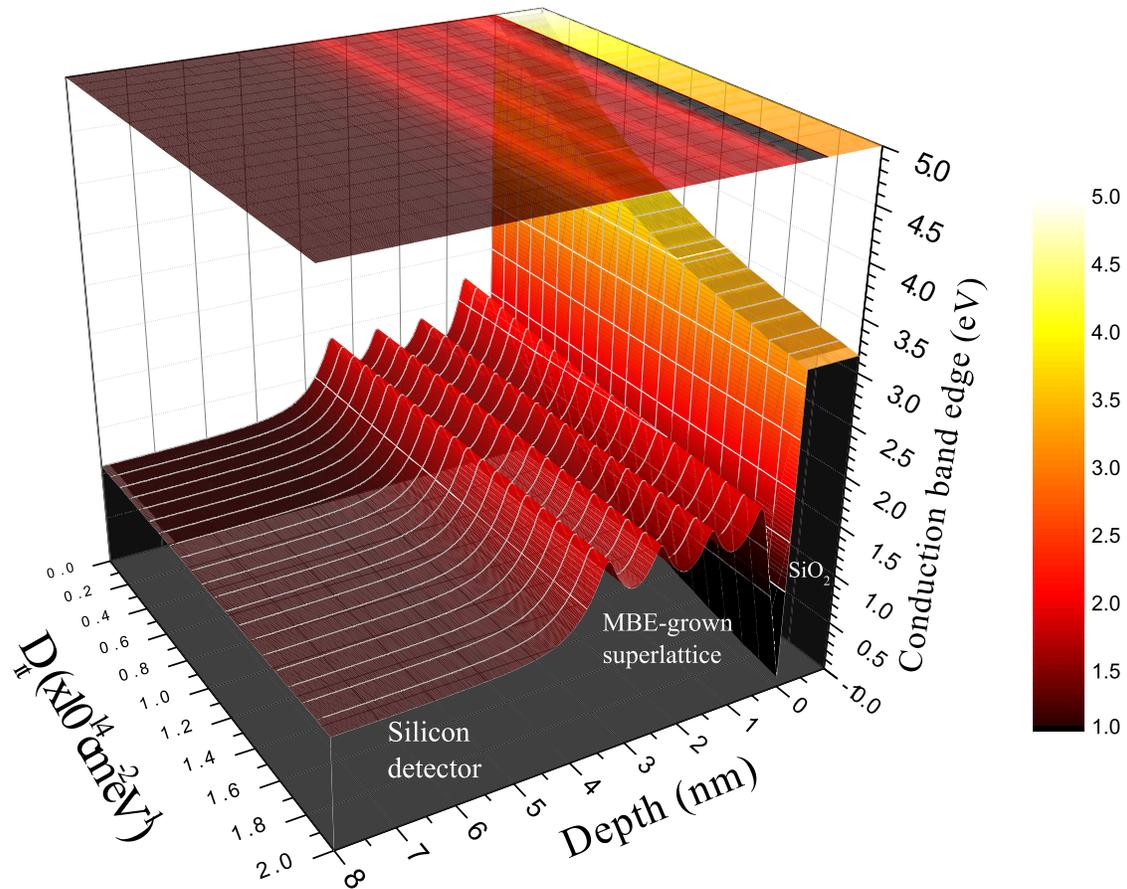


Figure 3: The stability of superlattice-doped CMOS detectors against long-term exposure to DUV lasers is predicted by the insensitivity of superlattice-doped surfaces to extremely high interface trap densities. This figure simulates the effect of interface traps on superlattice-doped surfaces. Simulations of conduction band vs. depth are plotted for MBE-grown superlattices with varying interface traps densities. Conduction band edges versus depth from the surface are plotted in the x-z planes, with energies ranging from 0 to 5 eV along the z-axis, and depths ranging from -1 to 8 nm along the x-axis. The simulations locate the Si-SiO₂ interface at a depth of 0 nm, with interface trap densities, D_{it} , varying along the y-axis from 0 to 2×10^{14} traps/cm²/eV. The MBE-grown superlattice represented in these computations is comprised of four delta-doped layers located at depths of approximately 0.5, 1.5, 2.5, and 3.5 nm. For reference, a 2D projection of this plot is shown at the top of the figure, in which the conduction band energy is represented by color according to the key at the right.

Three notable properties of superlattice doped surfaces are illustrated by the figure:

- (1) Thermal electrons are prevented from interacting with traps at the Si-SiO₂ interface by a potential barrier approximately ~1eV in height;
- (2) The height and width of the potential barrier are virtually independent of interface trap density, up to densities that are never reached in practice (with the exception of a silicon surface freshly-cleaved in an ultrahigh vacuum chamber);
- (3) The observed DUV detector stability is enabled by the near atomic scale control over surface doping that is achieved by MBE growth.