Maestro Path to Flight Study

Rafi Some, Dwight Geer and Alan Lee
Jet Propulsion Laboratory
California Institute of Technology
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## Agenda

- Motivation & Future NASA Needs
- The OPERA Program
- Maestro Status
- MCP SBC Path to Flight
  - Maestro Processor Path to Flight
  - DDR Path to Flight
  - MCP SBC H/W Development
  - MCP SBC S/W Development
- Conclusions/Recommendations
Future NASA Missions Require High Performance Processing

Mars Observing Opportunities

- Mars Science Laboratory
  - 5-20km in 24 months

Earth Observing Opportunities

Ref: Decadal Survey Workshops and other sources

- HyspIRI*
  - 3.2 TBytes per day data rate

- ASCENDS-CO2LAS*
  - 500 GBytes per hour data rate

- DESDynI*
  - 4.9 TBytes per day data rate

- ACE-MSPI*
  - 95 MBytes/sec data rate for each of 9 cameras

- ExoMars/TGO
- Mars Astrobiology Explorer-Cacher (MAX-C)
- Mars Sample Return
  - Acquire 34 samples
  - 10-30km in 6-12 months

Mars Science Laboratory (based on MRO/Odyssey)

MAVEN Scout

MAVEN Scout (based on MRO/Odyssey)

# 3 Distinct Classes of On-Board High Performance Processing

<table>
<thead>
<tr>
<th>Class of Computation</th>
<th>Science Mission Applications</th>
<th>Objective of Computation</th>
<th>Computing System Characteristics</th>
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</thead>
<tbody>
<tr>
<td>High-throughput Science Data Processing</td>
<td>High resolution sensors, e.g., SAR, Hyperspectral</td>
<td>Downlink images and products rather than raw data</td>
<td>Dedicated payload processors at sensors requiring less stringent fault tolerance</td>
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<tr>
<td>Short-Duration Real Time (R/T) Burst Calculations</td>
<td>Entry, Descent &amp; Landing (EDL), e.g., vision-based pinpoint landing and hazard avoidance</td>
<td>Achieve most robust results within available timeframe as input to control decisions</td>
<td>High peak performance and compute intensive with stringent fault tolerance and real-time requirements</td>
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<tr>
<td>Intensive Search-Based Reasoning (may be Non-R/T)</td>
<td>Mission planning, fault management, model-based reasoning</td>
<td>Accomplish opportunistic science; mitigate execution failures via contingency planning; detect, diagnose and recover from faults</td>
<td>Memory intensive, high throughput required, but less real time and less stringent fault tolerance.</td>
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</tbody>
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OPERA Program Overview
On-board Processing Expandable Reconfigurable Architecture

1999-2006
DARPA
Polymorphic Computing Architecture

2005-2009
DARPA/DTRA
RHBD

OPERA Program
2006-2011
Hardware & Software Development
Oct 06 – Sept 10

49 Core RHBD Chip April 10 and Development Board Sept 10

US Space Community

Tilera Multi-core Processor + RHBD => 49 Core RH Processor

OPERA Components

- **Hardware – Maestro Chip**
  - 49 core general purpose multi-core processor
  - Up to 350 MHz
  - Four - 10 Gbps SERDES XAUI interfaces
  - Radiation Hard By Design (RHBD)
  - Developed by Boeing SSED
    - Uses Tilera Corporation IP
    - Additional third party IP

- **Software**
  - Basic compiler tools
    - Complements Tilera’s toolset
  - Benchmark code
  - Performance and productivity tools
    - Parallel libraries, analyzer, debugger, run time monitor, OS ports

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Maestro Provides Good Performance Over a Wide Range of Applications and Comes with a Bundled S/W Suite Supporting Multiple Operating Systems

Maestro, Key Features

- Highest Performance Rad Hard General Purpose Processor
  - Up to 350 MHz, 44 GOPS, 20 GFLOPS
- Tiled Architecture
  - 49 tile, 2-D Processor Array connected by low-latency high bandwidth register-mapped networks
- Tile Processor
  - Main Processor: 3-way VLIW CPU
    - 64-bit instruction bundle
    - 32-bit integer operations
  - Static Switch Processor
  - Floating Point Co-Processor (IEEE 754 single and double precision)
- Memory
  - L1 cache: 2 cycle latency, 8KB I & 8 KB D
  - L2 cache: 7 cycle latency, 64 KB
  - Tiles can access each others L2
  - Off-chip Main Memory: 88 cycle latency
- I/O Interfaces
  - Four XAUI (10 Gigabit Ethernet Attachment Unit Interface)
  - Four DDR2 (double data rate SDRAM)

May 23, 2011
Maestro Status, as of Apr-2011

- Functional and Parametric Tests Completed
  - Passed with Minor Errata

- A JPL Led Maestro Radiation Testing Consortium Has been Organized:
  - Boeing Functional/Radiation test board and Radiation Effects Models
  - JPL / Honeywell co-development of Radiation Test S/W
  - JPL Beam Time

- Maestro development board from Boeing is on track for May-2011 delivery

- Maestro software tools 2.0.2 released

- VxWorks port to Tilera completed

- Lacking Rad Hard DDR Memory
MCP SBC Path to Flight

- Define a Path for a Multi-core High Performance Space Qualified Flight Computer Suitable for use in:
  - High-throughput Data Processing
  - Short Duration R/T Burst Calculations
  - Intensive Search Based Reasoning
- Leverage the Results of the OPERA Program
- Meet Power, Performance, Reliability Requirements at Chip and Board Levels
  - Target the MSL Environmental Requirements (thermal, dynamics and radiation)
- Include Additional Necessary Developments
  - DDR Memory
  - High Throughput I/O
  - Tailoring the Maestro Processor for NASA Missions
  - System S/W and Libraries

Maestro Processor Path to Flight

• Challenges with Flying Current Maestro
  – High Power Consumption and Heat Dissipation
  – Special packaging design required
  – Not space qualified

• Path to Flight will require:
  – Design improvements to address power and fault protection issues
    • Maestro-Lite is a proposed lower power processor
  – Custom package development and qualification
    • Based on MIL-PRF 38535 Class Y
  – Development of a NASA approved qualification flow to include:
    • Qualification of foundry wafer level technology performance
    • Extensive life test and burn-in screening
    • Development of compatible QML level Q/V flow
DDR Memory Path to Flight

- **Challenges with DDR2 Memory**
  - Space qualified Rad Hard/Tolerant DDR2 Does Not Exist
  - High Power Consumption
  - Memory Controller Can’t Tolerate Whole Chip Failures

- **Path to Flight Options for DDR Memory**
  - Commercial DDR2
    - Likely to Meet TID, but not SEE Challenge
      - Extensive up screening of COTS parts
      - Requires an error correction engine (to deal with upsets or chip failure)
    - Power Consumption/Thermal Management issues remain
  - Designing New DDR2 Using RHBD
    - Truly RH DDR
    - Minimized Power Consumption
  - Qualification will require:
    - Qualification of foundry wafer level technology performance
    - Extensive life test and burn-in screening
    - Development of compatible QML level Q/V flow
MCP SBC H/W Development

- MCP Single Board Computer
  - SBC Bridge
    - Requires a bridge function to adapt to the S/C host bus
    - Requires parts qualification/certification for Flight
  - SBC ancillary logic
    - Need space qualified 10GbE components (for Maestro XAUI ports)
    - Need space qualified RMGII (for Maestro Reduced Gigabit Media Independent Interface ports)
    - Requires parts qualification/certification for Flight
  - Qualification will require:
    - Qualification of foundry wafer level technology performance
    - Extensive life test and burn-in screening
    - Development of compatible QML level Q/V flow
  - Mission level environmental requirements
    - End-to-End Development including Qualification Testing
      - Example requirements: MSL Environmental Requirements
  - Goal is for Vendor development and productization
MCP SBC S/W Development

- Enhanced Software Suite
  - Porting Remaining VxWorks Modules to baseline Maestro
  - Porting Parallel Libraries to VxWorks
  - Additional Enhancements for Maestro Lite:
    - Power management
    - Error Detection/Correction on internal buses
    - Ability to route around powered down or disabled nodes
    - Ability to work with arbitrary array configuration
    - Ability to provide time sync
    - Ability to use XAUI port as simple high speed I/O port with min protocol overhead
    - Fault tolerance library

Conclusion/Recommendations

- **Maestro Based Options:**
  - Heat, Power and Fault Tolerance Issues Impose Limitations on Applicability

- **Commercial DDR Die Based Options:**
  - Desired Levels of RH Not Achievable via Packaging Alone

- **M-45nm with RHBD DDR3 Memory**
  - Pushing Technology Farthest Ahead
  - Smallest Footprint, Highest Die Yield
  - Desirable, but Higher Cost

- **M-Lite with RHBD DDR2 Memory**
  - Acceptable Power, Speed, Reliability, Board Level Packaging and Thermal Mgmt.
  - All Known Issues/Concerns/Challenges are Addressed
  - Most likely to Be Adopted by Any Mission without Operation Limitations
  - Best Option based on Near Term Desired Capabilities, Technology, Schedule and Cost
  - Qualification issues must still be addressed
BACKUP
M-Lite, M-LPlus and M-45nm

• **Maestro-Lite (M-Lite)**
  – Address Concerns with Current Maestro
    • Reduce the Number of Tiles from 49 to 25 or 16 for Further Power and Heat Reduction
      – Over 10 W power reduction expected
    • Provide Clock and Tile Management for Further Power and Heat Reduction
    • Improve Fault Tolerance
      – Clock and Cache Size Enhancement
      – Optimize I/O Interfaces

• **Maestro-Lite Plus (M-LPlus)**
  – M-Lite + Modified DDR Controller to Support DDR3
  – Re-layout for Smaller Die and Smaller Package
  – Enhanced Yield and Packaging

• **Maestro-45nm (M-45nm)**
  – M-LPlus + Enhanced Cache and FPU
  – Updated RHBD Lib for 45 nm fab line
  – Smaller Die, Smaller Package and Lower Power