

# Modeling from Local to Subsystem Level Effects in Analog and Digital Circuits due to Space Induced Single Event Transients

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**Abstract:** Single Event Transients in analog and digital electronics from space generated high energetic nuclear particles can disrupt either temporarily and sometimes permanently the functionality and performance of electronics in space vehicles. This work first provides some insights into the modeling of SET in electronic circuits that can be used in SPICE-like simulators. The work is then directed to present methodologies, one of which was developed by this author, for the assessment of SET at different levels of integration in electronics, from the circuit level to the subsystem level.

*Acknowledgment:* The research described in this (publication or paper) was carried out at the Jet Propulsion Laboratory, California Institute of Technology, under a contract with the National Aeronautics and Space Administration.

## I INTRODUCTION

Single Event Transients (SET) in both analog linear and digital circuits are caused by the generation of charges (holes-electrons pairs) deep inside semiconductor components as a result of a single space environment induced proton or heavy ion passing through a sensitive node in an analog or digital circuit. A good explanation of this phenomena, and some of the physics behind it, has been published by this author in reference [1]. A SET is made up of a transient voltage pulse generated at a node of an electrical component, then propagating to the device output, and then reappearing as either the same voltage transient, an amplified version of this transient, a degraded version of the transient, or a change in the logical output. SET in analog linear devices were observed in the Topex/Poseidon

spacecraft [2] and have, since then been identified in other spacecraft, such as Soho [3], Cassini [4], MAP [5], MRO [6], and possibly others. SET in both analog and digital circuits are a very important consideration when designing spacecraft electronics for avionics.

SET have been observed in a variety of linear circuits such as operational amplifiers, voltage references, voltage comparators, analog digital converters and others [7]. SET have also been observed in digital circuits such as inverters, flip-flops, drivers, and receivers [8]. Each SET has its own characteristics (polarity, amplitude, waveform, and pulse duration) depending on the ion or proton, impact location, the ion or proton energy, device bias conditions, and output load. For example, reference [9] shows that for DAC one of the worst case conditions for largest SET events is dependent on the highest supply voltage of the digital to analog converter IC. Figure 1 obtained from references [8,9] shows one of four dominant classes of SET that have been obtained on the LM124 operational amplifier. Figure 2 shows an illustration of a SET in a digital inverter device.

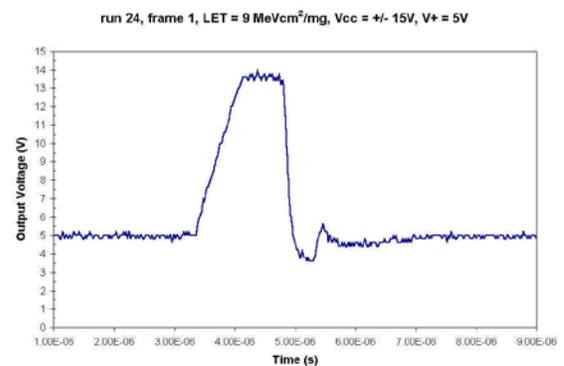


Fig 1. Example of large amplitude, fast recovery time, positive going transient.

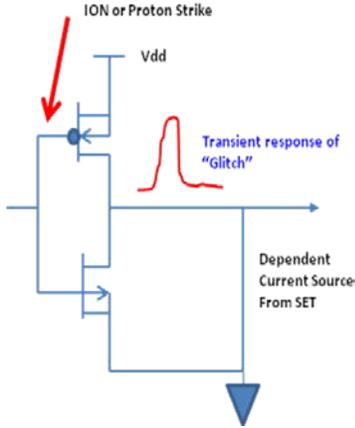


Fig 2. Illustration of a typical SET effect on an inverter device.

## II MODELING SET EVENTS in SPICE MODELS

**Analog Circuits:** Two dimensional device simulations are often used to generate current waveforms as a result of the penetration of heavy ions through all device types used in integrated circuits. These simplifications take into account the bias conditions present for a particular device in a circuit. The transient response can be used as an input for SPICE circuit simulations. This allows for the circuit output to be obtained due to heavy ions strikes on different devices of the integrated circuit, and eventually the propagated output of the whole circuit can be estimated if we model the transient propagation across the circuits.

One of the models developed for a NPN transistor is that shown in reference [10] and illustrated in Figure 3. The model considers the base current indirectly as the sum of the collector and emitter current pulses. However, this model is difficult to implement and evaluate for a linear IC because it is difficult to estimate which of its many transistors should be the recipient(s) of the model described in Figure 3.

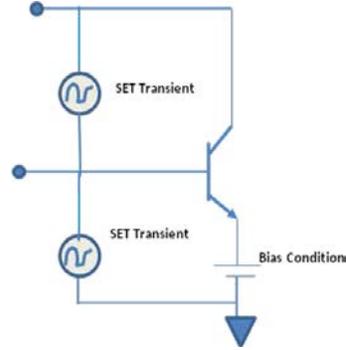


Fig 3. Illustration of SET SPICE modeling for a BJT transistor.

Each different transistor choice produces a different transient output. That transient output must then be propagated to the rest of a circuit as shown in Figure 4 which we discuss as an example.

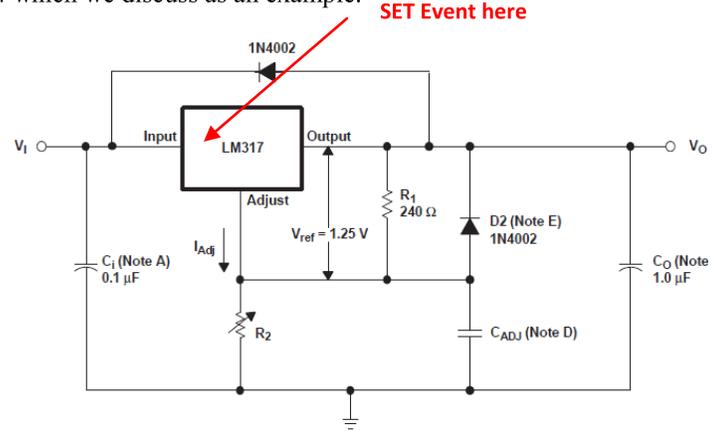


Fig. 4 Adjustable voltage regulator susceptible to a SET

Figure 4 shows an example application of an adjustable voltage regulator (LM137) capable of supplying up to 1.5A with an adjustable output voltage  $V_o$  that can range from 1.25V to 37V. The output voltage is given by

$$V_o = V_{ref} \left( 1 + \frac{R_2}{R_1} \right) + (I_{adj} * R_2) \quad (1)$$

$I_{adj}$  is usually around 50uA in most applications and it is often ignored.  $V_{ref}$  is defined in Figure 4. The LM 137 regulator (with 26 BJT transistors inside) is susceptible to SET, and a SET will cause  $V_{ref}$  to go to zero volts, hence, from equation 1,  $I_{adj} * R_2 = 0$ . A SET can last from a few microseconds up to tens of microseconds, hence,  $V_o = 0$  should last also for the duration of the transient. However, in the circuit of Figure 4,  $C_o$  will improve the transient response and

$C_{adj}$  will greatly improve ripple rejection as it prevents amplification of the ripple as the output voltage is adjusted higher. In this example SET propagation across the circuit has been shown to have little effect.

Because we are often only interested in the behavior of an overall circuit to a SET event, a different approach should be followed. Rather than modeling the internals of the linear IC in order to assess the SET effects on the outputs of the IC, an easier approach is to model just the SET transient on the IC output only. We can then propagate the behavior of the SET to the overall circuit. This approach is illustrated in Figure 5 where a transient pulse is modeled via SPICE on the output of U2. The transient is modeled as V3 using a pulse step function in SPICE. We can then capture the pulse response effect at the circuit load (represented by  $C2 \parallel R5$ ).

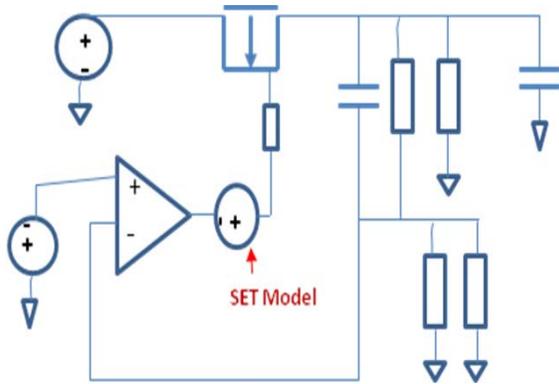


Fig 5. Modeling a pulse (V3) at the output of a susceptible device (U2) due to a SET.

This new approach begs the question as to what pulse type, amplitude, and pulse width should we use? The answer can range from an educated guess to test data, with the latter being the best approach. Many vendors of linear electronic components for the aerospace industry have test data on the susceptibility of their linear components to SET. Test data is often reported and provided to the users of the components when such components are procured. Also, several NASA centers (e.g. GSFC and JPL) keep databases of SET data for the most common linear circuits used in the industry. However, as some components become obsolete and other components are newly manufactured more test data must be generated.

**Digital Circuits:** The simpler topology of CMOS devices which is exemplified by the core of all the CMOS digital devices--the inverter, allows for a more analytical approach. The CMOS inverter with an ion strike was shown in Fig 2. From the work of Messenger [11], the charge deposition can be modeled as a double-exponential current pulse:

$$I(t) = I_0 [e^{-\alpha t} - e^{-\beta t}] \quad (2)$$

Where  $1/\alpha$  is the collection time constant for the junction and  $1/\beta$  is the time constant for initially establishing the ion track (see Fig 2 in reference [1]), and  $I_0$  is given by

$$I_0 = Q\mu NE \quad (3)$$

where  $Q$  is the charge of electron or hole,  $\mu$  is the ambipolar mobility of carriers,  $N$  is the number of electron holes pair generated per unit length and given by the expression in equation 4 [1]

$$N = LET (\text{MeV} \cdot \text{cm}^2 / \text{mg}) * (\text{density of Si} (\text{mg}/\text{cm}^3)) / 3.6 \text{ eV} \quad (4)$$

LET is the heavy ion linear energy transfer. An expression for LET was derived in reference 1 but it can also be measured experimentally for a given component.  $E$  is the electric field component in the direction of the "funnel" (see Fig 2 of reference [1] for illustration of the funnel). The electric field is given by the maximum value of the electric field within the junction in equation 5 [12].

$$E_0 = [(2Q/\epsilon) * (V_{\text{node}} - V_0) * (N_a N_d) / (N_a + N_d)]^{1/2} \quad (5)$$

where  $\epsilon$  is the permittivity of the material,  $V_{\text{node}}$  is the voltage of the injection node,  $N_a$  is the acceptor concentration,  $N_d$  is the donor concentration, and  $V_0$  is the contact potential

Substituting equation 3 into equation 2 gives:

$$I(t) = Q\mu N [(2Q/\epsilon) * (V_{\text{node}} - V_0) * (N_a N_d) / (N_a + N_d)]^{1/2} [e^{-\alpha t} - e^{-\beta t}] \quad (6)$$

We can now use equation 9 from reference [1] and arrive a final expression for  $I(t)$  for Silicon material .

$$I_{\text{critical}}(t) = 103 \times 10^{-8} * LET * T * I(t) \quad (7)$$

Where  $T$  is the IC device thickness in micrometers and  $I_{critical}$  is the minimum current produced by the SET event. For the purpose of SPICE modeling many of the terms in equation 7 can be combined into a single constant “C” to obtain equation 8.

$$I_{critical}(t) = C [e^{-\alpha t} - e^{-\beta t}] *(V_{node} - V_o)^{1/2} \quad (8)$$

In equation 8 the injection current is a current source which can be modeled in SPICE as a dependent current source and inserted in the drain of the inverter as shown in Figure 6.

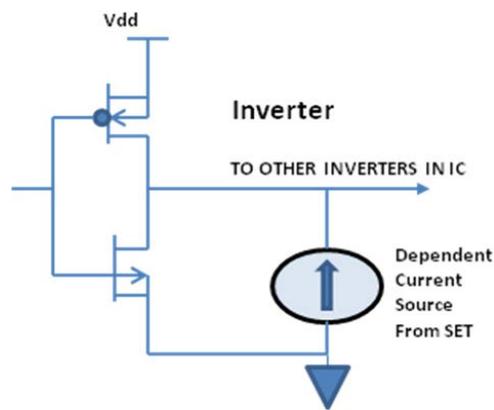


Fig 6.SPICE Modeling of SET in an inverter

Transient “glitches” can now be rigorously modeled at the inverter IC level starting with equation 8 and address its effects at the IC. This approach is illustrated in Figure 7 where the IC D1 (an AND gate) is shown to have experienced a “glitch” from logic 0 to logic 1. Figure 7 illustrates an asynchronous circuit and the glitch will ripple through downstream logic causing even more errors. Even, in clock circuits (synchronous logic) a SET can cause momentary glitches which are often recoverable in the next clock cycle but such errors can temporarily interrupt critical function in a space vehicle which can trigger internal alarms and cause emergency “safing” procedures to be executed. For example, work by this author has shown (non-publishable) that a few such events in critical circuits of resonance power supplies have caused the fault management software in two spacecraft to execute power-on resets in addition to other measures which have put the spacecraft in “safe modes” Once the

culprit circuits were identified correction in the fault management software were implemented to account for the glitch effects so as to “screen them out”.

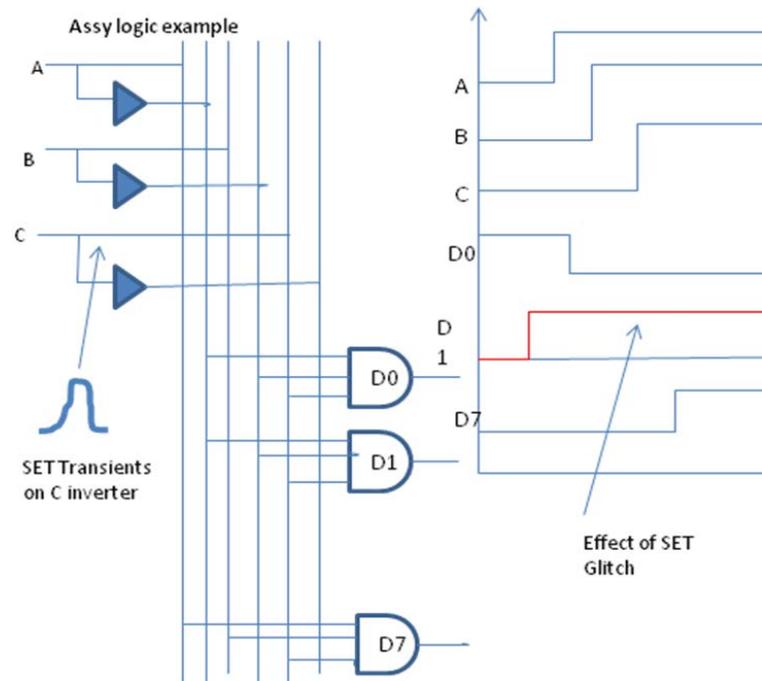


Fig 7. Illustration on how an SET event glitch can propagate in asynchronous circuits.

The same approach used for analog circuits can now also be used here for digital circuits, meaning that we can model the effects at the circuit level and then see the effects of such transient responses at the card and subsystem levels, as shown in the block diagram of Figure 8.

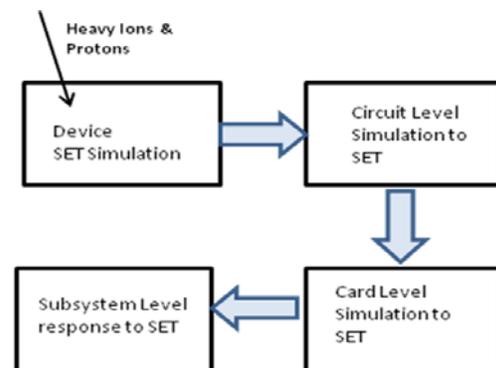


Fig 8.. SET effects can be propagated up to address subsystem level effects.

### III MODELING SUBSYSTEM and SYSTEM LEVEL EFFECTS from SET

The rigorous implementation of SET propagation effects as shown in Figure 8 is difficult to implement because it requires costly and time consuming SPICE-like simulations on multiple circuits with ever increasing complexities. Rather than providing a quantitative estimate of SET propagation across electronics of interest, a qualitative approach is pursued. In the qualitative approach the interest is mainly on the behavioral modeling of the circuits and the behavioral performance of such circuits. The SET effects are described in terms of behavioral responses which are first postulated at the circuit level and then extrapolated to higher level of complexities, such as the circuit card and then subsystem levels.

There are two methods to address subsystem and system levels effects from SET events in a behavioral approach. The first approach is the *Tabular model*. The Tabular model is quite good, and it has advantages with very little disadvantages. The main advantage of the Tabular model is that it emphasizes the outcome, including potential failures, without the need for transitional stages. The Tabular model is the most common approach used in the industry when performing SET analyses. The second approach is developed by this author; and it is identified as the *SET State Transition Model*. This author believes that the State Transition Model is much more revealing from the engineering point of view and more rigorous. The State Transition Model shows the states and the transitional probabilities to go from a fault-free state of the system to the actual failure state in multiple transitions. Figure 9 shows an example of the State Transition Model. The State Transition model has the unique advantage that it can be mathematically, logically, and discretely represented via software models, and can be made into an intricate part of a fault management system.

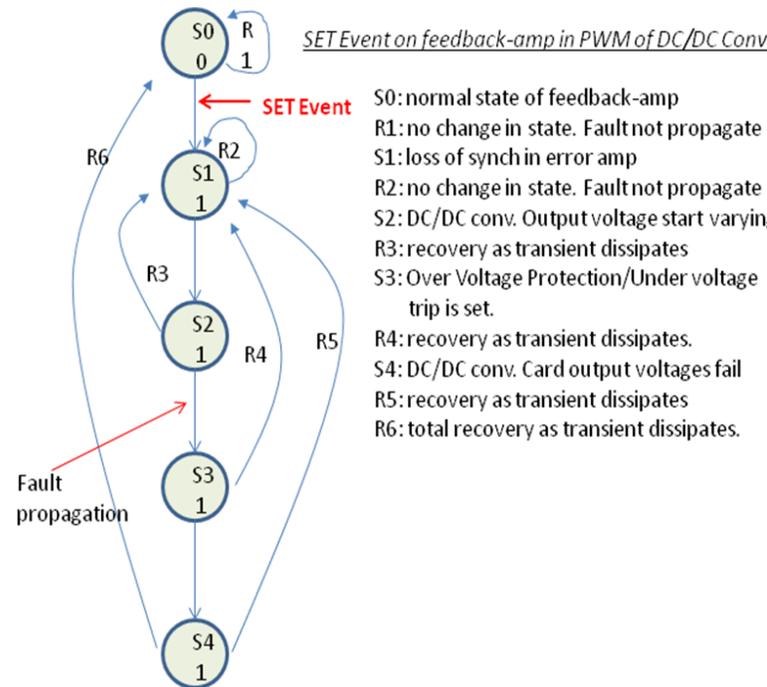


Fig 9. Example of using State Transition Model for modeling SET effects.

Figure 10 shows an example of modeling SET propagation effects via the tabular model.

### IV CONCLUSION

The goal of this work has been to expand on analytical modeling of SET in digital circuits that can be used in electronic simulators such as SPICE. An expression for a dependent current source in an inverter which models the injected current from a SET event has been derived. A second contribution in this paper is the development of a *SET State Transition Model* which this author believes provides greater insights into the propagation of SET events because the state transition model can actually be simulated and modeled in coded algorithms that can be used for fault protection purposes.

Ref. No	SH	Sec.	Qty	Part Number	Part Function	SET Perturbation Assessed	SET Circuit Assessment	SET Subsystem Assessment	SET System Assessment
U2B	1	D4	2	LM158A	Main Loop Error Amp	$\leq \pm 1V$ transient for 15 $\mu$ sec on output	Transients of this magnitude and duration due to the inherent delays of the system, will have little affect on the output voltage. No effect at NHA.	No effect since transient will be filtered out	No effect
						Transients of greater magnitudes than +1V transient for 15 $\mu$ sec on output	Direct testing and analysis shows that for pulses on the input pin of the UC1864J shorter than 17.5 $\mu$ sec, the 5V main output will not trip, but may transition above the required point of regulation.	Regulation holds but at a higher voltage	No effect that can be observed if small
						Transients of magnitudes greater than -1V including transients to ground output	Due to the high gain of the feedback system at this point, a small negative transient at this point may cause a dip in the output voltage, possibly beyond acceptable regulation limits. Always voltages will remain within about 0.5V below nominal.	small period for out of regulation	drop output voltage by no more than 0.5V may affect low voltage circuits temporarily

Fig 10. Example of Modeling SET propagation via a Tabular form

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