

# An SET-free, All-Digital Controlled Point-of-Load Regulator for Next-Generation Power Systems: ADC-POL

Philippe C. Adell, *IEEE member*, Tao Liu, Bert Vermeire, *IEEE member*, Bertan Bakkaloglu and David Aveline

**Abstract**—This paper presents a digitally controlled programmable point-of-load regulator for next-generation power systems. A novel digital control scheme was designed to minimize single-event effect (SEE)-induced transient effects. By effectively programming the loop transmission, the POL can trade off transient response time with SET robustness. The IC works with 5 V ( $\pm 20\%$ ) input voltage, 1–4.5V regulated output voltage, high efficiency (peak efficiency at 94%) and power of up to 5 W. The design was fabricated in the AMI i2t100 0.7  $\mu\text{m}$  complimentary, metal-oxide semiconductor (CMOS) process and characterized with the Jet Propulsion Laboratory (JPL) pulsed laser system.

## I. INTRODUCTION

Most low-to-medium level power distribution systems in spacecraft use two to three stages of regulation with point-of-load (POL) mounted regulators fed by isolated dc-dc converters. These systems cause multiple sources of power dissipation resulting in an end-to-end efficiency that can be as low as 30%, depending on the commercial parts selected. While they have limited capabilities, individual regulators work independently and without hierarchical load and device failure detection or adaptive built-in-self-test.

There is also a growing demand for high-speed, onboard digital integrated circuits (ICs) on spacecraft, including field-programmable gate arrays (FPGAs), digital signal processors (DSPs) and other application specific integrated circuits (ASICs) built with aggressively scaled technologies. As shown in Fig. 1, increasing reduction in effective device lengths have resulted in core voltage rails dropping to values close to 1 V as opposed to 2.5 V about ten years ago. This drastically reduces margin to standard switching converters or regulators that power digital (ICs).

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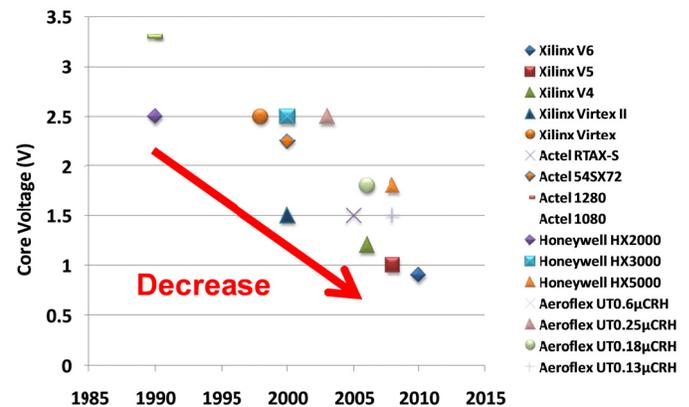


Fig 1. FPGAs and ASICs core voltage roadmap.

As a result, there is an increasing need for flexible POL regulators. Next-generation power distribution schemes will need new strategies to respond to sub-micron technologies and will require more design flexibility and better fault management. In addition, most space-use dc-dc converters or linear regulators are hybrid converters, and due to the lack of information regarding the process technology, it is often quite difficult to assess their radiation hardness. Their qualification cost is also often very high. Several NASA missions have had radiation-effect anomalies with hybrid switching converters, in particular, related to the single-event transient (SET) phenomenon. SET represents a major threat for power systems. Converter transient responses are dependent on load conditions as well as temperature [1-10]. Ion strikes on a sensitive area of a conventional pulse-width modulated switching converter or a linear regulator can result in an unacceptably large transient pulse of several volts of amplitude and several hundreds of  $\mu\text{s}$  at their output [1-10]. Recently, several stability issues tied to the ESR output capacitor for hybrid linear regulator have been reported as well.

To address these problems associated with state-of-the-art converters, digital control is becoming an emerging solution for next-generation power regulators. Along with the general advantages, such as high flexibility, reduced sensitivity to noise and

component parameter variations, and the capability to realize sophisticated control algorithms, digital systems can be hardened more easily against radiation-induced errors than its analog counterparts [11]. A digital power solution also offers observability, re-configurability, better fault management, and monitoring of system degradation. It has the advantage of having a convenient design flow with automated layout in standard process design kits (PDKs), resulting in the possibility of developing cost-effective, single-chip solutions as a reliable alternative to hybrid converters or linear regulators.

The proposed work presents the first digitally controlled, programmable POL regulator, suitable for next-generation, distributed flight power systems as an alternative to hybrid dc-dc or linear converters. A novel digital control scheme that helps minimization of SEE-induced transient effects, unlike analog converters, is proposed. The POL regulator has been designed, fabricated, and tested, and its characteristics are defined by a 5 Volt ( $\pm 20\%$ ) input voltage, 1–4.5 regulated output voltage, high efficiency (peak efficiency at 94%) and power of up to 5 W. The design was fabricated in the AMI i2t100 0.7  $\mu\text{m}$  complimentary, metal-oxide semiconductor (CMOS) process. The SET hardness of this approach is experimentally validated using the picosecond pulses laser system at the Jet Propulsion Laboratory.

## II. POINT-OF-LOAD ARCHITECTURE AND DESIGN

### 1. Design of the Scalable DC-DC Converter Module

Fig. 2 shows the schematic representation of the converter module with direct main power connectivity and adaptive digital control. The converter is configured in voltage control mode, where a proportional integral derivative (PID) compensator computes the required pulse duty cycle based on the difference of the digitized DC-DC feedback voltage  $V_{FB}$  and reference voltage  $V_{REF}$ . A 9-bit delay-locked loop (DLL)-based, digital pulse-width modulator (DPWM) generates the desired duty cycle. The digitization is carried out by digitally intensive frequency domain  $\Delta\Sigma$  analog-to-digital converters (ADCs). The ADC is composed of a voltage-controlled oscillator (VCO) followed by a first-order  $\Delta\Sigma$  frequency discriminator ( $\Delta\Sigma\text{FD}$ ) and a cascaded integrator comb (CIC) decimator [12]. The digital feedback loop is designed with a cross-over frequency of 50 kHz and a switching frequency of 500 kHz.

The digital control system operation is as follows: After voltage-to-frequency conversion using ring-oscillator-based VCOs, single-bit sigma-delta ( $\Sigma\Delta$ ) modulated feedback signals are compared to the  $\Sigma\Delta$  modulated

analog voltage reference. The 3-level, first-order  $\Sigma\Delta$  noise shaped error signal is then decimated using 2-stage comb (CIC) filter and applied to the compensator (PID) input as a 9-bit digital code. The 9-bit PID compensator computes the required duty cycle. Finally, the DPWM converts this voltage command into a duty cycle to drive the PFET and NFET via a built-in, non-overlap, dead-time gate driver. The implementation of the converter architecture is based on the following modules:

- **Digitally controlled DC-DC converter:** A digital PWM DC-DC buck converter utilizing a first order  $\Sigma\Delta$  based frequency discriminator ( $\Sigma\Delta\text{FD}$ ) is the core converter for this IC. A frequency discriminator generates an accurate representation of an instantaneous frequency of a carrier signal.
- **Digital PWM generators:** A coarse and fine scheme is used to generate the high-accuracy PWM duty cycle. The coarse scheme uses a counter-based approach, while the fine control is through a high-accuracy, phase-locked, digitally controlled ring oscillator, i.e., DLL. This DLL controls the 4 fine bits of DPWM codes.

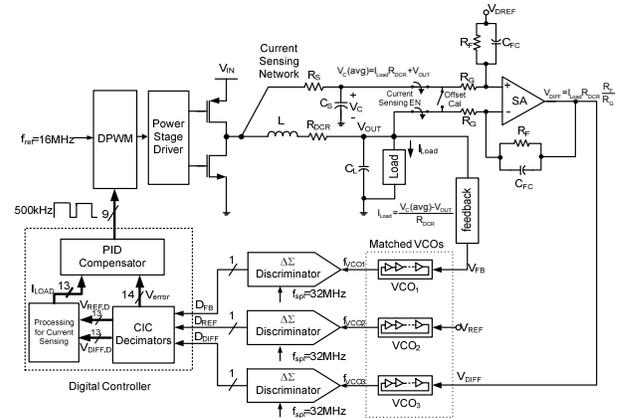


Fig. 2. Proposed DC-DC buck converter architecture with lossless load current sensing circuitry.

Fig. 3 shows the overview of the implementation. This approach avoids missing codes and ensures monotonicity.

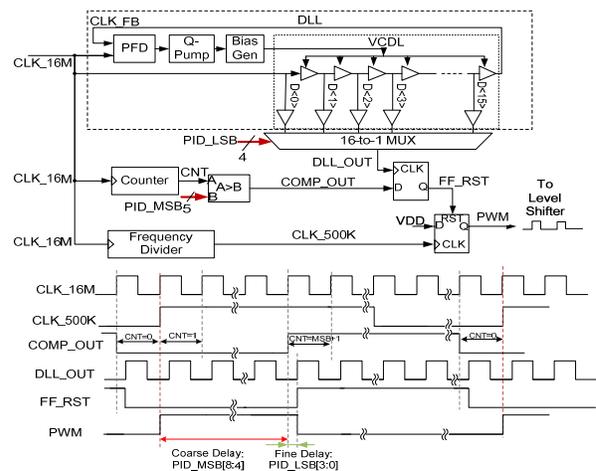


Fig. 3. Schematic representation of the digital pulse-width modulator

(DPWM) approach to reduce single-event-transient effects.

### III. EXPERIMENTAL RESULTS

#### 1. Device Performance and Programmability

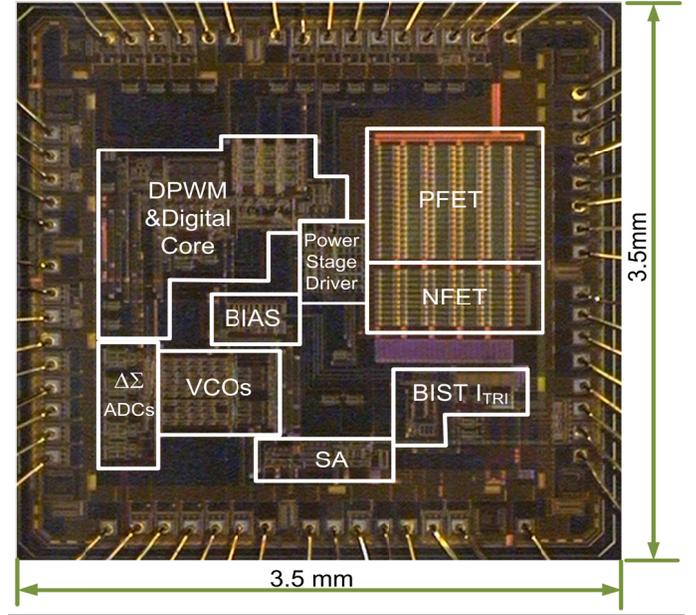
Table 1 summarizes the converter performance. The electrical parameters fit next-generation, POL application requirements (i.e., low output voltage, less than 1% accuracy and peak efficiency at 94%). Fig. 4 shows the die micrograph. The chip area is about  $3.5 \times 3.5 \text{ mm}^2$ . The design can be used as a single-chip solution, providing flexibility for adjusting to load conditions by adaptively updating the PID controller coefficients (equivalent of the analog compensator), minimizing transient effects. The programmable PID also provides a user-friendly flow for loop gain and phase frequency response optimization.

Digital load current sensing feature described in Fig. 2 provides information about the load current. Digital load sensing implementation details are provided in [12]. This feature can be used to select pre-stored PID coefficient sets and update the compensator, thereby minimizing the closed-loop response variation due to the load current deviations. Fig. 4 shows an example of how the programmability can be achieved. If the PID update function is disabled, PID1 can work properly at low load currents. However, at high load currents, it will show over-damped transient response and the settling time is increased from  $85 \mu\text{s}$  to near  $500 \mu\text{s}$ . PID 2 shows underdamped transient response when load current is small. Based on the sensed load current, PID first-set coefficients are selected for low  $I_{\text{LOAD}}$  and PID second-set coefficients are selected for high  $I_{\text{LOAD}}$  to maintain a suitable transient response for large load current range. This type of approach can be used when a single-event ion hits and generates transients at the converter output. The idea is to program coefficients that will permit minimization of the transients, while being hit by a single ion. Fig. 6 shows a typical efficiency plot to demonstrate the functionality of the design with a peak efficiency of 94% at half load. It should be noted that the process used is not an optimized process, indicating that there is still room for improvement.

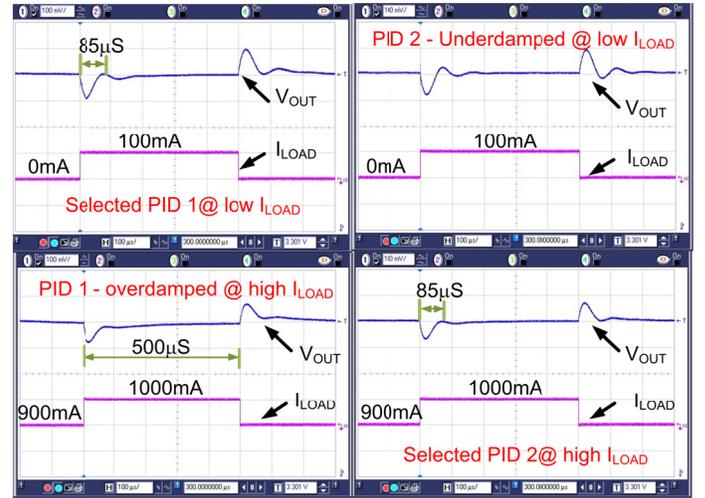
**Table 1.** Summary of POL performances.

Technology	AMI i2t100 0.7 $\mu\text{m}$ CMOS
$V_{\text{IN}}$	1 V–5.5 V (5 V typical)
$V_{\text{OUT}}$	1 V–5.5 V
Max load current( $I_{\text{LOAD}}$ )	1 A
Output voltage ripple	$\leq 10 \text{ mV}$
Switching frequency	500 kHz
Cross-over frequency	50 kHz
Off-chip $C_{\text{L}}$	22 $\mu\text{F}$
ESR (R in series with $C_{\text{L}}$ )	70 $\text{m}\Omega$
Efficiency	
$I_{\text{LOAD}}$ [0.1A – 1A] @ $V_{\text{IN}}=5\text{V}$ ,	$89.7\% \leq \eta \leq 94.5\%$

$V_{\text{OUT}}=4\text{V}$	
$I_{\text{LOAD}}$ [0.1A – 1A] @ $V_{\text{IN}}=5\text{V}$ , $V_{\text{OUT}}=3.3\text{V}$	$81.7\% \leq \eta \leq 91.8\%$
Chip Area	
Die	$3.5 \text{ mm} \times 3.5 \text{ mm}$
Inductor BIST & Current Sensing	5.2% of die area



**Fig. 4.** Die micrograph.



Left: PID 1 designed for low  $I_{\text{LOAD}}$

Right: PID 2 designed for high  $I_{\text{LOAD}}$

**Fig. 5.** PID update based on sensed load current illustration. *Left:* the pre-stored PIDs first set of coefficients, designed for low load current  $I_{\text{LOAD}}$ . *Right:* the pre-stored PID second set of coefficients designed for high  $I_{\text{LOAD}}$ .

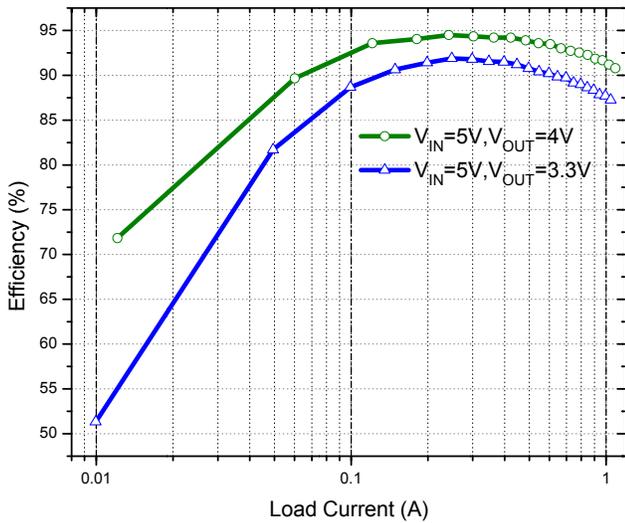


Fig. 6. Measured DC-DC buck converter efficiency for different  $V_{OUT}$

## 2. SET Response of the DCDC Converter Building Blocks

Unlike typical pulse-width modulator circuits used in hybrid DC-DC switching converters to generate the duty cycle, or compensated error amplifiers used in linear regulators, the DPWM approach selected here minimizes single-transient effects due to its digital intensive implementation. Ion strikes in the sensitive portion of a typical analog dc-dc converter (i.e., ramp generator or comparator) causes missing pulses within the PWM duty cycle signal [1-10], resulting in long transient pulses at the converter output. A similar problem exists for linear regulators, SET strikes causing settling errors at the error amplifier's high output impedance. These long pulses are application-dependent and vary with input bias and load conditions [1-10]. It has been shown as well that SETs in linear regulators are really dependent on the ESR values of their output capacitor and characterizing a part with the same capacitor with different values of ESR can introduce some instability in the transient response.

The proposed coarse-fine DPWM scheme, described in Fig. 3, ensures that when a SET occurs, only a small portion of the duty-cycle pulse signal can be affected, resulting in a very small transient at the converter output. The transient is also load independent. In other words, a hit on a sensitive transistor of the DLL or on the coarse scheme counter-based circuit will not create more than a small portion of the duty cycle signal to be missing; and will recover at the next cycle. The closed-loop nature of the DLL ensures that changes in the locking behavior are quickly corrected by the loop. The only potential problem would be if the DLL permanently moves out of lock; in this case, only the coarse portion of the duty cycle, which is a simple counter, would keep the regulation going. The PID part of the circuit can be hardened by typical digital

redundancy techniques using synthesized verilog code as shown in [11]. To validate the approach and characterize its hardened properties, we used the JPL pico-second pulsed laser system to irradiate the POL and evaluate its worst-case transient response. The laser system is a mode-locked Ti:sapphire cavity pumped by a 5 W diode-pumped solid-state laser at 532 nm. A laser beam with a 2 ps pulse width was tightly focused through a microscope objective onto the device under test (DUT) as shown in Fig. 7. During the test, the Ti:sapphire's output beam had a wavelength range of 800 nm, with typical power between 400 and 600 mW making it possible to simulate heavy ion effects with relative high linear-energy-transfer (LET) values. The system also incorporates a motorized three-axis stage to move the DUT and scan the area with resolution better than 100 nm; allowing for mapping of the sensitive region of the circuit.

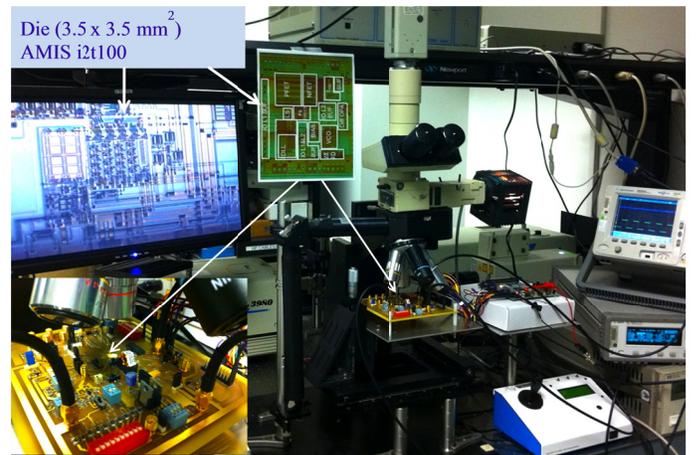
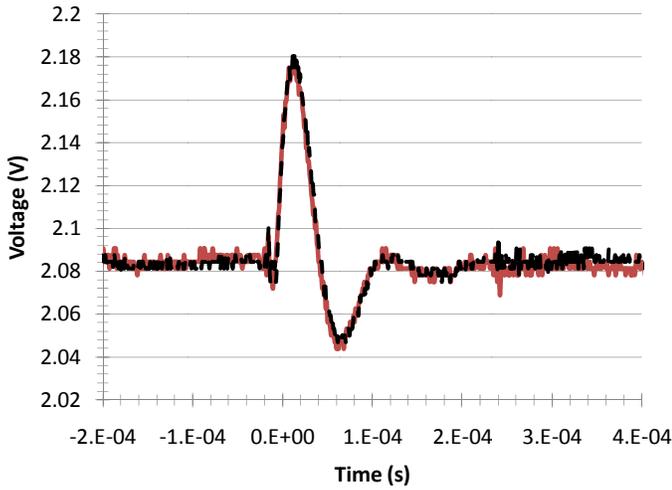


Fig. 7. JPL laser experimental setup. The POL was tested using a 20 pJ laser pulse. The main sensitive region of the device was the DLL.

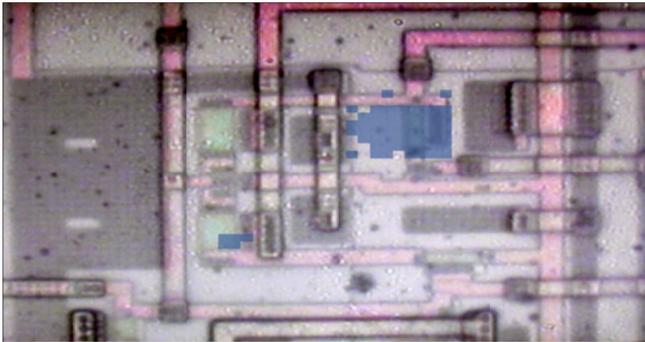
### - DLL portion of the DPWM circuit

To show the robustness of the design, Fig. 8 shows a typical transient resulting from a laser hit on the DLL block at a pulsed energy of approximately 30 pJ ( $\sim 100$  MeV.cm<sup>2</sup>/mg). As indicated in the figure, the worst-case transient ripple is measured to be around 100 mV, well within the regulator window (see Table 1). The other blocks of the DPWM circuit did not show any laser sensitivity.



**Fig. 8.** Typical worst-case transient measured at the ASU-JPL POL converter output. Transient is well within the load step change transient response. Two laser energy were considered 30 pJ (dashed line) and 10 pJ (line)

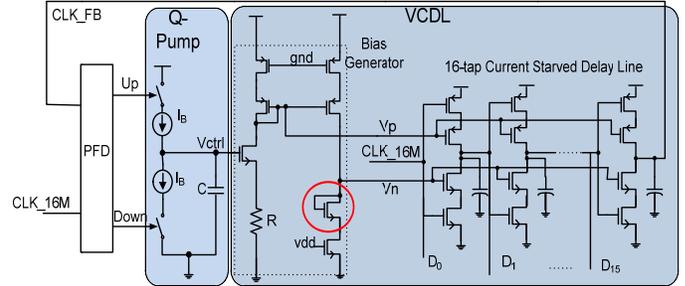
Using the JPL laser-scanning tool, we were able to locate and map the sensitive portion of the DLL circuit as shown on Fig. 9. On the picture, every pixel corresponds to a transient induced by a laser pulse with identical energy; 30 pJ in this particular case. The sensitive area ( $\sim 10 \times 10 \mu\text{m}^2$ ) is relatively small compared to the full chip area ( $3.5 \times 3.5 \text{ mm}^2$ ).



**Fig. 9.** SET sensitive region of the DLL portion of the circuit. The threshold energy is about 10 pJ ( $\sim 30 \text{ MeV.cm}^2/\text{mg}$ ). The sensitive region is located within the bias generator circuit between the current mode charge pump circuit and the delay line.

Fig. 10 shows a circuit representation of the DLL circuit ( $\sim$  fine part of the DPWM). One transistor within the bias generator circuit that separates the current charge pump and the delay lines has been identified as the sensitive transistor. The transistor is part of the circuit that set the voltage ( $V_n$ ) prior to the current starved delay lines. During normal operation,  $V_n$  is set by the  $V_{\text{ctrl}}$  from the current charge pump circuit through the voltage to current bias circuit shown in Fig. 10. If any perturbation occurs, the delay line will be affected and the PFD feedback circuit will help the delay line signal to re-adjust itself to the reference clock (CLK\_16 M). When the signals are in phase, the

$V_{\text{ctrl}}$  and  $V_n$  will reach their initial values. The time it takes for these voltages to return to their initial values is dependent on the capacitor of the current charge pump circuit. The transients observed experimentally are the results of a perturbation of the voltages  $V_{\text{ctrl}}$  and  $V_n$  and the time it takes for the DLL signal to be in phase with the 16 MHz clock.



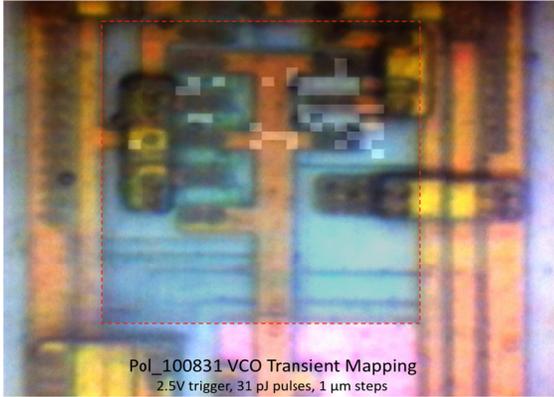
**Fig. 10.** DPWM fine portion of the circuit that uses a delay locked loop (DLL) circuit. One transistor in the bias generator circuit has been identified as the sensitive transistor. The DLL never goes out of lock after being hit by a laser pulse.

To completely harden the circuit against SETs, a triple modular redundant (TMR) DLL extension of the current design can also be implemented. However, because of the coarse-fine segmented implementation of the DPWM circuit, even if the DLL would go out of lock after a laser strike, the coarse count will still remain active, keeping the regulation steady until DLL locks again. Another alternative is to modify the DLL design and use a fully digital DLL implementation without the use of a current charge pump circuit.

In conclusion, only transients of small amplitude and duration have been recorded at the regulator output when hitting the DPWM circuit. The energy threshold was relatively high with a value of about 10 pJ ( $\sim 25 \text{ MeV.cm}^2/\text{mg}$ ). The identified sensitive area is small compared to the total chip area, indicating that these SETs would have a very low probability of occurrence if the converter operates in a harsh environment.

#### - ADC Voltage Controlled Oscillators

As shown in Fig. 11, a small area of the frequency domain ADC-VCOs was also identified as a sensitive region.

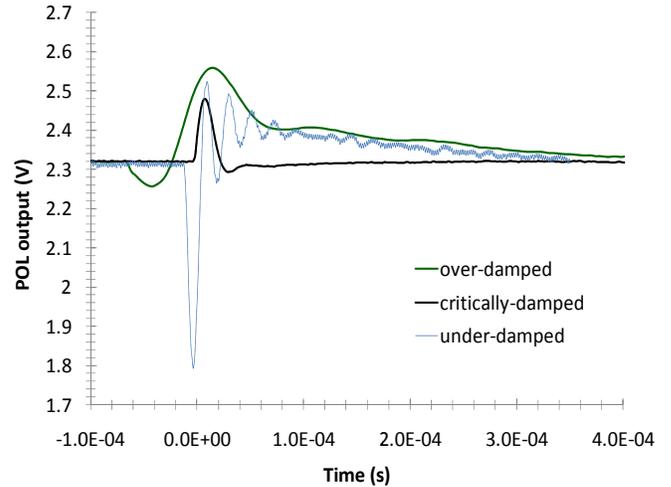


**Fig 11.** SET sensitive region of a single inverter within the ADC-VCOs. The threshold energy was 12 pJ.

The sensitivity characteristics are very similar to the ones observed in the DPWM circuit. The energy threshold is about 12-15 pJ. Laser energy did not affect the transient amplitude and duration; only a minimum energy was needed to create a transient. These results are interesting since they differ from a typical behavior observed in linear regulators where the transient characteristics are a strong function of ion energy [1-10]. The SET sensitive area is quite small as well. A transient hit in the n-MOS transistors within the inverter chains of the ADC-VCOs can cause small transients at the POL output as illustrated in Fig. 12. Because the ADC circuit is located prior to the PID compensation circuit, several case scenarios were considered in order to study the influence of different frequency responses (i.e. PID configurations) on the transient response. The goal was to find out if it would be possible to minimize transients by modifying the frequency response through the optimization of PID compensation coefficients. To illustrate the benefit of our digital approach, three cases have been looked at: over-damped, under-damped and critically damped (desired). The results of laser irradiation are shown in Fig. 11. In the case of the over-damped configuration, transients have a magnitude of few hundred mV and duration of several hundred  $\mu$ s. The under-damped case shows a transient with a peak amplitude of 500 mV and duration of few hundred  $\mu$ s. Because of the nature of the frequency response, several oscillations were recorded. The critically-damped case shows reduced and well behaved transients; with a peak amplitude of 150 mV and less than 50  $\mu$ s in duration, well within the regulation window.

These results prove that the field programmability of the PID coefficients can reduce the impact of transient effects. They illustrate how to optimize the POL SET response for a specific set of parameters; i.e. load conditions, output voltage and frequency response. With the right PID configuration, it indicates that it is possible to minimize or possibly eliminate transients at

the output of the converter. Results also indicate how the converter sensitivity is influenced by loop gain parameters.



**Fig. 12.** Single event transients resulting from laser strikes on the sensitive portion of the ADC-VCOs. Three cases are considered: under-damped, over-damped and critically damped. The laser energy was 30 pJ and transient did not show any energy dependence as well. The energy threshold was about 12 pJ corresponding to a relatively high LET threshold.

In conclusion, only small transients with relatively high-energy threshold have been recorded during the course of this evaluation. Only small sensitive areas of the chip have been identified, i.e. the bias generator circuit within the DLL circuitry and the ADC-VCOs. The other blocks of the design such as drivers,  $\Sigma\Delta$  decimator, coarse DPWM blocks have been screened and no transients were observed at the POL output. No single event functional interrupt (SEFI) or other modes of failure have been recorded; resulting in a very robust design compared to the state-of-the-art of hybrid dc-dc converters or linear regulators [1-10]. Finally, these data show the benefit of our digital approach by allowing for optimization of radiation response for a particular set of conditions.

#### IV. DISCUSSION

This work brings new insight into the development of next generation power system architecture. As illustrated in Fig. 13, power system architectures for space application are heading toward digital implementations with the attractive features of re-configurability, better fault management and monitoring of system degradation. Unlike common power systems where each regulator on a power distribution tree work independently and can't detect and report failure on the load of output components, digital implementation will allow for self-diagnostic capabilities, output filter and load conditions monitoring and re-configurability for extended lifetime operation.

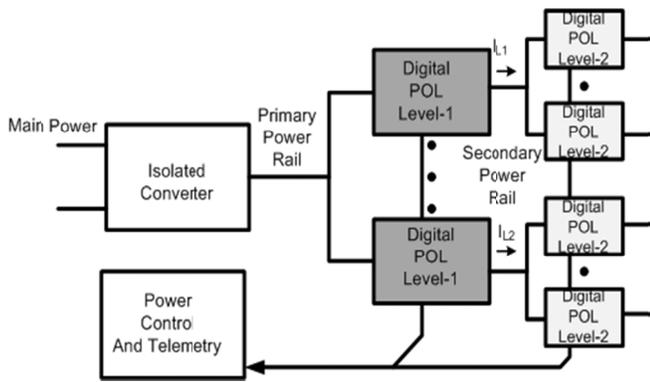


Fig. 13. Basic illustration of next generation digital power system architecture.

The design presented in this paper is a small portion of what is needed to build a full digital power system as described in Fig. 13; however, it is a first attempt at implementing a robust digital point of load regulator suitable for space application. It is designed to solve the standard radiation and reliability issues that are related to hybrid DC-DC converters and linear regulators [1-10] with the novelty of having re-configurability and self-test diagnostics capabilities. The approach has been successfully demonstrated in silicon and a single event transient evaluation indicated that the design is quite robust since most of the transients recorded are well within the regulation windows and have a very low probability to occur in a harsh environment. The SET sensitive regions have been identified and some mitigation schemes have already been proposed and are currently being implemented in the second-generation design. Finally, we also demonstrated the benefits of the digital approach by showing some illustrative example on how the POL transient response can be minimized by optimizing the frequency response using the PID function for a particular set of voltages and load conditions.

#### IV. CONCLUSION

This paper presents a digitally controlled programmable POL regulator for next-generation power systems. A maximum 5.5 V input, 1–4.5 output, maximum 1 A load current buck converter with lossless load current sensing capability was fabricated in a 0.7  $\mu\text{m}$  power CMOS process. A novel digital-control scheme was designed to minimize SEE-induced transient effects. The JPL pulsed laser system was used to experimentally validate the approach, showing transient response to SEE effects to be well within the regulation window. The approach was successful. Single event transients recorded during the laser evaluation appeared to be minimal and well within the regulation window. The sensitive regions have been identified and mapped; i.e. bias generator circuit within the DLL portion of the circuit and the ADCs VCO. Areas identified were very small compared to the full chip area

and the energy threshold relatively high ( $\sim 10$  pJ). These results indicate that the probability of occurrence of these events in a harsh environment would be very small. Finally, no permanent failure was observed.

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