Yearly Progress Update On the Class Y Initiative

(Infusion of new technology into the QML system)

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Agenda

- Current Status
- Effort at a Glance
- Road to QML-Y Flight Parts Procurement
- The Team

- Attachments:
  - Section Y: G-12 Task Group 10-01 Summary

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Current Status

DLA-VA's Engineering Practice (EP) Study on Class Y is closed.

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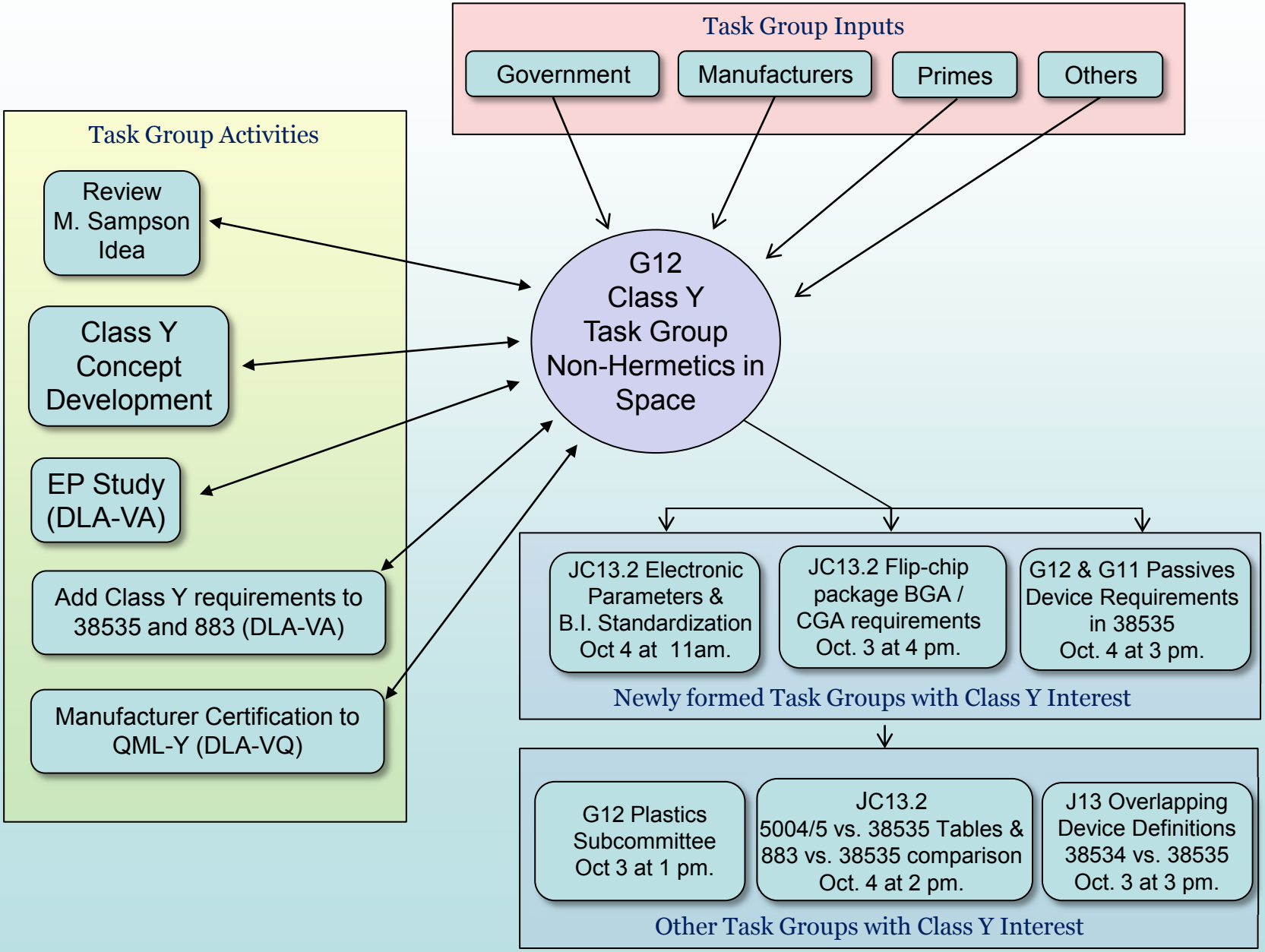
G12 Class Y Effort at a Glance



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Road to QML-Y Flight Parts Procurement

- Major Milestones:
  - ☑ G12 approval of TG charter
  - ☑ G-12 Class Y Task Group to develop requirements
  - ☑ G12 approval for DLA-VA to commence EP study
  - ☑ DLA-VA to conduct EP study
  - ☐ DLA-VA to make proposal
  - ☐ DLA-VA to add Class Y requirements to 38535 and 883
  - ☐ DLA-VQ to audit suppliers to Class Y requirements
  - – Users to procure QML-Y flight parts from certified suppliers

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The Team

The Team members are:

- Muhammad Akbar, DLA-VA
- Larry Harzstark, Aerospace
- David Sunderland, Boeing
- Shri Agarwal, NASA/JPL
- Roger Carlson, NASA/JPL

Team resources include:

- Mike Sampson, NASA/GSFC
- Mark Porter, G12
- Brent Rhoton, JC13
- Anduin Touw, G12
- Mike Adams, DLA-VQ
- Rob Heber, DLA-VA
- Tom Hess, DLA-VA
- Charles Saffle, DLA-VA

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Section Y

G-12 Task Group 10-01
(Class Y)
Summary

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Current Status

DLA-VA's Engineering Practice (EP) Study for Class Y
Is closed

Background

Back in 2009, there was a big push to bring the Xilinx Viirtex-4 (a non-hermetic part) into the QML system as Class V device. NASA and others were not in favor as it would have created a massive confusion. Mike Sampson conceived the idea of a new Class Y for non-hermetic space parts to provide QML coverage for Xilinx Virtex-4 and similar devices.

A new G-12 Task Group, TG 2010-01, was formed in early 2010 to address non-hermetic devices for space. Shri Agarwal was asked to lead the effort.

This task was challenging because it:

- Was far more involved than typical G12 tasks,
- Required development of a brand new concept,
- Used system-on-a-chip — one of the most complicated devices,
- Needed to be simple and easily understood,
- Possessed sketchy testing and board assembly boundaries, and
- Was needed to procure a standard QML product as quickly as possible.

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Why “Class Y”?

- This effort is an attempt to bring advancements in packaging technology into the QML system.
- Advancements in packaging technology, increasing functional density and increasing operating frequency have resulted in single die SoCs (System-on-a-Chip) with non-hermetic flip-chip construction, in high-pin-count ceramic column grid array packages
  - “Poster Child” example: Virtex-4 (V-4) FPGAs from Xilinx
  - Such products were evaluated for radiation and reliability and have drawn the attention of the space user community
- Question: How do we bring V-4 and similar microcircuits into the QML system as space products?
  - It can’t be Class V because those are hermetic devices
  - Our intent is to put V-4 like products for space users in a new category: “Class Y”.
  - In early 2010, G-12 opened a Task Group to develop Class Y
- What if we dropped the Class Y effort?
  - It would be a big loss for the space community and the QML program at large because the industry would be limited to ordering via Source Control Drawings (SCDs), which is counterproductive to Mission Assurance, prevents standardization, and is expensive.

G12 Class Y Task Group Summary

- G-12 Task Group formed in Jan.'10 to develop screening/qualification requirements for non-hermetics for Space (TG2010-01).
- The TG's work so far may be summarized as follows:
  - Each of the meetings was well attended
  - As soon as the TG was formed, users were enthusiastic and eager to know when they could procure QML-Y flight parts? *See slide 5 on road to procurement.*
  - A questionnaire was sent to a targeted group of users, manufacturers and others (There are about 150 names on the Class Y distribution list). The major inputs were:
    - Class Y should cover those items that are ceramic flip-chip non-hermetic construction that have passed the requirements of Appendix B. The broader issue of organic based substrates would be addressed in the next phase of this work.
    - Some respondents asked why should space community even allow use of non-hermetic parts. (Although the feasibility of a hermetic ceramic package with under-fill flip-chip die has been demonstrated, there are sealing process, board level, and other concerns. There are no current development programs as there is no user interest.)
    - Add the word "hermetic" to the definitions of QML-Q and QML-V classes in 38535.
    - NASA does not endorse attaching the description "near hermetic" to Class Y. (How do you quantify "near-hermetic": it could be 10% or 99% hermetic, or less than half, or…?). Both DLA-VA and DLA–VQ support NASA position.

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G12 Class Y Task Group Summary (Contd.)

- TG meetings summary (cont'd):
  - Boeing proposed "simplified approach" was adopted:
    - Add paragraph to existing 38535 Appendix B stating differences for class Y (most remains same as Class V). One key element is for the manufacturers to submit a Packaging Integration Demonstration Test Plan (PIDTP) to QA for approval. This plan must address issues unique to non-hermetic construction and materials, such as potential materials degradation, interconnect reliability, thermal management, resistance to processing stresses, thermo-mechanical stresses, shelf life, etc. The PIDTP plan shall be approved by QA after consultation with the space community.
    - Separate issues related to non-hermeticity from those related to solder terminations (see below).
    - Provide markups to other affected documents.
  - 10 manufacturers have so far expressed interest in offering Class Y products (Xilinx, Actel, Intersil, Aeroflex, BAE, Honeywell, TI, e2v, 3D Plus, Cypress).
  - Government customers and contractors have provided statements of support.
  - DLA Land and Maritime – VA (M. Akbar) was added to the team.
  - Comment from G12 management: The group may be surprised at how quickly this is moving. Most of the time, documents take over a year to get a full draft. You are far ahead of schedule. People just may not realize that this is out of the conceptual stage and into the writing stage.

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G12 Class Y Task Group Summary (Contd.)

- Solder terminated parts (could be hermetic or non-hermetic) need attention. Proposed a paragraph to add to MIL-PRF-38535, Appendix B. The JC-13.2 Task Group on solder terminations has been formed. The broad issues are: solderability, storage and shelf life, electrical testing, reworks, pull test, termination definition (Tin lead solder based?), etc. Some specific questions are:
  - What is the shelf life of the of the CGA? Specifically, how long will these parts be 100% solderable? Is this guaranteed?
  - As the columns would tend to oxidize when exposed to atmosphere, how do you store them: keep in sealed dry bags? Store in dry nitrogen?
  - Do all internal and external portions of the flip-chip package pass MIL-STD-883, Method 5011 (re. evaluation of polymeric materials)?
  - Once assembled, can the finished CGA (Like all other microcircuits, transistors, and hybrids) be functionally tested at -55C, 25C, and +125C? (If the solder melting point is estimated at about 180C, then it would be risky to electrically test the parts at 125C case temperature. Any cold brittle concerns at -55C?)
  - What board/assembly level test have been run for temp cycling/vibration, etc
  - What is the max number of allowable column reworks for space products?
  - Specify column pull test
  - Inspection of CGAs (area arrays, in general)
  - Need application notes on CGAs after column attach so that the users know what they are getting, any temperature limitations, adequacy of visual inspection, cleanliness, fluxes to avoid, etc.
  - Coordination with IPC – what are the boundaries that separate JEDEC work from IPC?

G12 Class Y Task Group Summary (Contd.)

- Clarification needed on burn-in, electricals and delta requirements. This is a big issue for all microcircuits and would apply to Class Y products as well. For instance, statements such as, the certain FPGA has undergone 4000 hours of life test with parts biased in a static condition, make you wonder why an FPGA which is basically a digital part was not subjected to a dynamic condition? There are other questions related to the activation energy, low temperature burn-in, etc. At the request of L. Harzstark and S. Agarwal, a JC13 Task Group was formed to clarify/update requirements in MIL-STD-883, Method 5004.
- The screening/qual requirements for signal conditioning capacitors should be clearly stated – ref. MIL-PRF-38535, Paras 3.15 and 3.15.1. What is the attached method of the BME capacitors used in many designs? During the G12 we heard couple of companies say they use epoxy or silver glass die attachment material to adhere the capacitor to the internal portion of the IC package. There are others who only use solder attachment. A JC13 Task Group has been formed to address these issues.
- What is a space flight part?
  - Land Grid Array, LGA, configuration (yes)
  - Column Grid Array, CGA, configuration (debatable)
- Will the set of 38535 classes, with Class Y added, cover microcircuits for the next several years? (yes, per the poll taken of major manufacturers)

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G12 Class Y Task Group Summary (Contd)

- The Team requested G12 approval for DLA Land and Maritime - VA to conduct an Engineering Practice (EP) study using the detailed requirement input the Task Group has developed. This request was approved by G12.
- The Team's request for clear approval of Task Group charter was also approved by G12. The charter statement reads:

  "This task group will develop requirements, including qualification and screening standards, for non-hermetic, ceramic-based microcircuits suitable for space applications. Initial effort will be focused on support for devices using flip-chip ceramic column grid array packaging, with resulting requirements to be submitted as a proposal for consideration to DLA Land and Maritime."
- So far 10 manufacturers have expressed interest in offering Class Y products (Xilinx, Actel, Intersil, Aeroflex, BAE, Honeywell, TI, e2v, 3D Plus, Cypress).

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