

BME Capacitor Risk Management

Douglas J. Sheldon
Jet Propulsion Laboratory
California Institute of Technology
Pasadena, California

*This work was performed at the Jet Propulsion Laboratory, California Institute of Technology,
Under contract with the National Aeronautics and Space Administration (NASA)*

Copyright 2012 California Institute of Technology. Government sponsorship acknowledged.

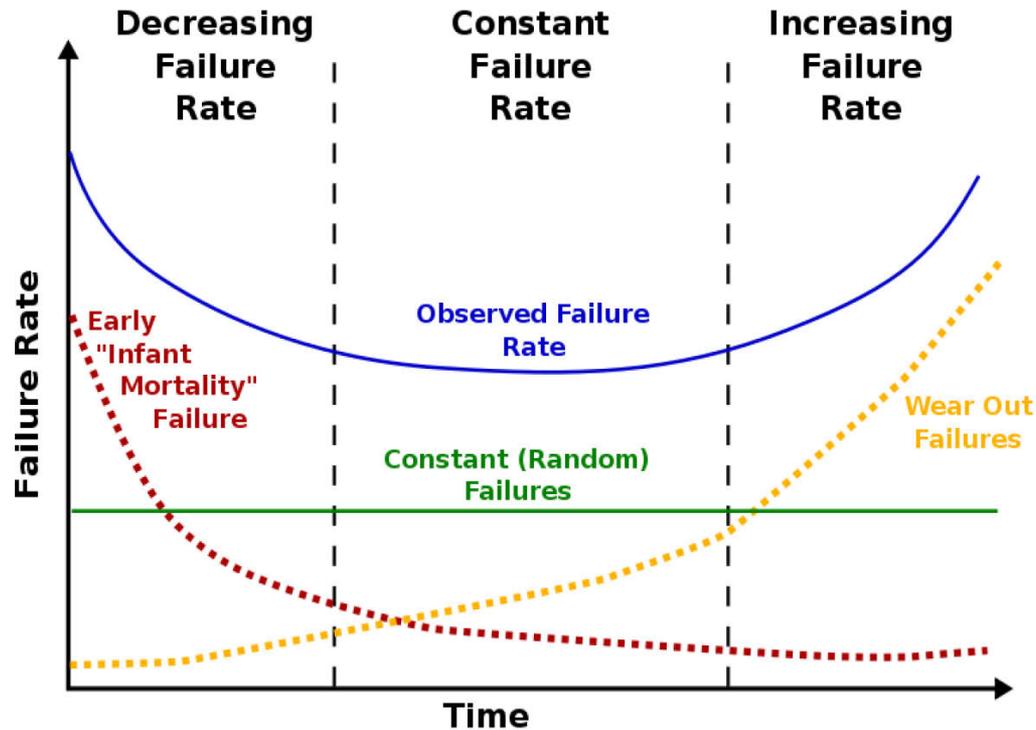


The Fundamental Reliability Graph



Section 514

Mission Assurance Office



- Managing risk always involves managing the entire reliability lifetime of a device:
 - *Early life: Screening*
 - *Useful life: Low levels of defects*
 - *End of life: Physics of Failure*



BMEs and FPGAs



Section 514

Mission Assurance Office



Our goal is to manage the risk of using Xilinx Virtex 4 and 5 FPGAs made with BME capacitors

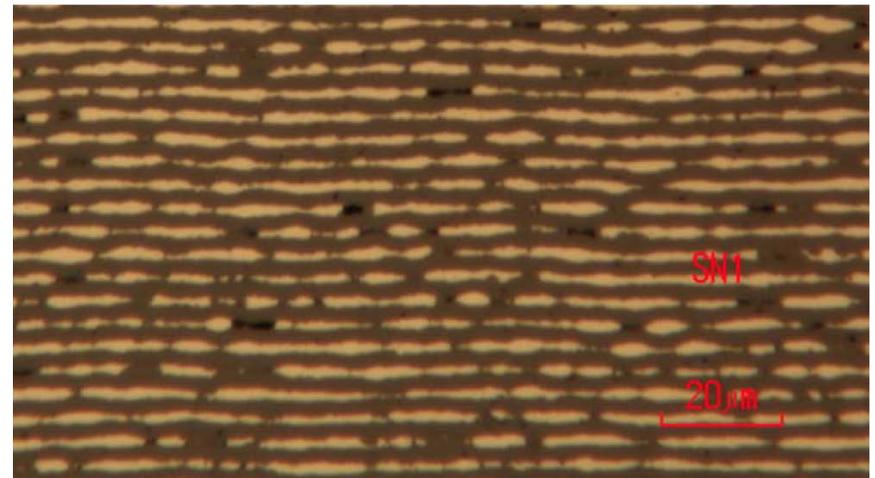
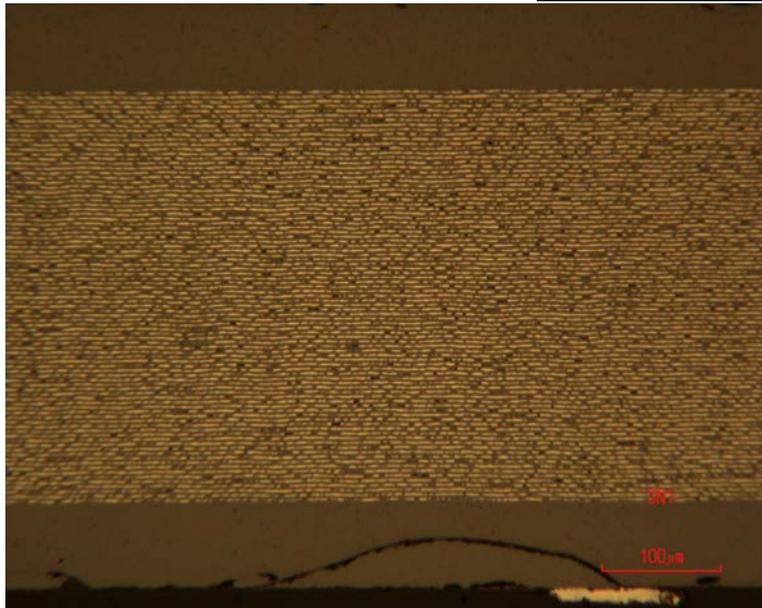
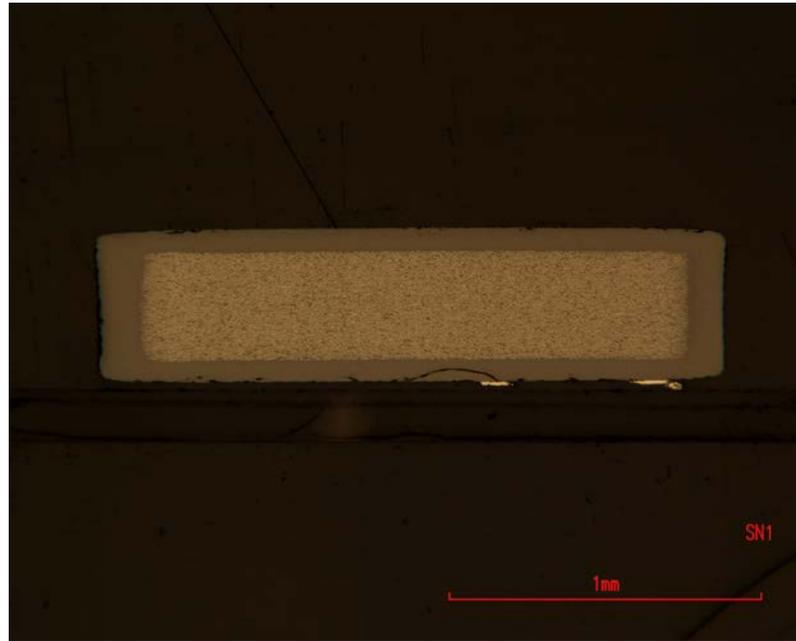


AVX BME Caps used on Xilinx FPGAs - Optical



Section 514

Mission Assurance Office



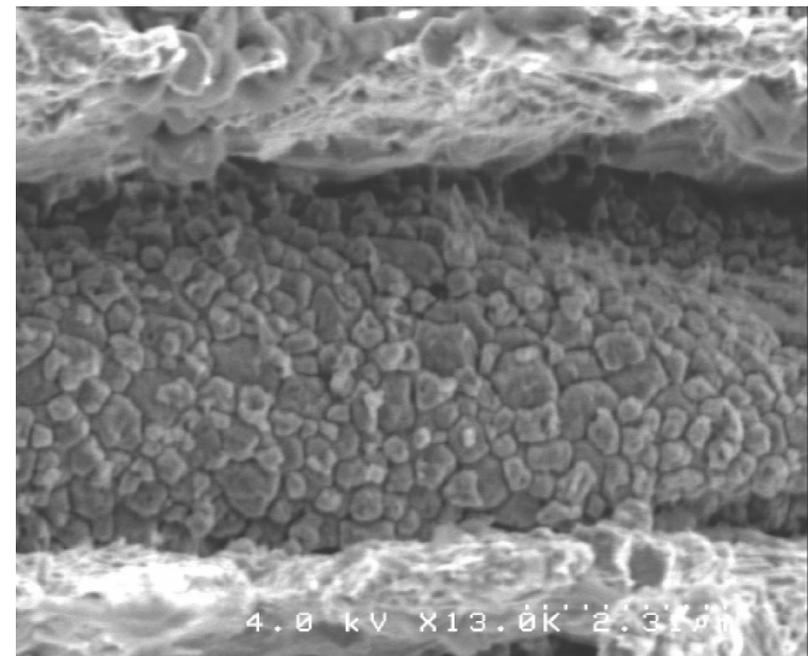
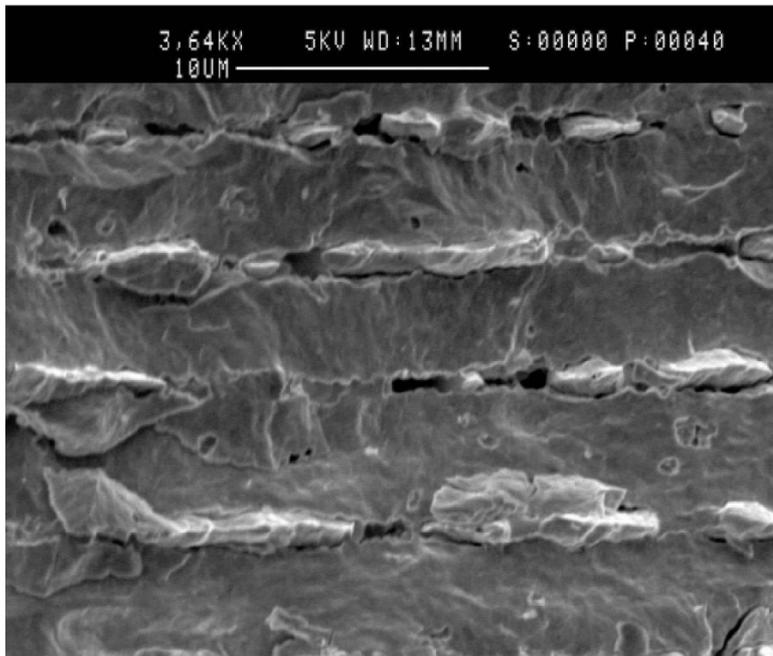
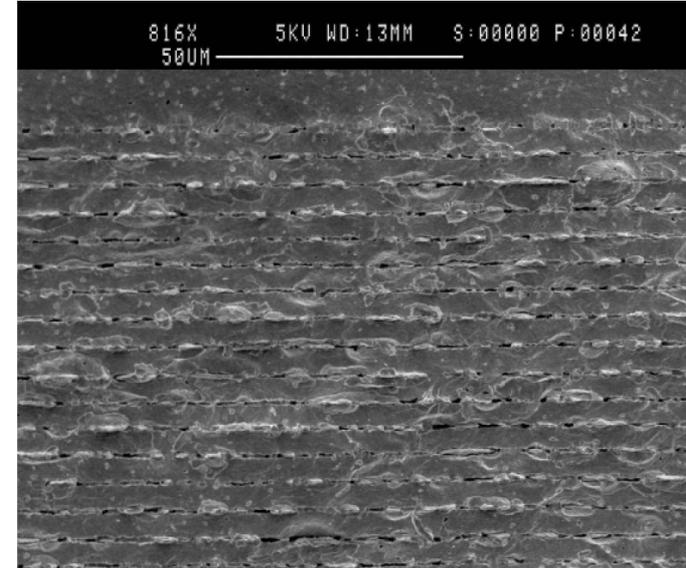
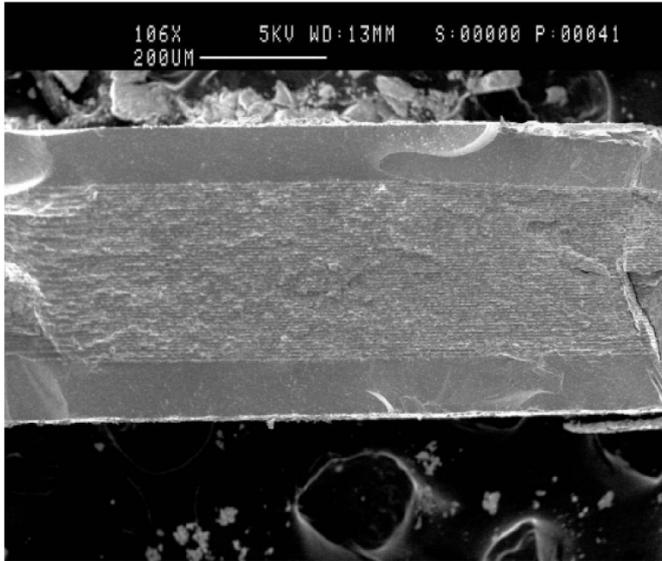


AVX BME Caps used on Xilinx FPGAs - SEM



Section 514

Mission Assurance Office





BME Background

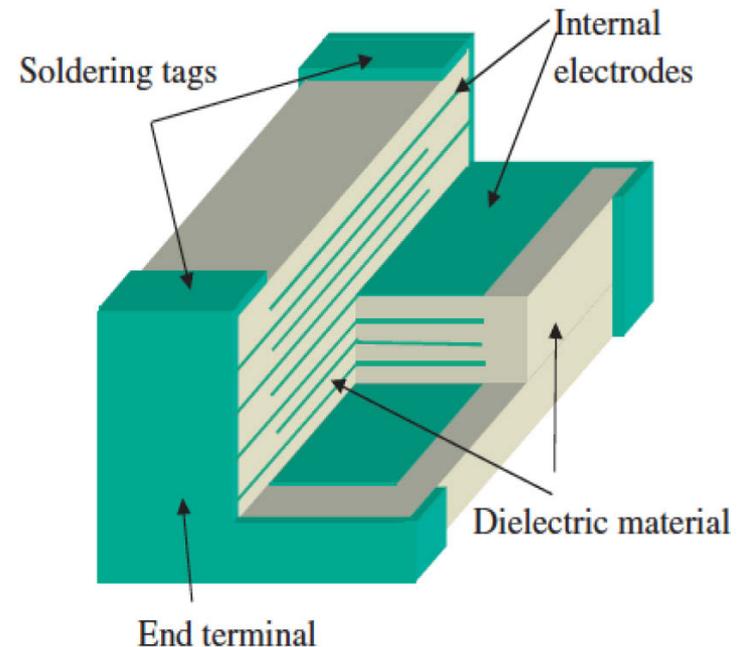


Section 514

Mission Assurance Office

- Multilayer ceramic capacitor (MLCC)
 - Alternating layers of dielectric and electrode
 - Used through out electronics industry
- Historically these type of capacitors used **PME = Precious Metal Electrodes** (usually palladium).
- Pd prices jumped from \$100/ounce to \$1500/ounce in 1990's.
 - Also demand for cheap electronics drove capacitor prices down.
- **BME = Base Metal Electrode** (usually nickel) developed as cost and performance solution

2 Jpn. J. Appl. Phys. Vol. 42 (2003) Pt. 1, No. 1





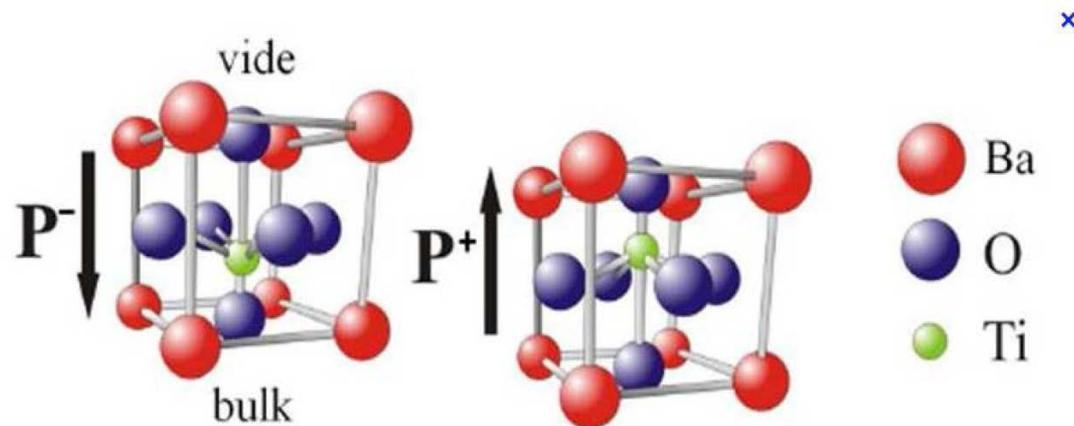
What about the dielectric?



Section 514

Mission Assurance Office

- MLCC dielectric of choice for both PME and BME is **BaTiO₃**
 - High melting point: 1625° C (good for stable manufacturing)
 - Ferroelectric: High dielectric constant ~3000 (helps volumetric efficiency)
 - Perovskite structure: allows for many dopants/stoichiometry to customize thermal, electrical, manufacturing and reliability performance





Relationship of Electrode to Dielectric



Section 514

Mission Assurance Office

- *Changing electrodes but keeping the dielectric the same requires a change to the manufacturing processing.*
- **PME** were sintered/fired in air atmosphere
 - Pd Electrodes will not oxidize
 - Produces favorable electrical properties
- **BME** must be sintered in reducing (i.e. vacuum, forming gas) atmosphere
 - Ni Electrodes will oxidize in air
 - Interface capacitance will dominate performance
 - Dielectric turns to semiconductor
- No free oxygen/reduction atmosphere => oxygen vacancies in dielectric film
 - Degrades internal resistance and long term reliability
- Additional dopants must be added and new re-oxidation process added to BME to address oxygen vacancies.

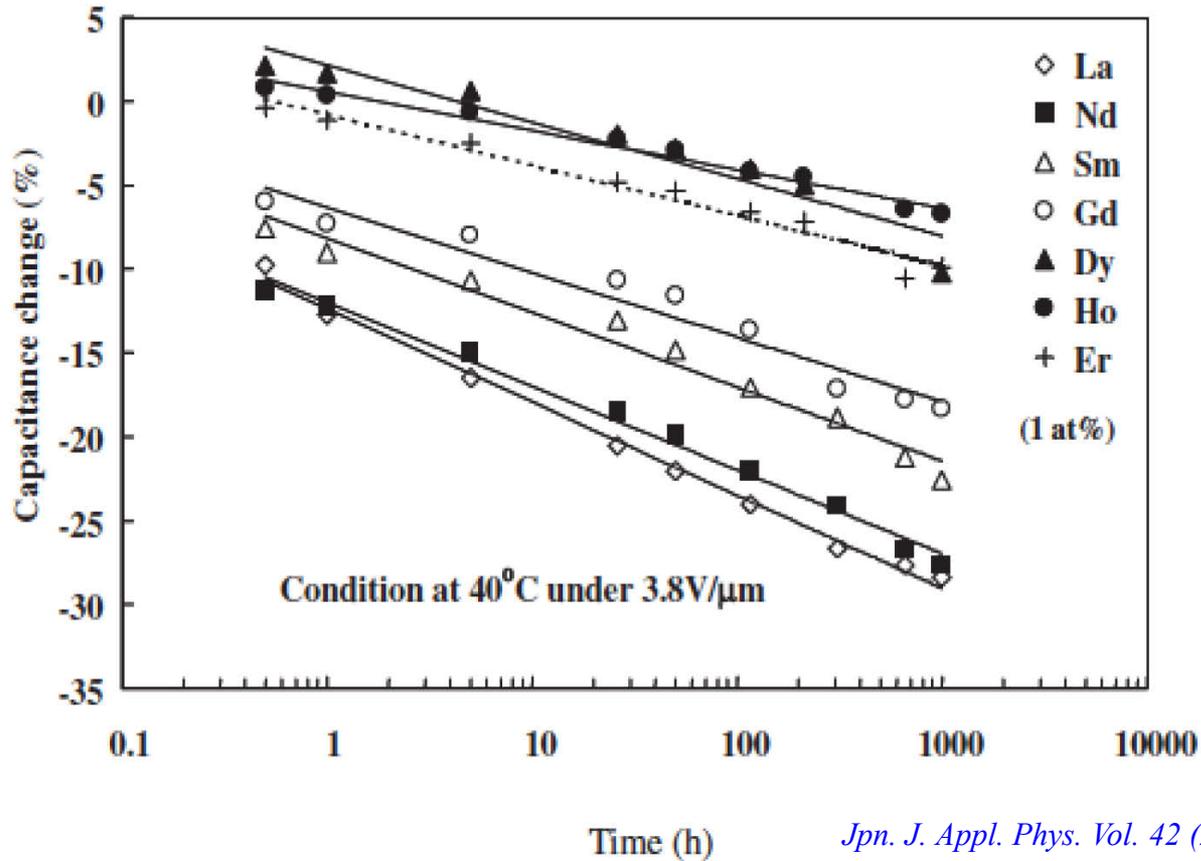


Examples of Oxygen Vacancies in BaTiO₃



Section 514

Mission Assurance Office



Jpn. J. Appl. Phys. Vol. 42 (2003) Pt. 1, No. 1

- Intermediate ionic radius rare-earth (Dy, Ho, Er) show smaller aging rates than large radius (La, Sm, Gd)
- DC bias drives oxygen vacancies to cathode/ceramic interface
 - Degrades insulation resistance

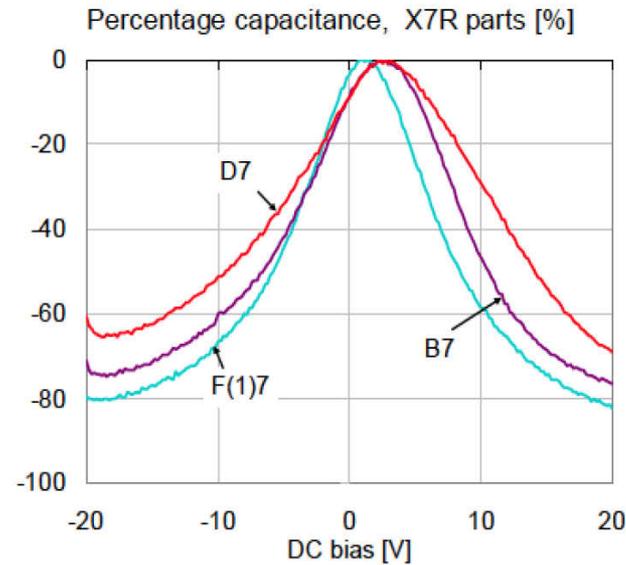
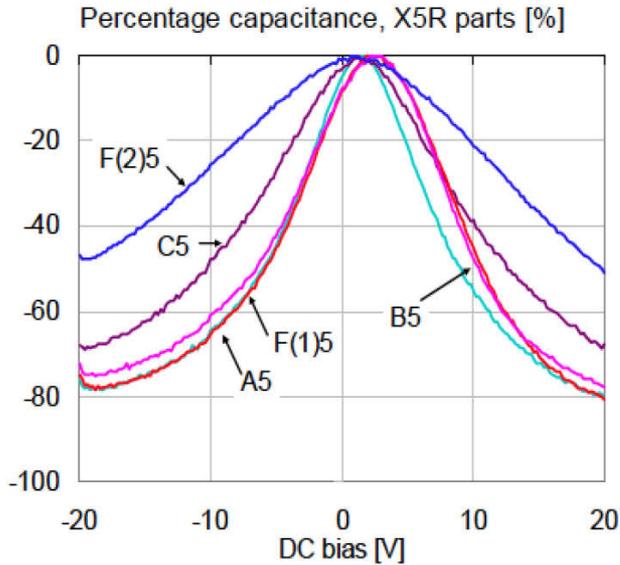


BME Performance Concerns

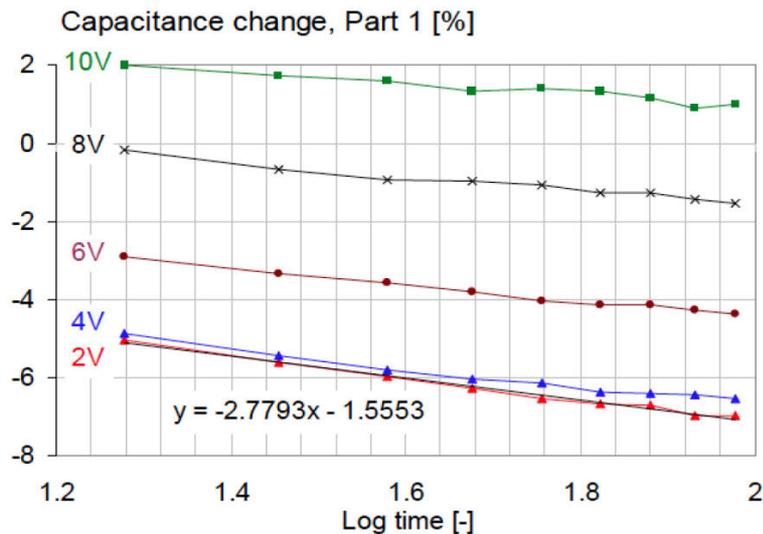


Section 514

Mission Assurance Office



Variation among vendors (same 16V/1uF capacitor)



*Logarithmic degradation over time.
 $C(t)/C(0) = 1 - k \cdot \log(t)$
15 year missions could have
20 decades of operation =>
final value is ~35% of t=0 value*

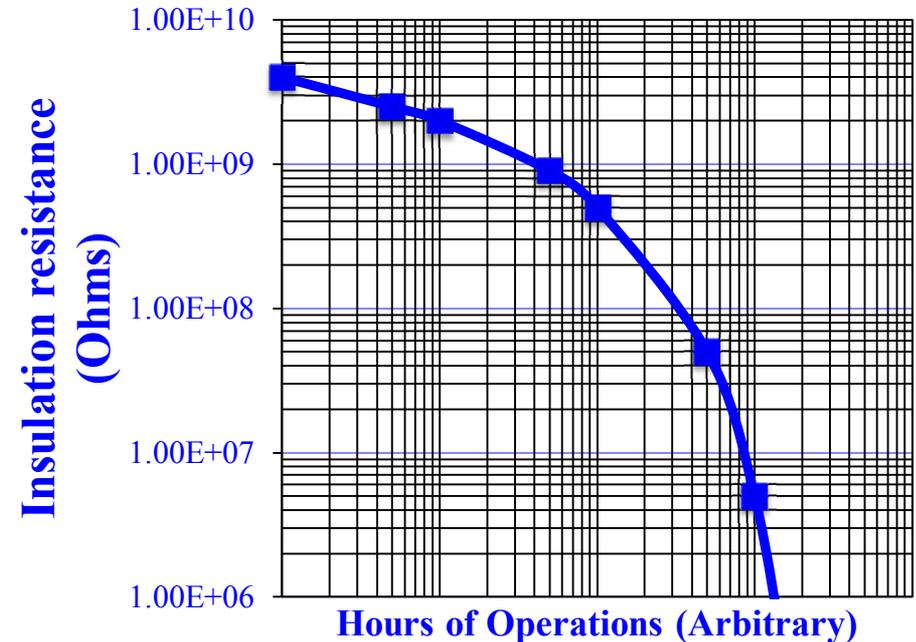
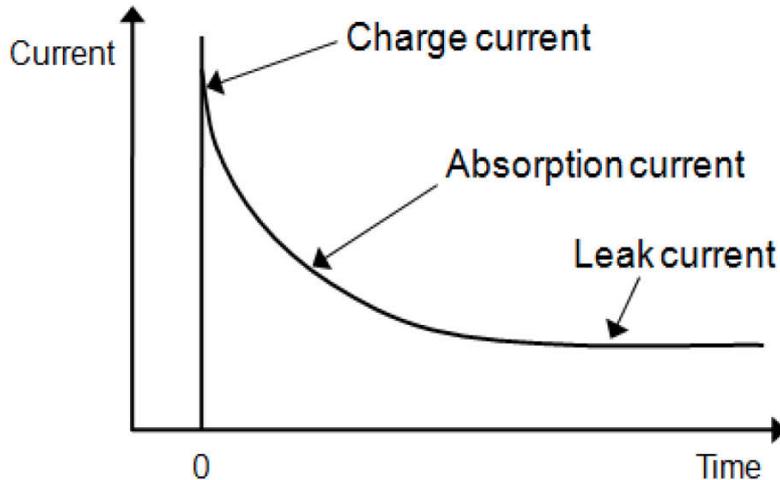


Physics of Failure



Section 514

Mission Assurance Office



- *Insulation Resistance = applied voltage/leakage current*
- *As time increases, electromigration of oxygen vacancies from core to interface across grain boundaries*
 - *Decreases resistivity*
 - *Tunneling current through grain boundaries*
- *Pile up of oxygen vacancies finally decreases resistivity to critical level*



Manage Risk with

Likelihood and Consequence Matrix



Section 514

Mission Assurance Office

Likelihood	5	>50%					HIGH
	4	>10%					
	3	>1%			MEDIUM		
	2	>0.1%					
	1	<0.1%	LOW				
			Minimal degradation, circuit performance not affected	Parametric degradation, degraded circuit performance	Part Failure, circuit failure. Mitigation scheme to restore	Part failure/circuit failure. No mitigation scheme	Part Failure/Circuit Failure. Failure of adjacent circuits
			1	2	3	4	5
Consequence							



Determine Capacitor & System Reliability Requirements



Section 514

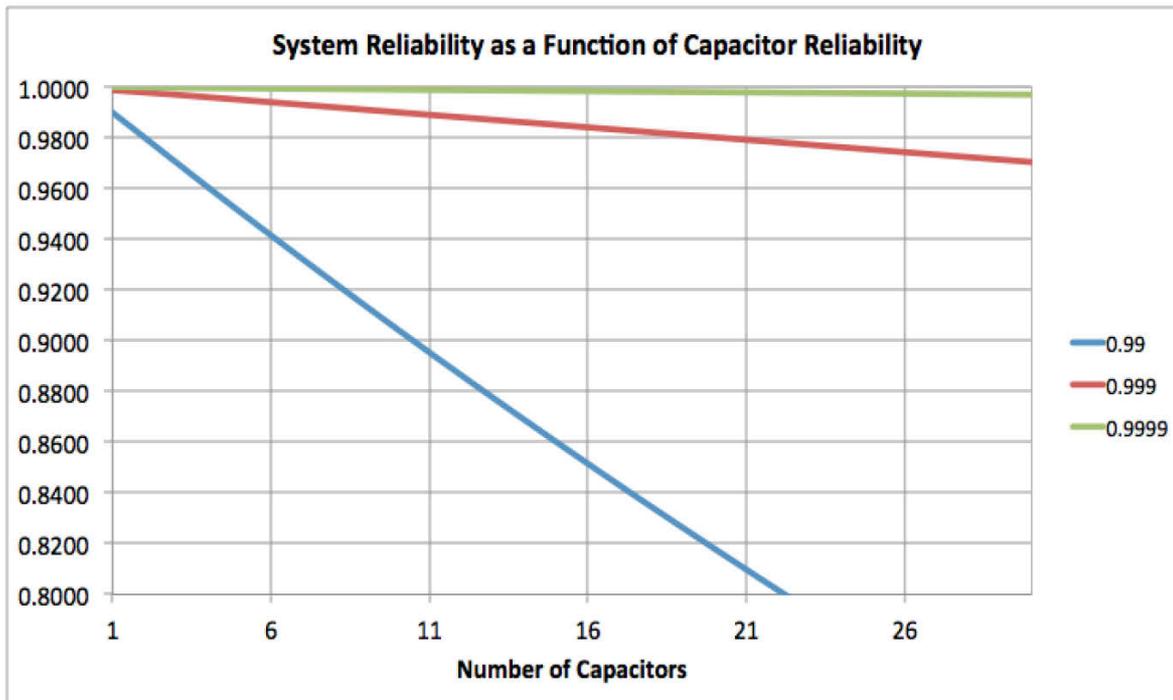
Mission Assurance Office

Capacitor System Reliability = Component Reliability^{#_of_capacitors}

# of caps	Capacitor Reliability			
	0.99	0.999	0.9999	0.99999
1	0.9900	0.9990	0.9999	1.0000
5	0.9510	0.9950	0.9995	1.0000
10	0.9044	0.9900	0.9990	0.9999
15	0.8601	0.9851	0.9985	0.9999
20	0.8179	0.9802	0.9980	0.9998
25	0.7778	0.9753	0.9975	0.9998
30	0.7397	0.9704	0.9970	0.9997

Xilinx FPGAs

*JPL needs capacitors with 4 to 5 9's reliability at the **END** of mission life to have a low likelihood rating.*





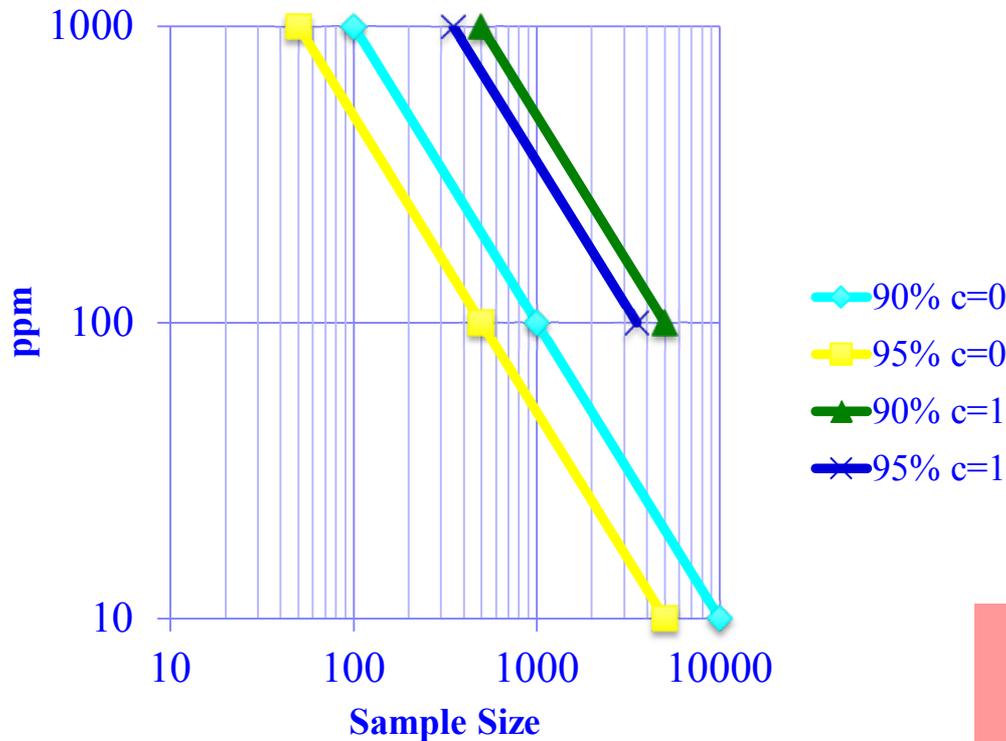
Sample Size Requirements



Section 514

Mission Assurance Office

Percent Defective (ppm) vs Sample Size vs Confidence Limit



MIL-S-19500G				
Max. % Defective (LTPD) with 90% Confidence				
	10	5	1	0.1
accept/rej	Sample Size			
c=0	22	45	231	2303
c=1	38	77	390	3891

Current life test have sample size variation

Xilinx Part #	Cap Size	Life Test Voltage (V)	Total	Fails (0 to 2000 hr)	Fails (2000 to 4000 hr)
BCC0013	0508	6	259	0	0
BCC0014	0508	9.45	138	0	0
BCC0019	0306	6	91	2*	0



COTS FIT Rates



USA / El Salvador / Malaysia

RELIABILITY ENGINEERING

QUARTERLY RELIABILITY SUMMARY

1st QUARTER 2011

PRODUCT: MULTILAYER CERAMIC CAPACITORS

TEST CONDITIONS: 2X-RATED VOLTAGE DC MINIMUM
MAXIMUM RATED TEMPERATURE

				AT RATED VOLTAGE & TEMPERATURE		AT TYPICAL USAGE CONDITION (0.5XRVDC & 50°C)			
DIELECTRIC GROUP	LOTS TESTED	PIECES TESTED	DEVICE HOURS	EQUIVALENT DEVICE HRS	FAILURE RATE (1/)	EQUIVALENT DEVICE HRS	FAILURE RATE (1/)	FAILURE RATE FITS - (2/)	MTBF
NPO/COG	230	29170	2.87 X 10 ⁶	2.30 X 10 ⁷	0.010	1.84 X 10 ¹¹	1.25 X 10 ⁻⁶	0.013	7.99 X 10 ¹⁰
X7R	659	104191	1.21 X 10 ⁷	9.64 X 10 ⁷	0.013	7.71 X 10 ¹¹	1.68 X 10 ⁻⁶	0.017	5.94 X 10 ¹⁰
X5R	26	3008	2.89 X 10 ⁵	2.31 X 10 ⁶	0.100	1.04 X 10 ⁹	2.22 X 10 ⁻⁴	2.216	4.51 X 10 ⁸

NOTES:

- 1/ Failure Rates are calculated in Percent Per 1000 Hours at 90% Confidence Level
- 2/ 1 FIT = 1 Failure in 10⁹ Hours (PPM per 1000 Hours) at 90% Confidence Level

Hours	FIT Rate (FITs)			
	0.1	1	10	100
100	1.00000	1.00000	1.00000	0.99999
1000	1.00000	1.00000	0.99999	0.99990
8760	1.00000	0.99999	0.99991	0.99912
43800	1.00000	0.99996	0.99956	0.99563
87600	0.99999	0.99991	0.99912	0.99128
131400	0.99999	0.99987	0.99869	0.98695

- *COTS AVX data shows strong dependence on dielectric.*
- *Space dielectric does not have this large database to leverage.*



Life Test Requirements



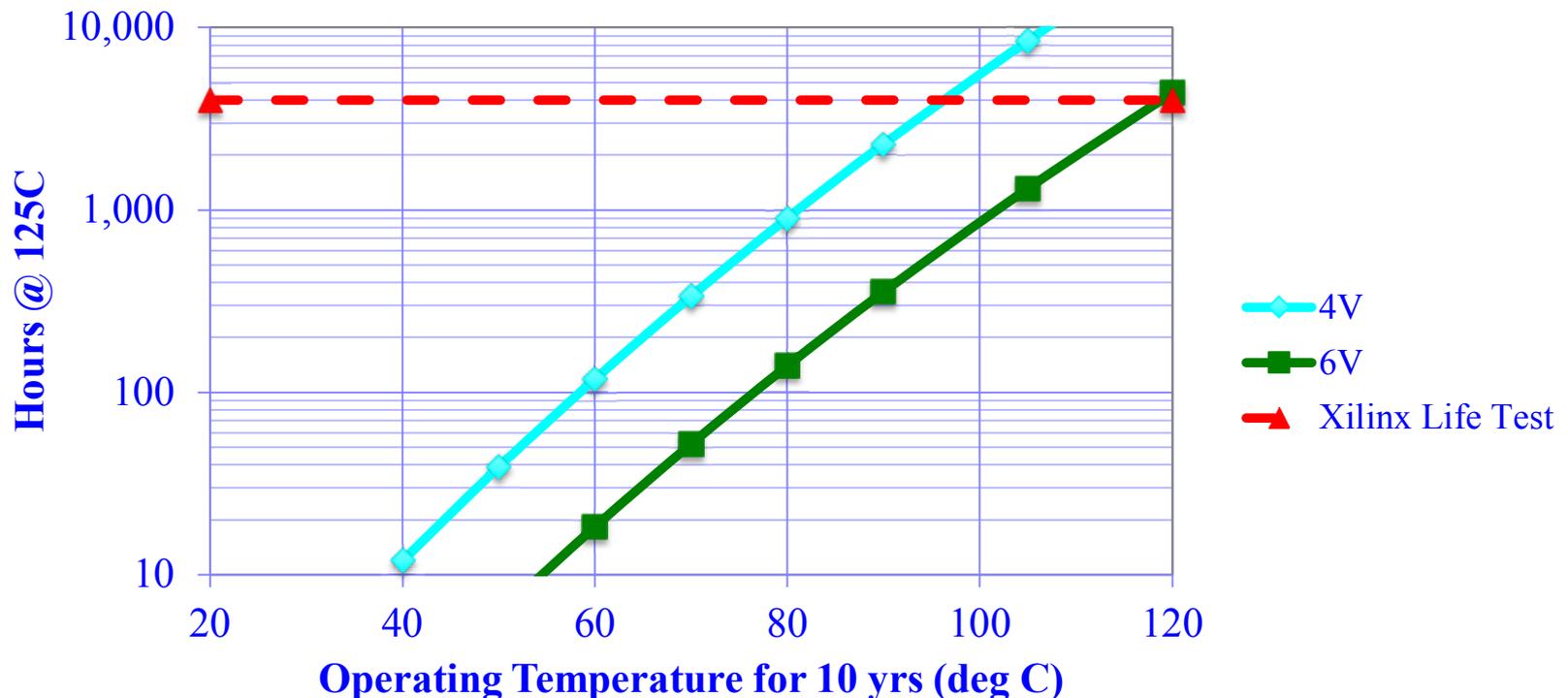
Section 514

Mission Assurance Office

$$\frac{t}{t_0} = \left[\frac{V}{V_0} \right]^{-n} e^{\left(\frac{E_a}{k} \left[\frac{1}{T} - \frac{1}{T_0} \right] \right)}$$

- T_0 and V_0 are life test conditions
- T and V are mission conditions
- $t =$ mission life, $t_0 =$ life test duration
- $E_a = 1.03$ and $n = 4.6$

Hours of 125C Life Test Required to Ensure 10 yrs of life at 3.4V for Various Temperatures & Voltage



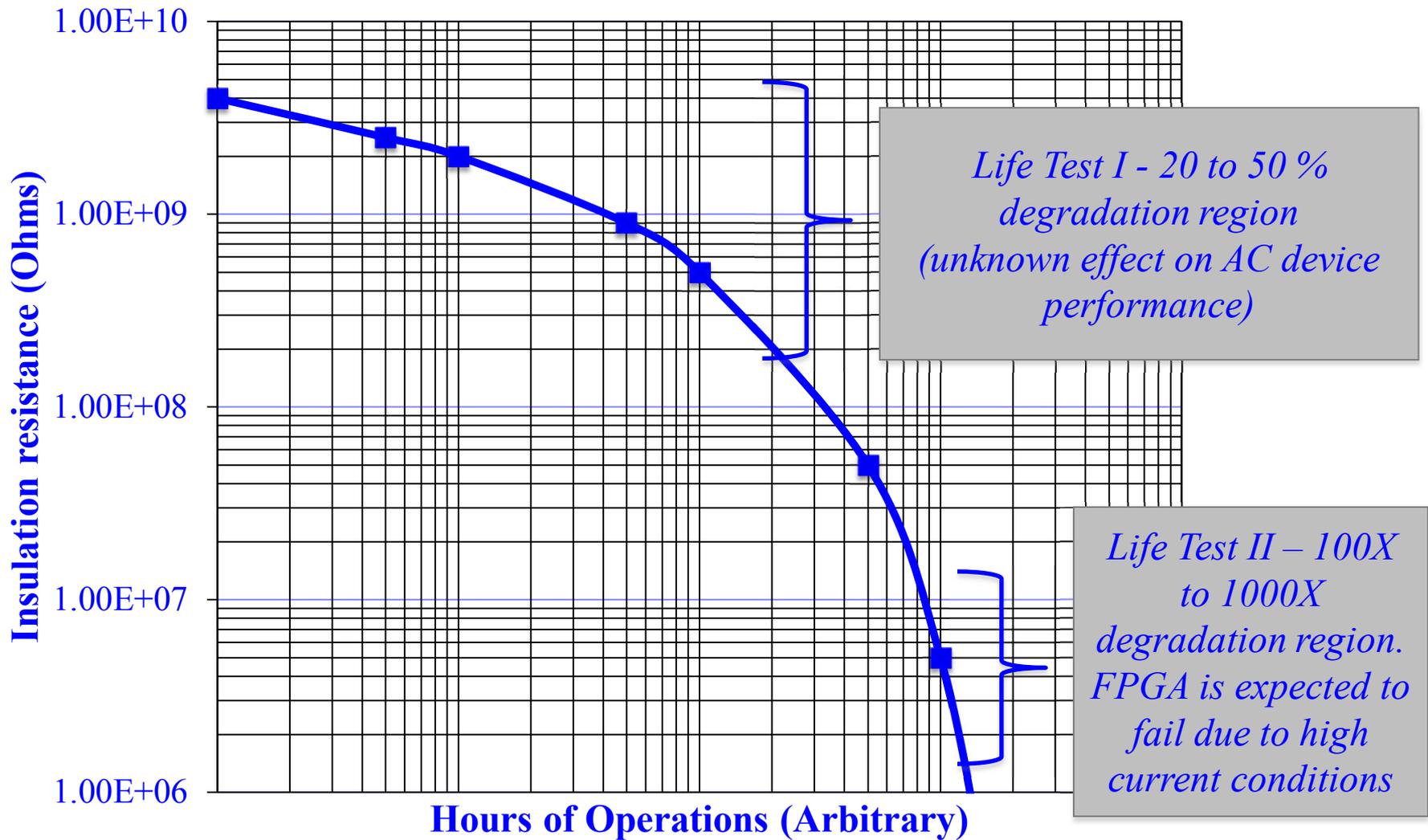


IR Degradation Life Test Analysis



Section 514

Mission Assurance Office



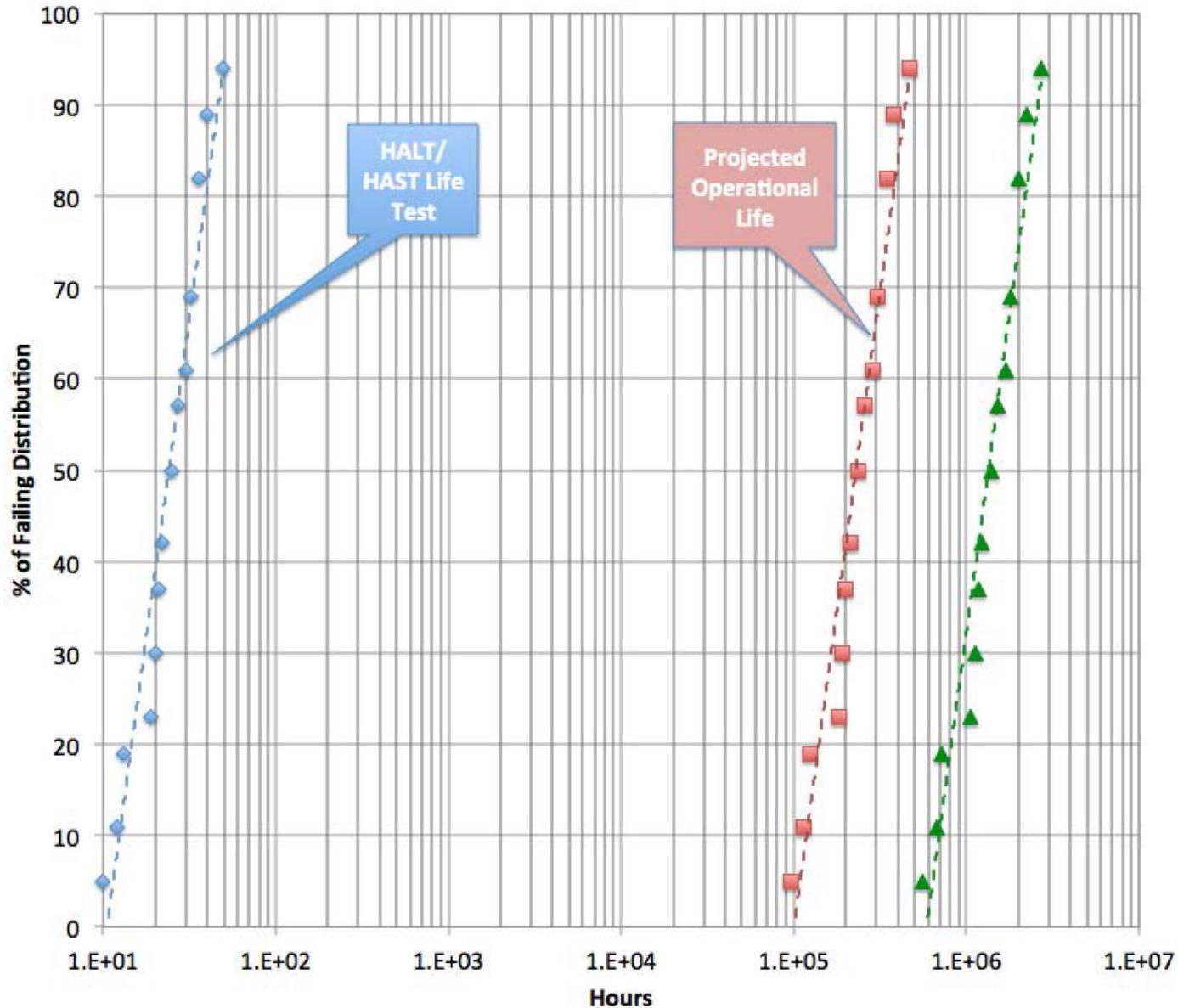


Life Test Predictions for Operational Conditions



Section 514

Mission Assurance Office



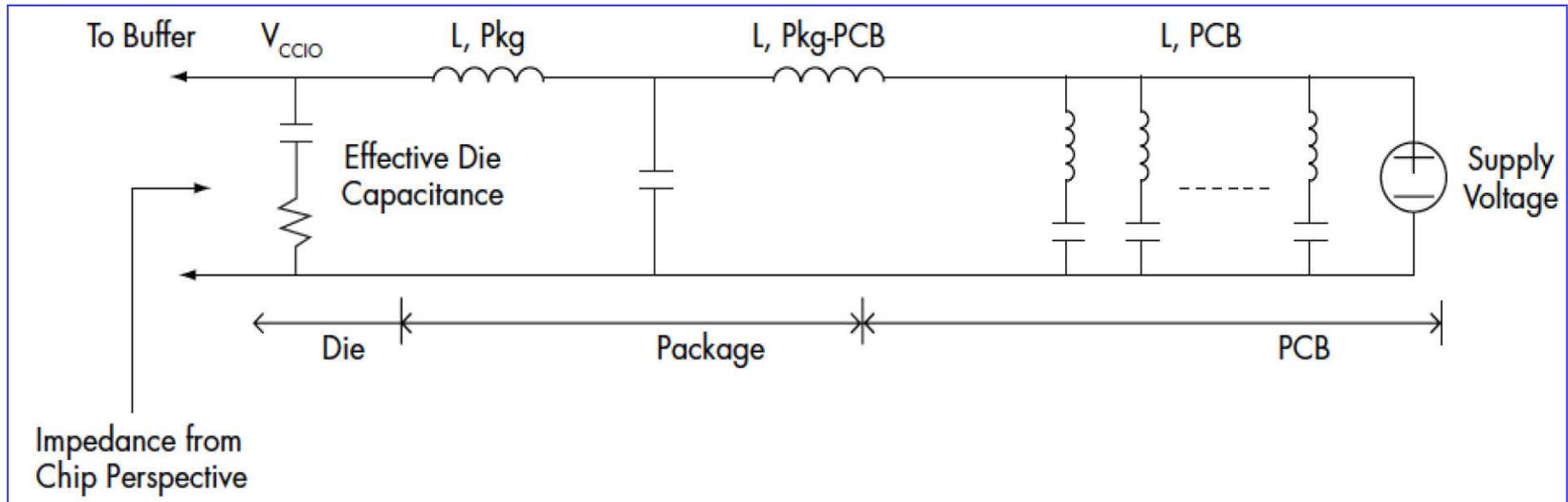


FPGA Power Distribution Network



Section 514

Mission Assurance Office



- High speed (>100MHz) operation requires sophisticated signal integrity management
- Maintain low impedance path from FPGA to supply through die, package, and PCB.
 - Different regions have frequency response ranges
 - Compensate for large swings in current until V_{supply} can respond
- BME caps on FPGA
 - Power/GND plane decoupling
 - Filtering
 - Series DC blocking for Gbit/sec links
- *What happens to PDN when BME degrades?*



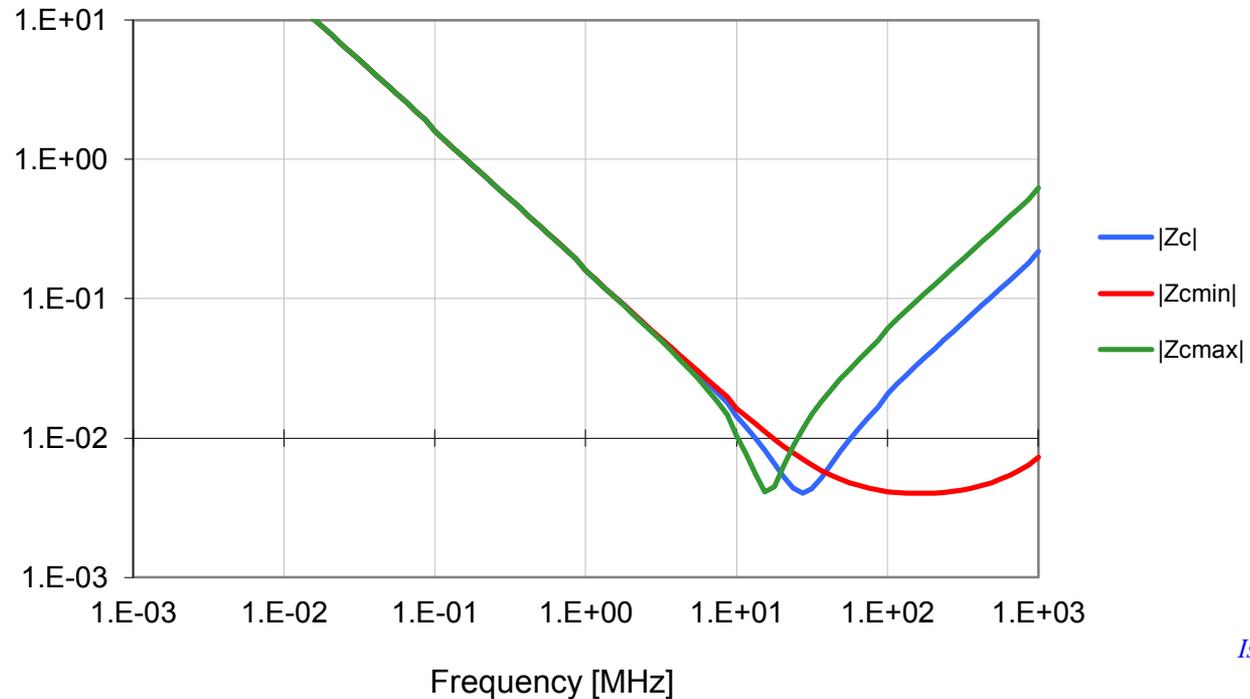
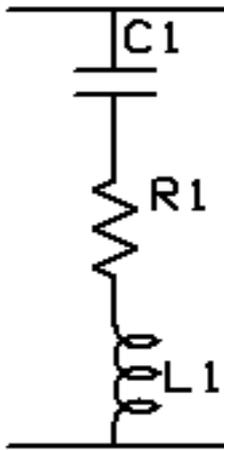
Effect of ESL Change on 0306



Section 514

Mission Assurance Office

Impedance of 0306 bypass capacitor [ohms]



Istavan novak

$$Z_C = R + j \left\{ \omega L - \frac{1}{\omega C} \right\} = \text{Re}\{Z_C\} + j \text{Im}\{Z_C\} = R + jX$$

$$C = 1.0 \mu\text{F}, \text{ESR} = 0.004 \text{ ohm}, L = 1, 35, 100 \text{ pH}$$



Summary



Section 514

Mission Assurance Office

- *Integrate reliability function of BME into FPGA reliability function with risk matrix.*
- *Significant sample size required to resolve acceptable levels of defects.*
- *Long term (> 1khrs) needed to cover long term high temperature mission operation.*
- *HAST/HALT data needed on exact space BME caps for operational predictions.*
- *Electric field based specifications are required to advance BMEs for general purpose use.*
- *Impact of the electrical degradation of the BME cap on FPGA performance is required portion of overall risk plan.*