The NASA Electronic Parts and Packaging (NEPP) Program – Parts, Packaging, and Radiation Reliability Research on Electronics

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Unclassified
Outline

- Overview of NEPP
  - What We Do and Who We Are
  - Flight Projects
  - Technology
  - Working With Others
- Recent Highlights
- Plans for FY13
- Challenges
- Summary
NEPP – What We Do

• **NEPP provides two prime functions for NASA**
  – Assurance infrastructure for NASA
  – Research on advanced/new electronic devices and technologies

• **We work with**
  – Active and passive semiconductors
  – Electronic device packaging
  – Radiation effects on electronics

• **We collaborate with others in technical areas such as**
  – Workmanship
  – Alert systems
  – Standards development and maintenance
  – Engineering and technology development

• **We provide an *independent* view for the safe use of electronic integrated circuits for NASA**

Electrical overstress failure in a commercial electronic device
NEPP’s Two Functions

• Assurance
  – Customer: *Space systems in design and development*
  – Issues applicable to currently available technologies (aka, mature technologies)
  – Examples
    • Cracked capacitors
    • Power converter reliability
  – NASA Electronic Parts Assurance Group (NEPAG) - a subset of NEPP
    • Communication infrastructure
    • Audit and review support
    • Investigation into reported failures (when of potential wide-reaching impact to NASA flight projects)

• Advanced/new electronics technology research
  – Customer: *Space systems in early design or conceptualization*
  – Issues applicable to new technologies (or those with potential Mil/Aero applicability)
  – Examples
    • Commercial field programmable gate arrays (FPGAs)
    • Sub 32nm electronics
  – Technology evaluation
  – Development of test methods and qualification recommendations
# The NEPP Program in a Nutshell

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## Core Elements

- Electronic Parts Reliability
- Radiation Effects
- Parts Assurance (NEPAG)
- Advanced Packaging
- Information Dissemination

## Focus Technologies

- Extreme Environments
- Sensor Technology
- Fiber Optics
- Radio Frequency
- Power Devices
- Scaled CMOS
- Passives
- Interconnects
- Memories
- Embedded Technologies
- SiGe Mixed Signal
- Area Arrays
- Programmable Logic
- Discretes
- Lead-free
- Systems on a Chip (SOC)

## Products/Deliverables

- Guidelines
- Specifications and Standards
- Test Methods
- Website Content
  - NASA Parts Selection List
  - Tools
  - Data
- Technical Reports
  - Bodies of Knowledge
  - Conference Papers

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NEPP for RHET presented by Steve McClure – Irvine, CA  October 10, 2012
NASA EEE Parts Assurance Group (NEPAG)

- Formed in 2000
- Weekly Telecons
  - International monthly
  - Typical participation ~ 35
  - Share knowledge and experience
  - Address failures, requirements, test methods
  - Monthly international
- Audit support
- Coordinate specification and standards changes
NEPP and NASA Flight Projects

**NEPP**
- Works general device qualification standards
- Develops the knowledge-base on **HOW** to qualify a device used by flight projects
  - Test methods
  - Failure mode identification
  - User guidelines and lessons learned
- Works issues that are relevant across NASA

**Flight Projects**
- Work mission specific requirements
- Qualify a device to mission requirements or to a standard
  - Uses NEPP knowledge to perform qualification
- Work issues relevant to a specific project

NEPP provides products for use by flight projects
Qualifying Electronic Technologies

**NEPP Perspective**

- Electronics in space face hazards significantly beyond the terrestrial/commercial environment
- *Qualification requires repeatable and statistically significant testing over relevant environments to ensure mission success*
- NEPP provides the basis for understanding the “how to” for electronics qualification
- Is this needed for commercial devices?
  - Previous independent review/testing has repeatedly shown discrepancies between industry claims versus independent test results that impact reliable usage in space

**Electronics Space Qualification**

- Shock/Vibration
- Ionizing Radiation
- Long Lifetime/No Servicing
- Vacuum
- Thermal
Maturity of Technology – The NEPP Model

- NASA flight project timelines are insufficient to learn how to qualify a new technology device
  - Sufficient time may exist to qualify a device, but not to determine **HOW to qualify**
- For 2016 launch, technology freeze dates are typically 2013 or earlier
- Technology development and evaluation programs need to be in place prior to mission design
  - NEPP’s strategic advanced planning on technology evaluation is critical to allow timely and safe flight project insertion of new technologies
Sample NEPP Technology Challenges

**Key Question:** Can we “qualify” without breaking the bank?

### Silicon
- <32 nm CMOS
- new materials such as CNT
- FINFETs
- 3D ICs

### Device Architectures
- system on a chip
- interconnects
- power distribution
- high frequencies
- application specific results

### Packages
- inspection
- lead free
- failure analysis
- stacking

### Connectors
- higher-speed, lower noise
- serial/parallel
- ruggedized, electro-optic

### Power Conversion
- widebandgap devices
- distributed architecture
- thermal modeling
- stability

### Passives
- embedded
- higher performance
- BME capacitors

### Board Material
- thermal coefficients
- material interfaces

### Design Flows/Tools
- programming algorithms, application
- design rules, tools, simulation, layout
- hard/soft IP instantiation

### Workmanship
- inspection, lead free
- stacking, double-sided
- signal integrity

### Related areas (non-NEPP)

*NEPP for RHET presented by Steve McClure – Irvine, CA  October 10, 2012*
Sharing NEPP Knowledge

• NEPP success is based on providing appropriate guidance to NASA flight projects
  – Interaction with the aerospace community, other government agencies, universities, and flight projects is critical.

• NEPP utilizes
  – NEPP Website: http://nepp.nasa.gov
  – NEPP 4th Annual Electronics Technology Workshop (ETW): Week of June 3rd 2013 (tentative)
    • HiREV (National High Reliability Electronics Virtual Center) Review Meeting to be held in conjunction
  – Standards working groups
  – Telecons (NEPAG weekly and monthly international)
  – Documents such as Guidelines, Lessons Learned, Bodies of Knowledge (BOKs)
Collaboration

• “Promote enhanced cooperation with international, industry, other U.S. government agency, and academic partners in the pursuit of our missions.” – Charles Bolden, NASA Administrator

• NEPP has a long history of collaboration. Examples include:
  – Direct funding and in-kind (no funds exchanged) support from DoD
  – Multiple universities
    • Vanderbilt, Georgia Tech, U of MD, Auburn University, …
  – Electronics manufacturers too numerous to mention!
  – International with major non-US government agencies

• We work with the NASA flight programs, but do not perform mission specific tasks
Consortia and Working Groups

• NEPP realizes the need to work in teams to provide better solutions

• NEPP utilizes working groups for information exchange and product development
  – External examples:
    • JEDEC commercial electronics and TechAmerica G11/12 Government Users
  – Internal (NASA-only) examples:
    • DC-DC converters, point-of-load converters, GaN/SiC, and connectors

• NEPP supports university-based research when funds allow
NEPP Recent Highlights (1 of 2)

• Continued leading Qualified Manufacturer’s List (QML) MIL-PRF-38535 Class Y development

• Released documents:
  – Single event effects (SEE) Test Guideline for FPGAs

• Documents in review (release in FY13):
  – Flash memory radiation test guideline
  – Solid state recorder (SSR) radiation considerations

• Firsts
  – Combined radiation/reliability tests of GaN devices, DDR-class and Flash memories
  – Radiation tests of
    • 28nm TriGate processor (proprietary data)
    • 32nm SOI processor (AMD)
  – Destructive SEE observed on Schottky Diodes
  – Independent SEE test of Xilinx Virtex-5QV
NEPP Recent Highlights (2 of 2)

- **3rd NEPP Electronics Technology Workshop (ETW) - June 2012**
  - 2.5 days of presentations
  - ~250 attendees including 50% via the web

- **Interesting assurance**
  - Hermetic seal test method intercomparison
  - Cracked capacitor evaluation

- **Recent test focuses (on-going)**
  - Power devices
    - GaN, SiC, and Si Power Device (radiation and combined effects)
  - FPGAs
    - Xilinx Virtex-5QV and Commercial (radiation)
      - Underfill (reliability)
  - Point-of-load (POL) Converters
Non-hermetic Package, With “Space” Features (CCGA?)

Space Challenge | Some Defenses
--- | ---
Vacuum | Low out/off-gassing materials. Ceramics vs polymers.
Shock and vibration | Compliant / robust interconnects - wire bonds, solder balls, columns, conductive polymer
Thermal cycling | Compliant/robust interconnects, matched thermal expansion coefficients
Thermal management | Heat spreader in the lid and/or substrate, thermally conductive materials
Thousands of interconnects | Process control, planarity, solderability, substrate design
Low volume assembly | Remains a challenge
Long life | Good design, materials, parts and process control
Novel hardware | Test, test, test
Rigorous test and inspection | Testability and inspectability will always be challenges
Gallium Nitride FET Radiation Effects

- GaN enhancement mode HEMTs are represent a considerable increase in PMAD capability
  - Intrinsically TID hard
  - Higher speed and smaller package for when compared to similar Si VDMOS
  - Ideal part for cubesat, microrovers, and missions needing high efficiency
- Single-Event Effects do present an issue
  - Latest generation parts show SEE failures comparable to silicon VDMOS
  - 80 V (40% of Vds) for Xenon
- SEE modeling, RF SEE, and reliability testing underway
  - FIT rate estimated on par with Si
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SOC Radiation Testing

- Developing radiation qualification methods for advanced SOCs
  - Like testing a combination of complex parts simultaneously...
  - Test efforts can easily be very expensive – we are looking for general ways to keep costs down
- Example: UT699 Register Partial Reset
  - Registers protected by EDAC – makes detection difficult
  - Event rate very low (<1/100,000 years Adams 90% worst-case GEO)
- Finding – must identify SEE well, and understand flux dependence

- Example: Maestro Integrated Test Chip (ITC)
  - Complex device response in ground radiation environments due to EDAC
  - Test software must run across multiple processor cores
- Findings – manufacturer debug tools should be used to examine SEEs, and Fault Tolerance impacts sensitivity
Current SOC Efforts

- Multi-core on P2020
  - Heat spreader cannot be completely removed
  - Developing DUTs exposing key areas of dies

Future SOC Efforts

- PowerPC P2020/P5020
  - Memory interface testing
  - Other IO interface testing

- Other
  - Working on follow up for newer Aeroflex device

- This work was supported by the NASA Electronic Parts and Packaging program (NEPP)
Reconfigurable FPGA Technology - Radiation

- Work with XRTC characterizing Xilinx XQR5VFX130 completed (GSFC to perform independent verification of results)
  - Results available on NEPP or JPL parts websites
- Beginning work to characterize 28nm, 0.85V Altera Stratix-V
  - Altera typically exhibited SEL, Stratix-IV was shown to be SEL immune.
  - Full device characterization to take place
- SEE characterization of other devices as applicable
  - e.g. Lattice Semiconductor’s ECP3 devices

Stratix-V Dev Board
NEPP Task Focuses – FY13

- **Goals:** Develop guidelines for qualification and radiation testing
  - Class Y Qualification (non-hermetic area array)
  - Flash Memory Qualification (reliability)
  - Flash Memory Testing (radiation)
  - Solid State Recorder (radiation)
  - DDR-class Memory (reliability)

- **Evaluate state-of-the-art commercial electronics (reliability, radiation)**
  - Memories, FPGAs, SOC Processors
  - Xilinx Virtex-7
  - Sub-32nm CMOS
  - Ipad™
  - Base Metal Electrode (BME) Capacitors
Sample NEPP Areas – Radiation Effects

Core Areas are Bubbles; Boxes underneath are variable tasks in each core

NEPP Research Categories – Active Electronics (1 of 2)

- SiGe. Mixed Signal
- Scaled CMOS
- Sensor Technologies
- Photonics
- Performance Tools

Legend
- DoD and NASA funded
- NASA-only funded
- Unfunded in FY13

IBM 9hp
- SiGe Physics Modeling
- Advanced Data Conversion, Amplifiers, Drivers
- Architectural comparison

Develops students at Georgia Tech

Commercial Devices
- Memories – Non-volatile, volatile
- FPGAs
- Processors, SOCs
- Structured ASICS

Test Structures
- Silicon on Insulator (SOI)
- Ultra-low power
- Below 32nm
- CNTs
- RHBD Support

Develops students at Georgia Tech

Partners include:
- DoD, IBM, TI, Intel, Boeing, AeroFLEX, Xilinx, Microsemi

Partners at:
- AFRL, Cypress, Ball

- IR
  - Visible
  - Cryo SEL
  - Others

- Fiber Amplifiers
  - Exotic-doped Fiber components
  - Wavelength Division Multiplexing
  - Free space Optical interconnects
  - Fiber Data Links
  - Optocouplers and PM Optocouplers

Develops students at Vanderbilt

Legend
- DoD and NASA funded
- NASA-only funded
- Unfunded in FY13
Estimated Test/Parts Costs Normalized to FY98

![Graph](image-url)

**Bottom line:**
Test costs have risen significantly, unfortunately NEPP budget hasn’t!
Disclaimer:
Statistics and “Radiation Qualification”

Commercial 1 Gb SDRAM
-68 operating modes
-can operate to >500 MHz
-Vdd 2.5V external, 1.25V internal

Device Under Test (DUT)

Single Event Effect Test Matrix

full generic testing

<table>
<thead>
<tr>
<th>Amount</th>
<th>Item</th>
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<tr>
<td>3</td>
<td>Number of Samples</td>
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<tr>
<td>68</td>
<td>Modes of Operation</td>
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<tr>
<td>4</td>
<td>Test Patterns</td>
</tr>
<tr>
<td>3</td>
<td>Frequencies of Operation</td>
</tr>
<tr>
<td>3</td>
<td>Power Supply Voltages</td>
</tr>
<tr>
<td>3</td>
<td>Ions</td>
</tr>
<tr>
<td>3</td>
<td>Hours per Ion per Test Matrix Point</td>
</tr>
</tbody>
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66096 Hours
2754 Days
7.54 Years

 Doesn’t include temperature variations!!!

Devices/technology are more complex: testing is as well
Budget Challenges for FY13

• The NEPP Program had a significant budget cut in FY13

• Reduction in efforts from FY12:
  – Areas unfunded or very limited in FY13 include
    • Photonics
    • Sensors/imagers
    • Mixed signal electronics
    • Commercial systems
    • University grants (research)
  – Fewer technology evaluations/tests
  – Commodities expertise at risk
  – Travel reduction impacts number of audits and meetings supported
Summary

• NEPP is an agency-wide program that endeavors to provide added-value to the greater aerospace community.
  – Always looking at the big picture (widest potential space use of evaluated technologies),
  – Never forgetting our partners, and,
  – Attempting to do “less with less” (rising test costs versus NEPP budget reduction).

• We invite your feedback and collaboration and invite you to visit our website (http://nepp.nasa.gov) and join us at our annual meeting in June at NASA/GSFC or via the web.

• Questions?
FY12 NEPP Technology Efforts – Part 1

Radiation Hardness Assurance (RHA) and Guidelines

Low proton energy SEE test guide –
Jonathan Pellish, NASA/GSFC
Ultra-ELDRS and ELDRS on Discretes –
Dakai Chen, NASA/GSFC

IR Array Lessons Learned – Cheryl Marshall, NASA/GSFC
FPGA Standard SEE Test Guide –
Melanie Berg, MEI Technologies – NASA/GSFC

Flash Memory Qualification Guide - Doug Sheldon, JPL
NVM Standard Radiation Test Guide –
Tim Oldham, Dell – NASA/GSFC
NVM Combined Radiation and Reliability Effects –
Tim Oldham, Dell – NASA/GSFC
DDR2 Combined Radiation and Reliability Effects -
Ray Ladbury, NASA/GSFC
Updated Solid State Recorder Guidelines –
Ray Ladbury, NASA/GSFC
Correlation of LASER to Heavy Ion Millibeam with FLASH Memories - Tim Oldham, Dell – NASA/GSFC

SEE Test Planning Guide – Ken LaBel, NASA/GSFC
Hydrogen and ELDRS – Philippe Adell, JPL

Devices

FPGA – Xilinx Virtex 5QV (SIRF) Independent SEE Testing -
Melanie Berg, MEI Technologies – NASA/GSFC
FPGA – Commercial Virtex 5 SEE –
Melanie Berg, MEI Technologies – NASA/GSFC
FPGA - Microsemi RTAX4000DSP SEE and ProASIC TID/SEE -
Melanie Berg, MEI Technologies – NASA/GSFC

FPGA – Microsemi ProASIC Reliability – Doug Sheldon, JPL
Class Y (non-hermetic area array packaged device qualification) and related tests (Xilinx and Aeroflex packages/devices) – Doug Sheldon, JPL
FLASH Memory Radiation Effects – Tim Oldham, Dell –
NASA/GSFC and Farohk Irom, JPL
Alternate NVM – MRAM/FRAM Reliability –
Jason Heidecker, JPL
DDR2/3 Radiation Effects and Combined Effects –
Ray Ladbury, NASA/GSFC
DDR2/3 Reliability – Steve Guertin, JPL
Newly Developed Si Power MOSFETs – Leif Scheick, JPL
and Jean Marie Lauenstein, NASA/GSFC
System on a Chip (SOC) Radiation Testing –
Steve Guertin, JPL
Newly Developed POLs Radiation and Reliability –
Dakai Chen, NASA/GSFC and Philippe Adell, JPL
CMOS Technology

IBM Technology and Radiation – Jonathan Pellish, NASA/GSFC w/ IBM, SNL, and NRL

INTEL Technology and Radiation (22nm FinFET processor – TID/Dose Rate) – Ken LaBel, NASA/GSFC w/ INTEL, NAVSEA Crane


Lyric Semiconductor Radiation – Jonathan Pellish, NASA/GSFC

Complex CMOS Device SEE Modeling – Vanderbilt University and Melanie Berg, NASA/GSFC

Physics-Based Modeling for SEE - Vanderbilt University

CMOS Radiation Testing  TBD Others: TI, ON, Cypress, STM

III-V, Widebandgap, and RF

90nm SiGe Radiation Effects (IBM 9hp) – Georgia Tech and Paul Marshall, NASA/GSFC – Consultant

SiC and GaN Power Device Radiation Testing – Megan Casey, NASA/GSFC and Leif Scheick, JPL

RF Device Screening Practices (Reliability) – Mark White, JPL

SiC and GaN Power Device NASA Working Group – Leif Scheick

SiC and GaN Reliability Testing – Richard Patterson, NASA-GRC

Miscellaneous SiGe Device Radiation Testing – NASA/GSFC

TBD GaAs HEXFET Radiation – NASA/GSFC:

We are tracking ESA research and determining applicability
Qualification and Packaging

Class Y related packaging tests CCGA/PBGA, underfill, etc... – Doug Sheldon, JPL (w/many others)

Cryogenic Connector Failure Analysis – NASA/JPL

Body of Knowledge (BOK) documents on multiple packaging-related areas (TSV, 3D packages, X-ray and Workmanship, etc) – NASA/JPL

BME, Tantallum, and Polymer Capacitor

Reliability/Screening – NASA/GSFC

DC-DC Converter NASA Working Group – John Pandolf, NASA/LaRC

NASA Connectors Working Group – Carlton Faller, NASA-JSC

Other

Infrared focal plane array lessons learned – Cheryl Marshall, NASA/GSFC

Development of SEGR Power MOSFET predictive technique – Jean Marie Lauenstein, NASA/GSFC

SEE Failures and Results Related to DC-DC Converter Design – Robert Gligiuto, MEI Technologies – NASA/GSFC

Point of Load NASA Working Group – Dakai Chen, NASA/GSFC

Optoelectronic Connectors and Transceivers – Melanie Ott, NASA/GSFC
NASA Electronic Parts Assurance Group (NEPAG)

Core Areas are Bubbles; Boxes underneath are elements in each core

NEPAG Focus Areas

- Failure Investigations
  - Investigate
  - Assess NASA Impact
  - Test/Analyze
  - Corrective Action
  - Lessons Learned

- Specs and Standards
  - US MIL
  - VCS

- Audits
  - US MIL

- Collaborations
  - National
    - International

- Parts Support
  - NPSL
    - Technical Expertise Resource
    - Bulletins
    - Connectors

- Consortia
  - CAVE
  - CALCE