



SDRAM SEFI on the Juno and MSL Projects

Steven M. Guertin, Farokh Irom, Greg Allen,
and Douglas Sheldon

Jet Propulsion Laboratory / California Institute of Technology
Pasadena, CA

Sponsorship of the NASA Electronic Parts and Packaging (NEPP) program acknowledged.

This work was performed at the Jet Propulsion Laboratory, California Institute of Technology,
Under contract with the National Aeronautics and Space Administration (NASA)

Copyright 2012 California Institute of Technology. Government sponsorship acknowledged.

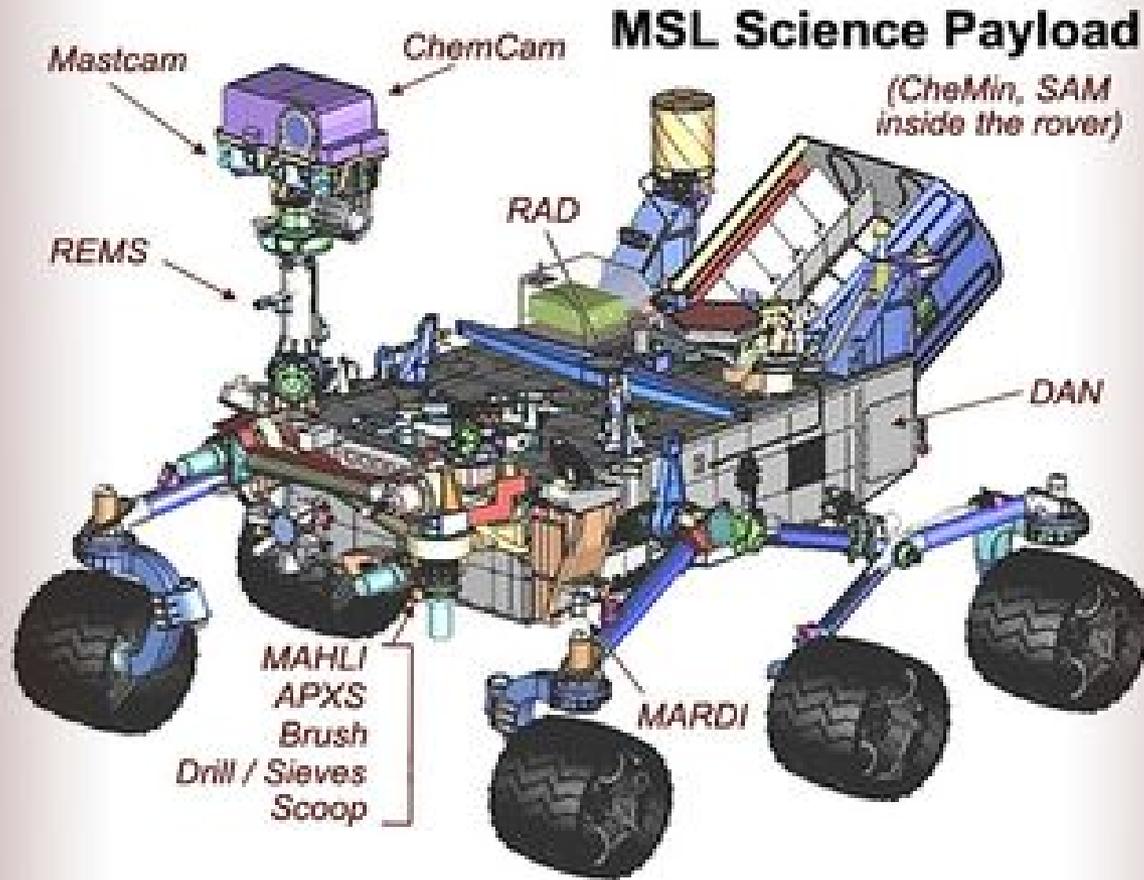


Outline

- Background on MSL/Computers
- Space events from Juno
- Radiation Testing
- Results
- Conclusion

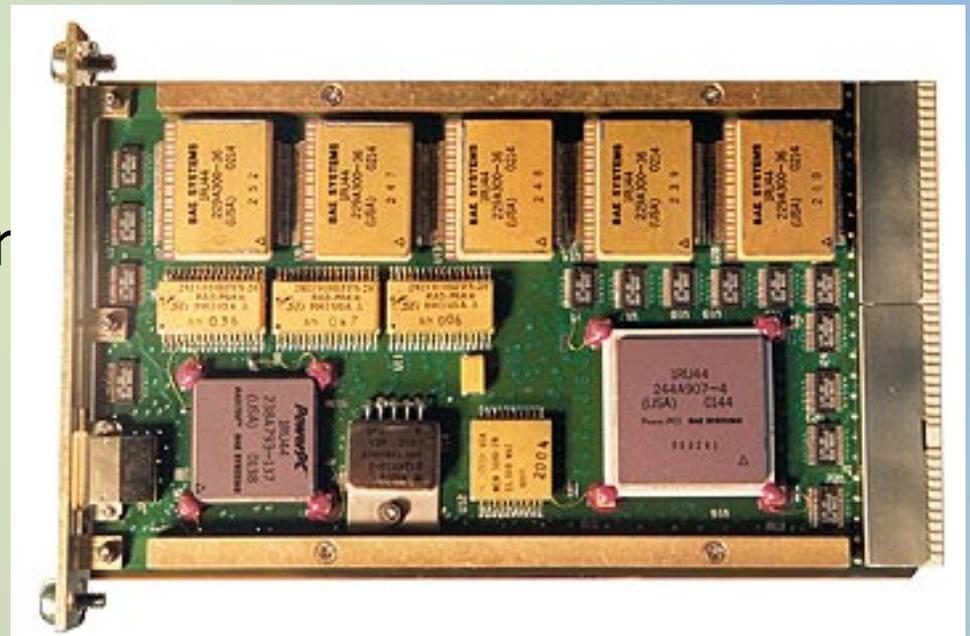
Special Note: A SEFI (Single Event Functionality Interrupt) here refers to an event that disrupts data stored in the SDRAM. The disrupted data is lost, but device operation may or may not have been affected

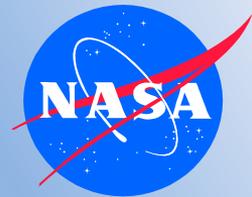
Quick MSL Overview



Rover Compute Elements

- MSL has two Rover Compute Elements (RCEs)
 - RAD750 computer with 256MB of memory
 - Memory is Elpida EDS5108 SDRAM
- RCEs involved in Entry Descent and Landing (EDL)
 - Analysis of images
 - Tolerant of distortion
 - Patched to be tolerant of SEFI





Events on Juno

- The Juno spacecraft was launched on August 5, 2011 and will arrive at Jupiter July 4, 2016
- Juno has a Data, Telemetry, and Command Interface (DTCI) card that has EDS5104 memory
 - Juno has 80 devices for 4GB of memory + EDAC
 - DTCI has experience 5 SEFIs during flight (about 1/3 months)
- Juno SEFIs:

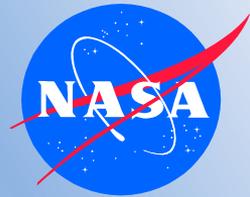


Error Type	Bits	Bank	Row Range	Column Formula	#MBEs	Changing Address Bits	
						#	Affected Bits
Band_Type	X,_,_,X	1	0x1000-0x13ff	(0x24,0xa4)x(0x200N)	2681	14	R0-R9, C5, C9, C11, C12
Band_Type	X,_,_,X	3	0x1000-0x13ff	(0x01,0x41)x(0x200N)	4349	14	R0-R9, C6, C9, C11, C12
Band_Type	_,X,X,_	2	0x800-0xbff	(0x20)x(0x200N)	3057	13	R0-R9, , C9, C11, C12
Band_Type	Unknown	3	0x1800-0x1bff	(0xe)x(0x200N)	4082	13	R0-R9, , C9, C11, C12



Juno Event Analysis

- Effort to understand events on MSL and Juno have indicated a high likelihood SEFIs come from the “Latch Array”.
 - Reloading the mode register fixes them, indicating a temporary remapping
 - Laser testing by Bougerol et. al. (2010) suggests fuse latch upsets result in addressing errors
- MSL does not have a mechanism to periodically reload the mode register
- This suggests that without mode register reload the memory may not be functional



Questions for MSL

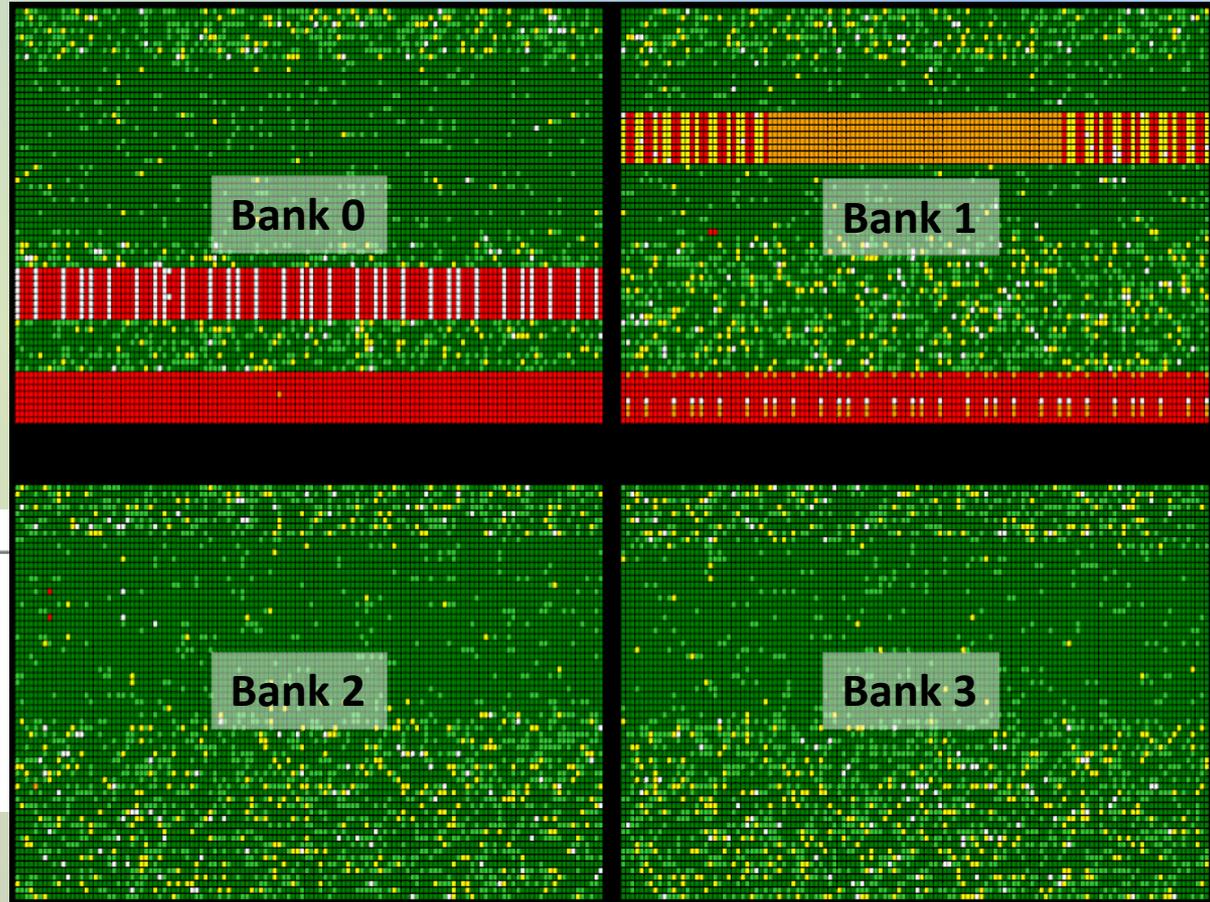
- The first Juno event occurred before MSL launch, and predicted rates for MSL were estimated around 1/month.
- A set of questions related to MSL's specific use of the EDS5108 was raised.
 - Since the EDS5108 is 8-bit instead of Juno's 4-bit, are single-ion MBUs a significant concern?
 - Juno SEFIs are 1 or 2 bits in each 4-bit word, does this hold true for MSL
 - Without mode register reload, what percentage of SEFIs result in a compromised memory device?
 - Is there any evidence of differences between read and write operations on SEFI rate?

Testing at BNL





Test Data



Bank 0

Bank 1

Bank 2

Bank 3

Color	Bit Errors in Row
Dark Green	No error
Light Green	1 SBU only
Yellow	2 SBUs only
White	3 or more SBUs
Orange	One or more Double bit error
Red	One or more Triple+ bit error

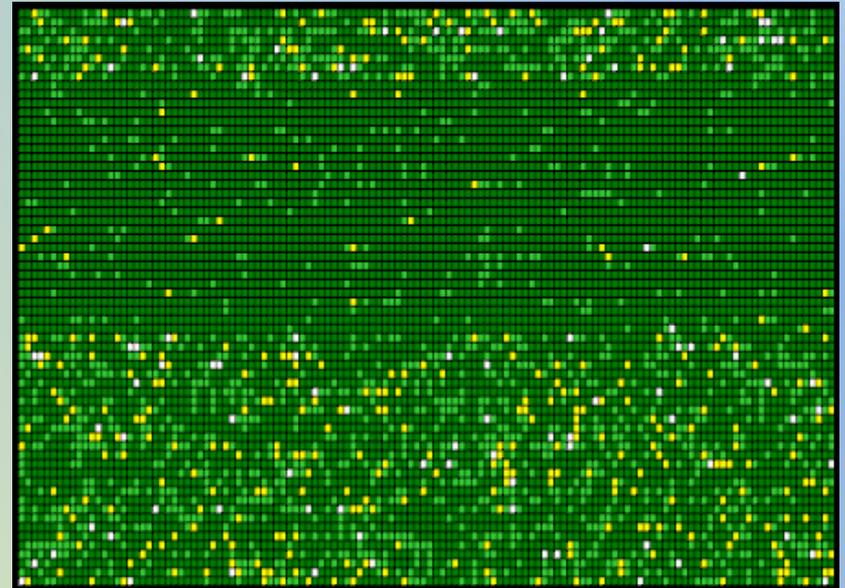
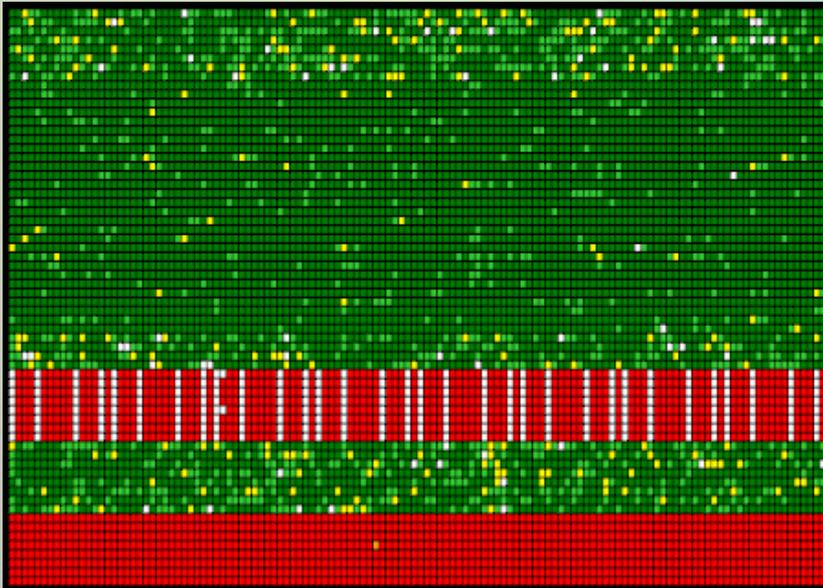
- Test data is collected with an eye towards logical mapping of errors.
- The various types of SEFIs and potential MBUs have different implications for EDAC systems.



Testing Highlights

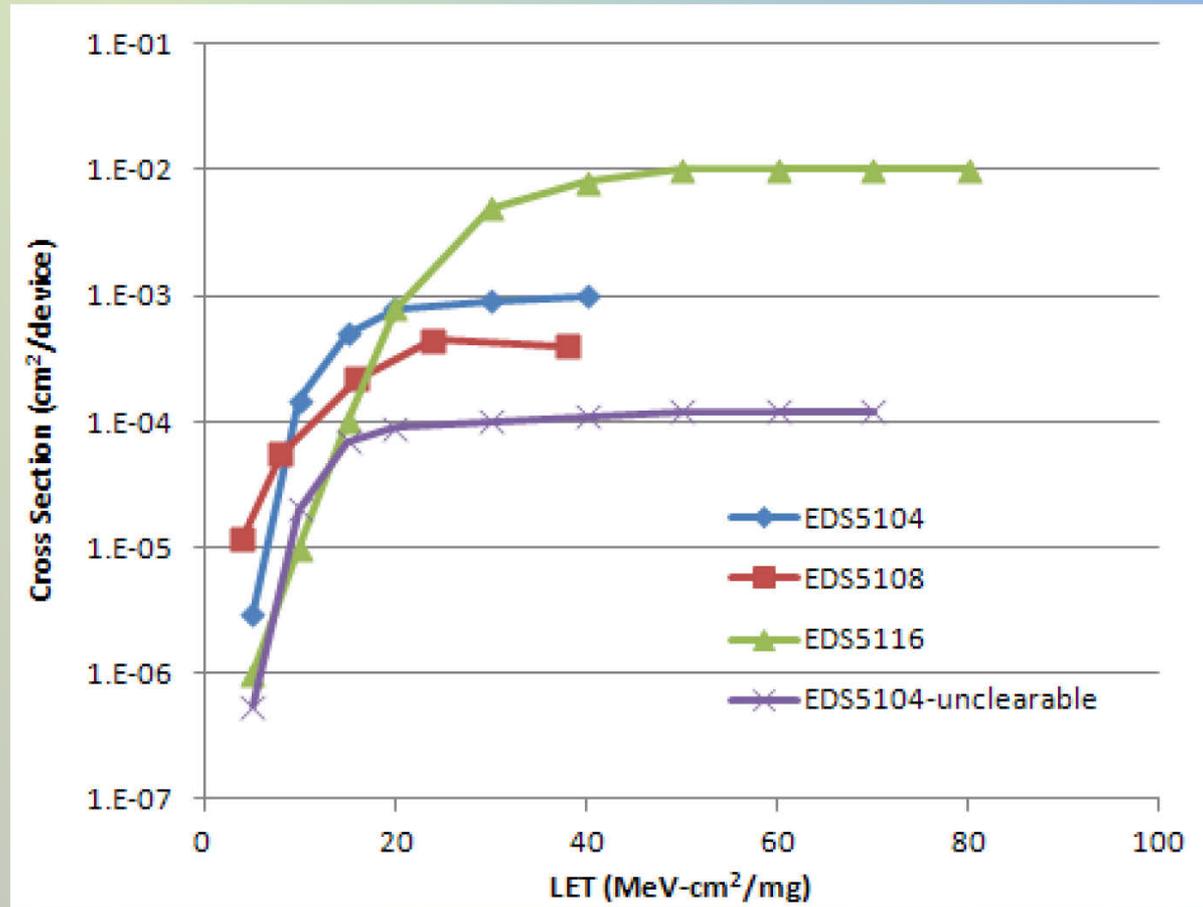
- Testing performed on flight lot parts at BNL
- Utilized modified JPL test system
 - Full capture of read operations with device snapshot.
 - New device snapshot every 20 seconds.
- Observed SBUs, rare MBUs (about as frequent as SEFIs), and SEFIs (affecting up to 4 bits, with patterns: X,X,_,_,_,X,X and _,_,X,X,X,X,_,_)
- SEFIs were row-type with 11 affected column bits and 1 or 2 affected row bits or band-type with 10 affected row bits and 2 or 3 affected column bits.
- No significant changes in event cross section with usage (write/read/refresh).

Effect of Mode Reload on a SEFI



- Band SEFIs on the left are cleared by reloading the mode register in the EDS5108, producing the error map on the right.
- Approximately 90% of SEFIs are affected this way
- Only issue is whether or not the affected memory is accessed between the SEFI and the mode register reload operation...

SEFI Test Results

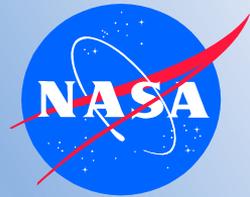


- EDS5104 and 5108 results were very similar.
- The lower curve (purple) shows that about 90% of SEFIs are effectively handled by reloading the mode register (but 10% still remain).
- EDS5116 results are impacted by testing a subset of the device and extrapolating.



SEFI during Flight on MSL

- A SEFI was observed on RCE-B when it was not primary
 - if it had been primary, it would have caused a swap to RCE-A
 - Only able to record the address list (not the data)
- Bank = 11 (3)
- Row 1 = 0_1100_0000_0110
- Row 2 = 0_1110_0000_0110
- All columns potentially affected (11 column bits) – total affected address range was 12 bits (which is the same as 13 bits on the EDS5104)
- NOTE THAT ALTERNATING ROW IS R9!
 - This is consistent with ground “row SEFIs” with only two rows impacted
 - Predicted: there might be two “hidden rows”, which would be close to the two observed - Estimated worst case address range of event is 0x0d80_4000-0x0de0_dffc
 - Actual mode reload on MSL resulted in two additional rows within the predicted range.



Conclusion

- Reload mode registers on SDRAMs/DDRs
 - But may only buy you a factor of 10 - you still need engineering
- Events on Juno prompted examination of SEFI impact on MSL.
- Testing performed to examine MSL's x8 version of device
 - no significant risk of degraded performance without mode reload
 - SEFIs observed to impact up to 4 bits
- Flight event on MSL
 - Luckily captured due to occurring on “non-prime” RCE
 - Event was “row SEFI”, and scrubber corrupted many additional bits
 - Recovery operation failed to remove MBEs due to additional corruptions