National Aeronautics and Space Administration

Single-Event Transient Testing of Low Dropout PNP Series Linear Voltage Regulators

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1.0 INTRODUCTION

Analog single-event transients (SETs) result from the interaction of a heavy ions or high-energy protons with a sensitive device in an analog integrated circuit (IC). Ion-induced electron-hole pairs in the semiconductor can lead to current transients on the transistor terminals that propagate through the IC and result in significant transient voltage excursions in the output. These variations represent a threat for space systems since a transient pulse can propagate from the device through a system and can result in temporary or permanent failure [1–8]. It is also difficult to assess the impact of this phenomenon on system-level reliability since the experimental data obtained for a particular IC depends highly on the application in which the IC was tested.

There is growing demand for high-speed, on-board digital ICs on spacecraft, reducing design margins in terms of voltage ripple, transient response, and efficiency for which linear regulators remain very attractive for space power systems. They offer a simple design, low noise, low power consumption, and a rapid transient response to load conditions. They can be used over a wide range of load capacitor values, load currents, and input voltages. However, they are very sensitive to SETs. They have been shown to have a low linear energy transfer (LET) threshold for low amplitude transients, making it likely that protons will induce transients in addition to heavy ions [9]. The wide range of input voltages and variation in output loading conditions are critical parameters in determining SETs for these devices, but increase the complexity of radiation testing and data evaluation. It has also been reported that in some cases SETs can induce large signal instabilities [10].

The goal of this document is to provide recommendations about the SET assessment of low dropout (LDO) PNP series linear regulators that are implemented in power distribution architectures. Through several experiments on various flight candidates and simulations we demonstrate the importance of key elements that have to be taken into account for proper SET evaluation and interpretation. Those include the role of board layout, load currents and load type selection, and the SETs dependence on output capacitor selection and its equivalent series resistance (ESR). To our knowledge, this is the first time that such practical recommendations are provided and will be added to the NEPP SET guideline, written by C. Poivey (GSFC). We intend for this paper to help test engineers, flight designers, and radiation specialists in using the appropriate tools to properly evaluate those designs. Finally, due to additional protection circuits implemented in linear regulator topologies, we revealed the existence of a thermal shutdown mode that can be triggered by a load-dependent single event.

2.0 IMPACT OF EQUIVALENT SERIES RESISTANCE ON REGULATOR SET RESPONSE: SIMULATION RESPONSE

A basic representation of a generic series linear regulator is given in Figure 2.0-1. A regulator uses a power bipolar transistor that behaves like a variable resistor and is placed in series with the load and modulates the output current. In combination with the load resistance (R_L, illustrated to the right of the ESR model) at the output, the pass transistor forms a voltage divider to reduce the unregulated input voltage to the regulated output voltage. The output voltage is sampled, scaled, and then compared to an input reference voltage. An error amplifier generates an output voltage proportional to the difference between these two voltages, which in turn biases the pass transistor though a base driver circuit. The sampling circuit and error amplifier form a negative feedback loop that maintains the regulator output voltage. A key element for the loop stability is the selection of the output capacitor.

It is common knowledge that a capacitor contains unwanted parasitic elements that typically degrade electrical performance. One of the most important parasitic elements is the ESR. Capacitors that are not properly selected during flight design and SET characterizations can lead to electrical stability issues and variation in the transient response. Figure 2.0-2 illustrates the latter point.

Using the generic PNP series regulator design of Figure 2.0-1, we performed single-event SPICE simulations by striking sensitive transistors in the error amplifier circuit [11] for various values of ESR (0.12–0.3 Ω), following the modeling methodology used in [4]. Those values of resistance are representative values for screened capacitors. The regulator was designed to regulate at 3.3 V and a maximum load current of 1.5 A.

As shown in Figure 2.0-2 and Figure 2.0-3, for selected values of ESR (0.1–0.3 Ω) of the 20μF capacitor, we observed different transient responses. In Figure 2.0-2, when hitting the amplification stage of the error amplifier in the regulator feedback loop, the resulting negative-going transients show that transient peak amplitude variation can reach up to over 100 mV with changing ESR values; the transient durations also vary by a few microseconds and the settling times by a few tens of microseconds. For extreme cases, transients can induce sustained instabilities in the output. In Figure 2.0-3, similar to the negative-going transients, by striking transistors of the input stages, positive-going transients show similar trends with a peak amplitude that can vary from 50–150 mV depending on the ESR values; the transient duration is also affected by a few microseconds and a settling time that varies by a few tens of microseconds.

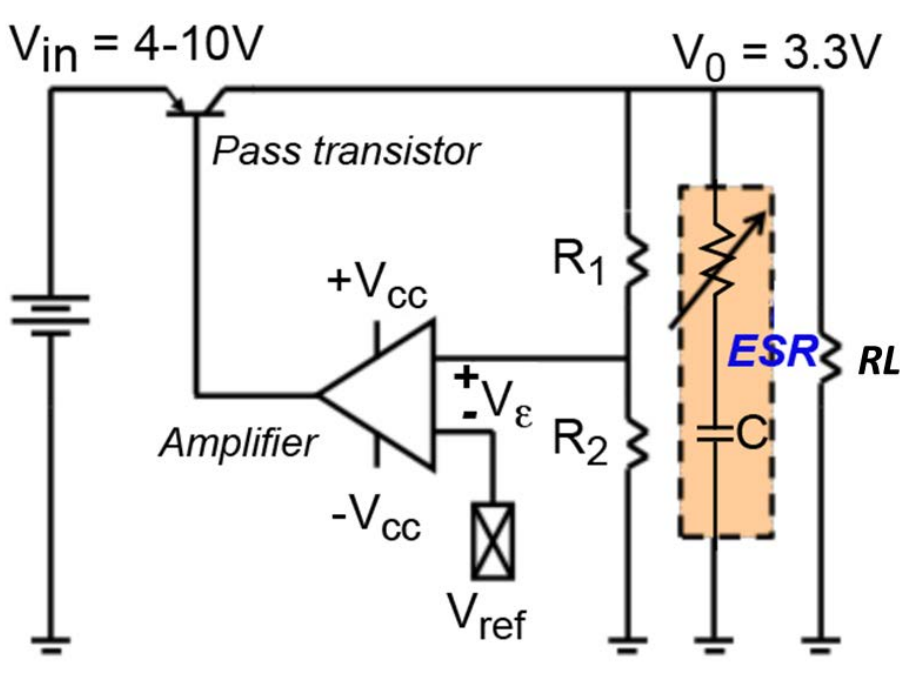


Figure 2.0-1. Illustration of a basic linear series regulator with output capacitor modeled as an ideal capacitor in series with an ESR.

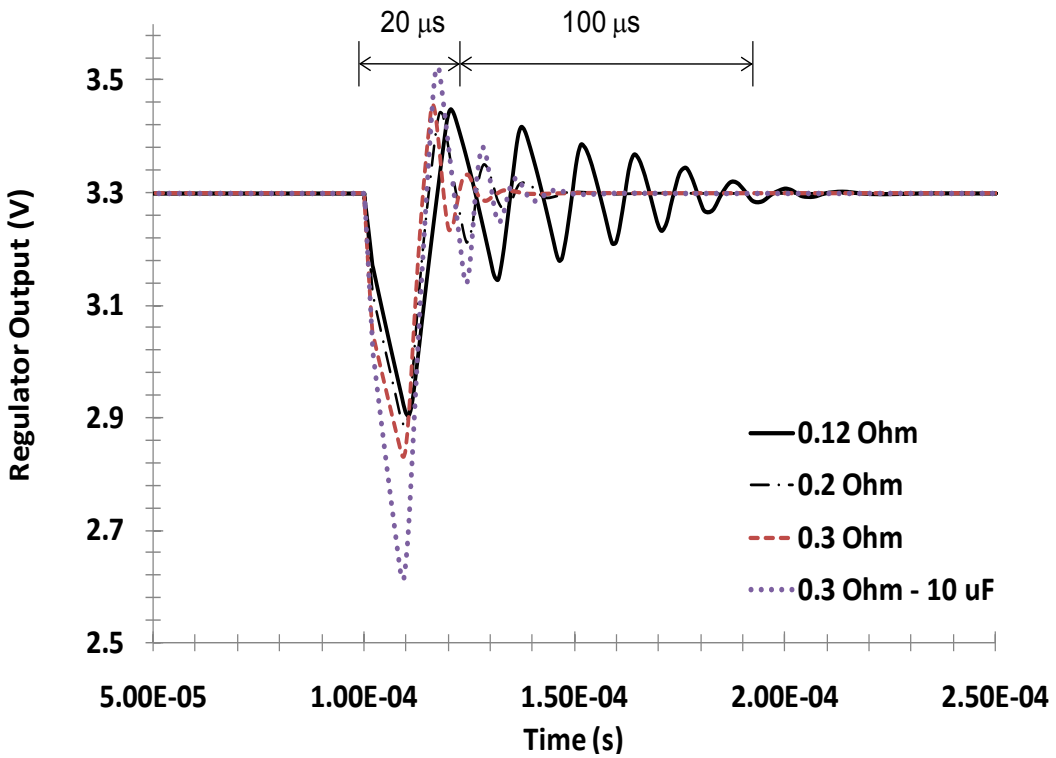


Figure 2.0-2. SET response of a generic linear PNP series regulator by striking a sensitive transistor of the amplification stage of the error amplifier [11]. The impact of ESR values on SET response is shown. Transient duration, peak amplitude, and settling time are all affected by changes in ESR.

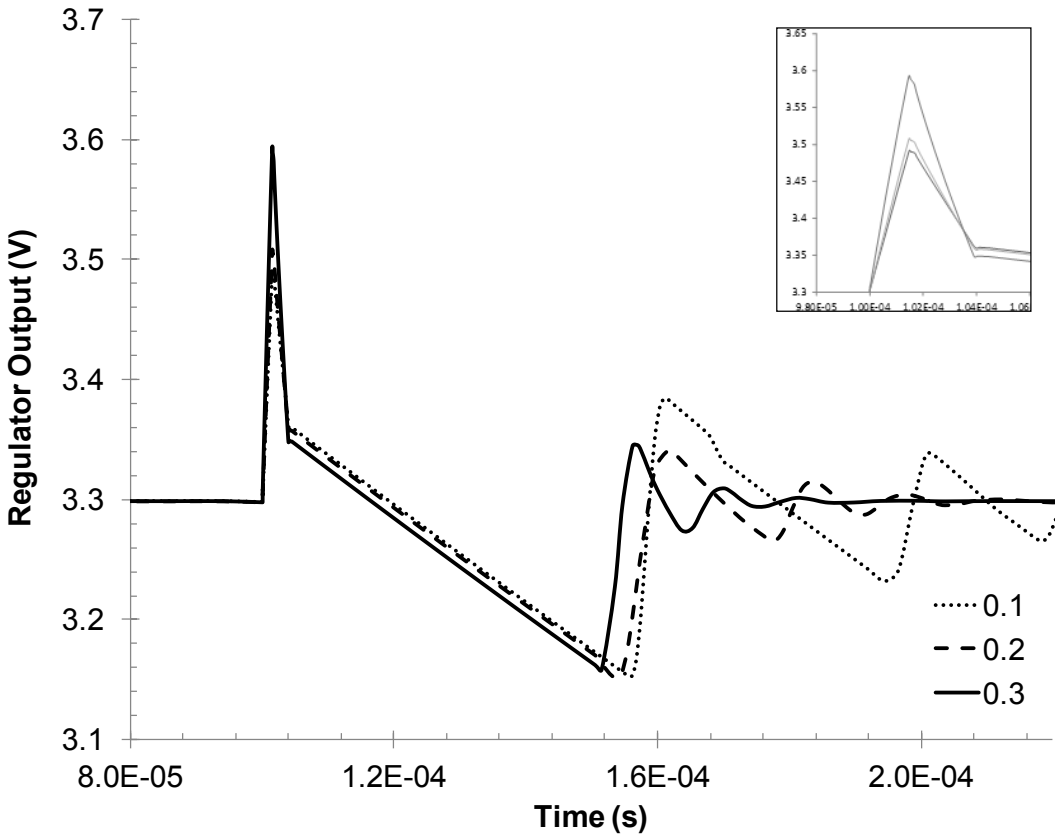


Figure 2.0-3. SET response of a generic linear PNP series regulator by striking a sensitive transistor of the input stage of the error amplifier [11]. The impact of ESR positive SET transients is shown. Transient duration, peak amplitude, and settling time are all affected by changes in ESR. The bias conditions of the regulator were: V_{in} = 5 V, V_{out} = 3.3 V and I_{Load} = 150 mA. The inset is a zoomed in view of the initial voltage transient.

Further single-event simulations were performed to study the effect of output loading for fixed values of ESR and output capacitor. Three output current values were considered: 150 mA, 750 mA, and 1.5 A. Results from the simulations are plotted on Figure 2.0-4. Data indicates that the transient peak amplitude gets worse as load current is increased as well as the duration. Indeed, the 1.5 A transient shows a peak amplitude of 800 mV and a duration of about 200 μs, whereas the 150 mA transient shows a peak amplitude of about 100 mV and a duration of about 100 μs.

These simulation results provide us with some insights about the key elements to consider when testing flight candidates for SET. The simulation allowed us to validate the experimental results using a micro-model. It provides insight about which part of the circuit is sensitive, in this case the amplification stage for negative transients and input stage for positive transients. Finally, we showed that ESR impacts both transient types, validating the experiments.

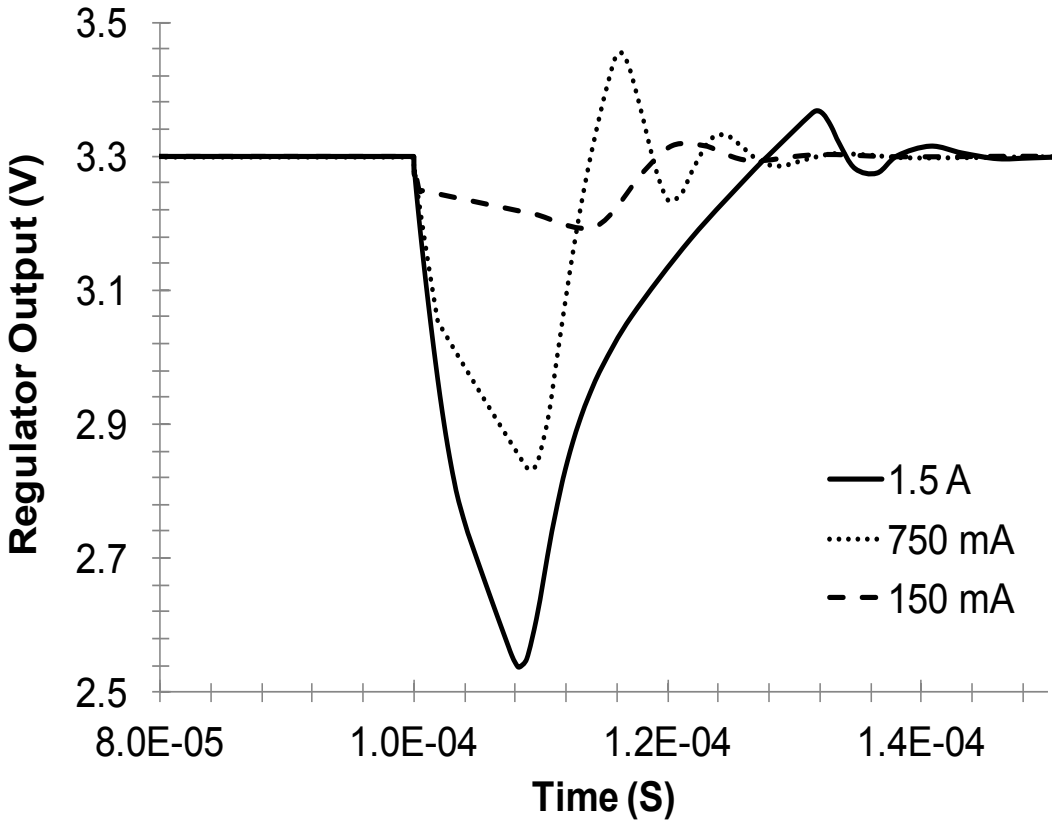


Figure 2.0-4. SET response of a generic linear PNP series regulator as a function of three load current: 1.5 A, 750 mA, and 150 mA for a fixed value of capacitor, 20°F and ESR of 0.3 Ω. The negative-going transients are worse for high load conditions, i.e., 1.5 A.

3.0 IMPACT OF INPUT VOLTAGE, LOAD CONDITIONS, AND LODE TYPES ON REGULATOR SET RESPONSE: LASER RESULTS

Several flight candidate PNP series regulators from M. S. Kennedy (MSK5920, MSK5900, MSK5058, and MSK5810) were selected for studying the impact of load conditions and input voltage on the regulators' SET responses. Their specifications are summarized in Table 3.0-1. All of the regulators we tested are configured in hybrid packages, meaning the power transistor and feedback circuits are on separate dies. SET assessments were performed using a single-photon-pulsed laser from either the Naval Research Laboratory (NRL) [12–14] or the Jet Propulsion Laboratory (JPL) [15]. Front-side irradiations of the devices were performed at both test facilities.

Laser SET irradiation techniques have been widely accepted in the radiation effects community and are representative of heavy ion effects for large linear technologies [15–19]. Laser irradiations allow for identification of the sensitive node of a circuit as well as for testing many configurations in a cost-effective manner. There are several methods by which an approximated LET value can be inferred or calculated from laser energy. Throughout this paper, the approximation we provided comes from agreements between the experimental correlation of similar technology heavy ion and broad beam test results on LM124, as well as a general model from [23].

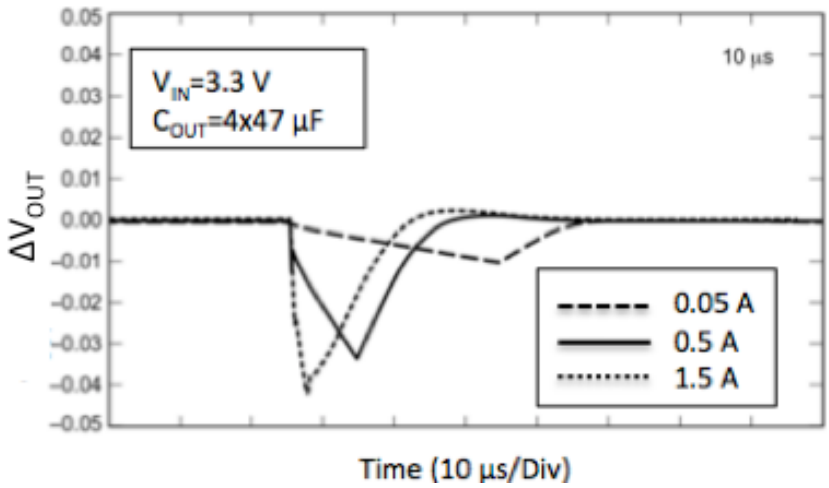
Table 3.0-1. PNP LDOs tested.

Part Number	ESR Range (mΩ)	Manufacturer	Output Voltage/Current	Package
5920RH	ESR<180	M. S. Kennedy	1.5V/5A	5-pin SIP
5900RH	ESR<180	M. S. Kennedy	1.5–6.8V/4A	5-pin SIP
5058RH	50<ESR<200	M. S. Kennedy	0.79–20V/2A	16-pin FP
5810RH	ESR<180	M. S. Kennedy	1.5–7/5A	16-pin FP
5010	ESR<180	M. S. Kennedy	3.3V/10A	5-pin SIP

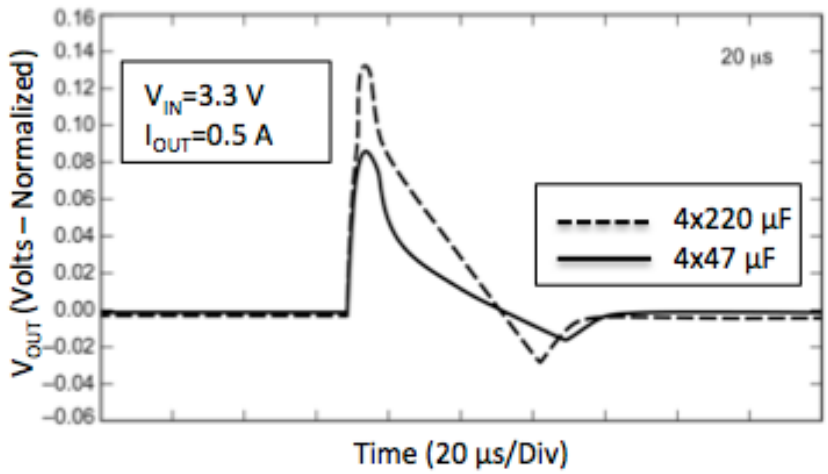
3.1 Bias and Load Variables

Figure 3.1-1 shows a first set of SET waveforms obtained from irradiations performed at NRL on the MSK5810RH LDO PNP series regulator. The laser's wavelength was 590 nm and the pulse width approximately 1 ps. The laser energy was selected to correspond to a heavy ion LET greater than, but on the order of, 100 MeV-cm^2/mg. An evaluation board from the manufacturer was also provided for this test. The MSK5810RH was characterized for SETs with various output capacitors, bias conditions, and load currents. Results are summarized in Figure 3.1-1 and, as it was demonstrated in the SET simulation section, show a strong dependence on output load and bias conditions.

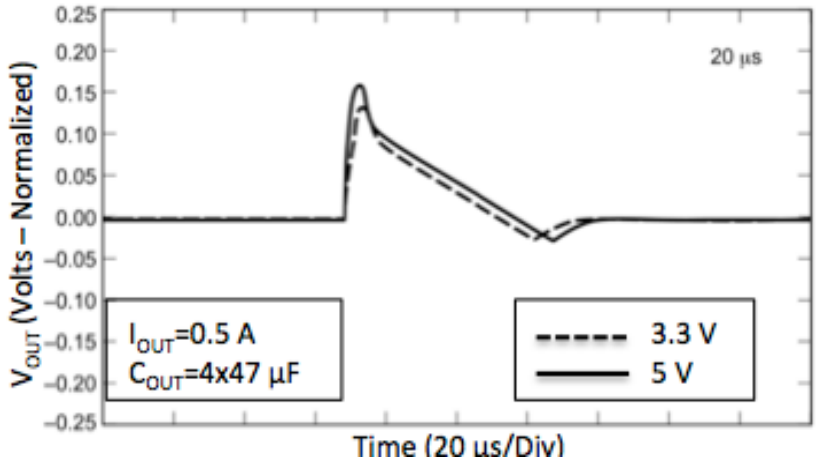
- Figure 3.1-1(a) shows negative-going SETs with three different load conditions: the dashed line is 0.05 A, the solid line is 0.5 A, and the dotted line is 1.5 A. The V_{in} was equal to 3.3 V and the capacitor (C_{out}) was equal to 4×47 µF for all three SET waveforms. The SET peak amplitudes were −9.7 mV, −33.5 mV, and −41.9 mV, respectively. Experimental results show similar trends as the simulation results in Figure 2.0-4.
- Figure 3.1-1(b) shows positive-going SETs: the solid line represents a SET using a total capacitor value, C_{out} equal to 4×47 µF, and the dashed line represents a SET using a total capacitor value, C_{out} equal to 4×220 µF. The SET peak amplitudes were 134 mV and 87 mV, respectively. The V_{in} was 3.3 V and the load current (I_{out}) was 0.5 A for both conditions.
- Figure 3.1-1 (c) shows positive-going SETs: the solid line represents a SET using a V_{in} of 5.0 V and the dashed line a SET using a V_{in} of 3.3 V. The SET peak amplitudes were 162 mV and 134 mV, respectively. The load current and output capacitor values were fixed; i.e., I_{out} equal to 0.5 A and C_{out} equal to 4×47 µF for both. It should be noted that the duration of the transients for conditions (a) and (b) is strongly affected by load current and capacitor selection.



(a) Load variation.



(b) Variable capacitive load.



(c) Variable V_{in}.

Figure 3.1-1. The ordinate is normalized in volts and the time scale for the abscissa is noted, per division, in the upper right hand corner for 5(a)–5(c).

To evaluate the impact of output voltage on the regulator SET response, additional data were obtained from irradiations performed on the MSK5900RH LDO PNP series regulator. Figure 3.1-2 shows SET waveforms resulting from irradiations performed on this device using JPL's picosecond laser facility. In this instance the laser's wavelength was 800 nm and the pulse width approximately 2 ps. The laser energy was approximately 55 pJ, corresponding to a heavy ion LET at or above 100 MeV-cm^2/mg. Custom test boards were designed for this test.

The device was characterized for various bias and load conditions; the highlighted result is shown in Figure 3.1-2. While the bias, load, and laser energy were held constant (V_{IN} = 5 V and I_{LOAD} = 50 mA), as well as the strike location, three values of output voltage were selected: 1.5 V, 1.8 V, and 2.5 V. Data indicated that, as the output voltage is increased from 1.5 to 2.5 V, the transient duration also increased by about 25%. However, the peak amplitude and shape of the transient was not affected. Similar observations were obtained when irradiating the MSK5920 PNP series regulator.

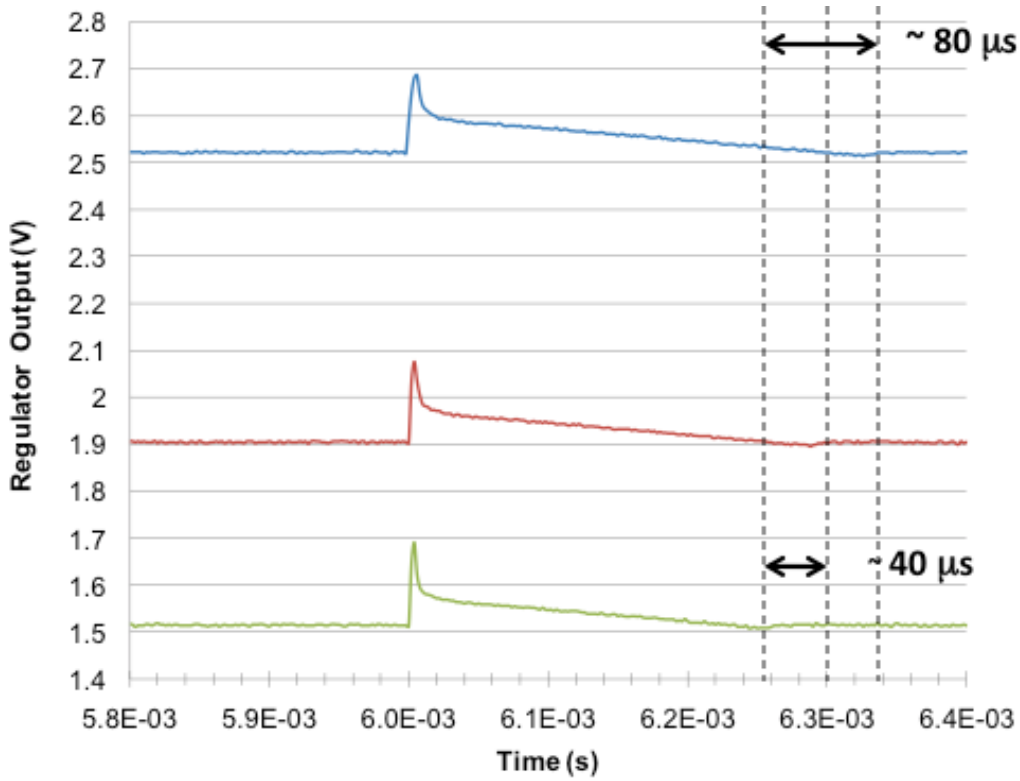


Figure 3.1-2. MSK5900 output transient signature for three irradiation conditions: the output voltage was set to 1.5 V, 1.8 V, and 2.5 V and laser energy was 55 pJ (~100 MeV-cm^2/mg). Input voltage was 5 V and output current 50 mA. Data show that transient duration increases with increasing output voltage for identical load conditions

3.2 Equivalent Series Resistance Impact on SET Response

As shown on Figure 2.0-1, ESR is a parasitic element that is an often overlooked, but distinguishing trait of every capacitor, often as important as the capacitance value itself, with respect to the LDO regulator stability and SET response. Nearly all LDO regulators manufacturers specify an ESR value range for their output capacitor selection to assure voltage stability.

It is well known that all voltage regulators use a feedback loop to maintain the output voltage at a constant DC level. As the feedback signal passes through the return loop, gain and phase changes occur due to the natural poles and zeros of the circuit. Typically, a stable loop requires at least 30 degrees of phase margin. Zeros are intentionally added to feedback loops to cancel out the effect of poles that would cause instability if left unbalanced. Hence, the selection of the output capacitor to force the gain to roll off

fast enough to meet stability requirements and its ESR component are critical variables to consider in LDO regulator designs.

The intent behind this research was driven by concern for voltage regulator SET test circuits not having appropriate attention paid to overall stability prior to testing; most of the focus was given to LDOs, where ESR is of greater concern. As was shown in the simulation section, the experimental results below will show that variable ESR values, within manufacturer specifications, would change the output transient characteristics up to the point that the circuit could go unstable; something we have only observed in simulation, i.e., we have not observed this effect in any of our testing. However, we have observed a noticeable effect of ESR on SET amplitude and duration.

To illustrate this latter point, Figure 3.2-1 show results of laser irradiation performed at JPL on the MSK5920RH-1.5 listed in Table 3.0-1. Several precision 47 µF output capacitors with various ESR values were selected for this evaluation. Each ESR measurement was performed with a calibrated network analyzer at 100 kHz and at room temperature, as specified in the manufacturer datasheet. Irradiations were conducted using a constant laser energy of 55 pJ (~100 MeV-cm^2/mg) and by striking the same sensitive node of the circuit. The input was 5 V and the output was fixed at 1.5 V. The load was passive and fixed at 50 mA. When using a 47 µF capacitor, three different ESR values were considered: 68, 152, and 198 mΩ.

As shown in Figure 3.2-1, data indicated that the SET magnitude and duration increase as ESR value increases: ΔV of approximately 0.15 V to 0.65 V with 68 and 198 mΩ measured 47 µF capacitors, respectively.

This behavior can be explained by the fact that when a laser strike occurs, the series pass transistor is fully turned on and gets into a saturation regime. The pass transistor in this regime behaves as a small value resistor (several tens of Ω) just after the SET occurs. Since the series transistor is directly connected to the regulator output, it is reasonable to think that the peak amplitude of the transient will be directly related to the ratio of the small resistance of the transistor in saturation and the ESR value of the output capacitor. Since the two values of resistance have a similar order of magnitude, it can be concluded that the SET peak response will be strongly affected by ESR. Simulations agree with this statement and show similar trends as the one obtained experimentally. Indeed, we showed that ESR directly affects the peak amplitude right after the SET occurs. It should be noted that few hundred mV is a non-negligible effect since those devices are typically used to power digital electronics that have very tight input transient requirements. Both simulations and experiments show that the impact of ESR is more sensitive at low load currents, i.e., few tens of mA.

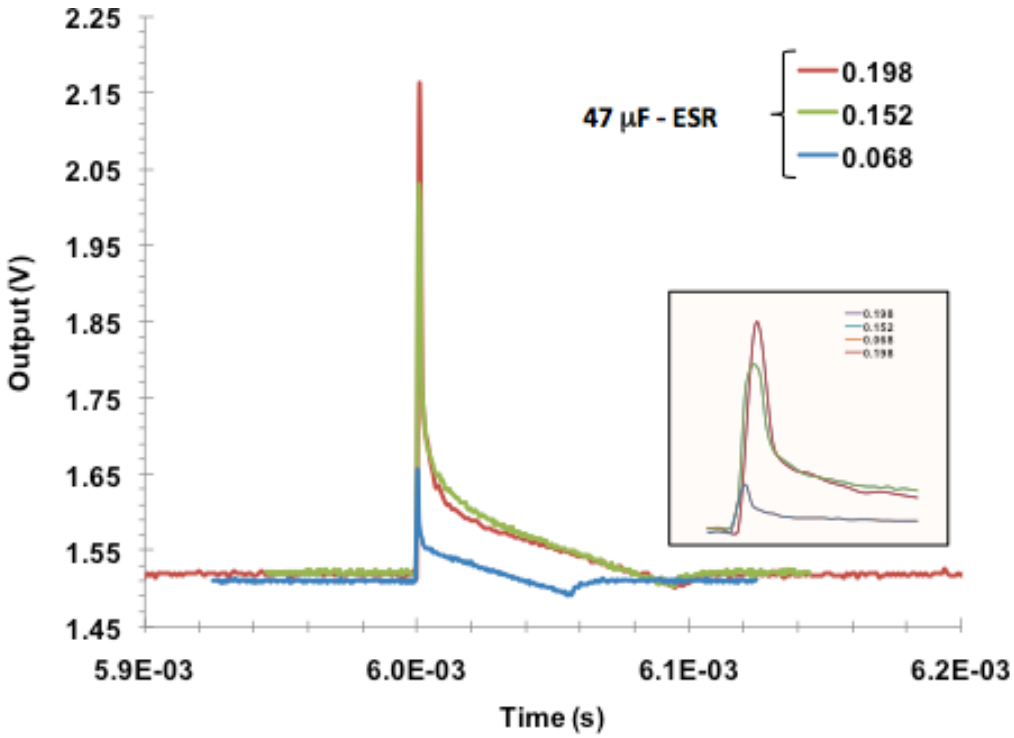


Figure 3.2-1. Impact of ESR on the regulator SET response for a fixed output capacitor and load current. The MSK5920RH was tested for SET with a V_{in} of 5 V, V_{out} of 1.5 V, a load of 50 mA, and a capacitive value of 47 µF. The capacitive load ESR was varied: 68, 152, and 198 mΩ. SET magnitude and duration were observed to increase with increasing ESR.

3.3 Load Variations and Board Layout Considerations

SET waveforms were also compared by either using an electronic load or physical loads near the device output. Both load types are commonly used during SET testing at heavy ion facilities. Figures 3.3-1 and 3.3-2 show the effect of load type, i.e., electronic load versus physical load on the SET waveforms from testing on another device, the MSK5058. The devices were operating from an electronic load at 1.5 A and 2 A respectively, each with a physical resistor of 1 Ω. In each instance, the SET obtained for irradiation using the physical resistors showed a slower slew rate relative to the SET from using the electronic load, resulting in a difference in transient amplitude of nearly 250 mV in the case of the MSK5058 and a slower shutdown in the case of the MSK5059. Such conditions are exacerbated when testing at accelerator facilities when the electronic load has to potentially be positioned at a physical location further from the output of the regulator. While for many circuits a delta as illustrated in the two results in Figure 3.3=1 may be of minor importance. Yet, as scaling pushes voltages lower and noise margins to smaller values, it may cross the threshold between noise and an unacceptable interruption in circuit function.

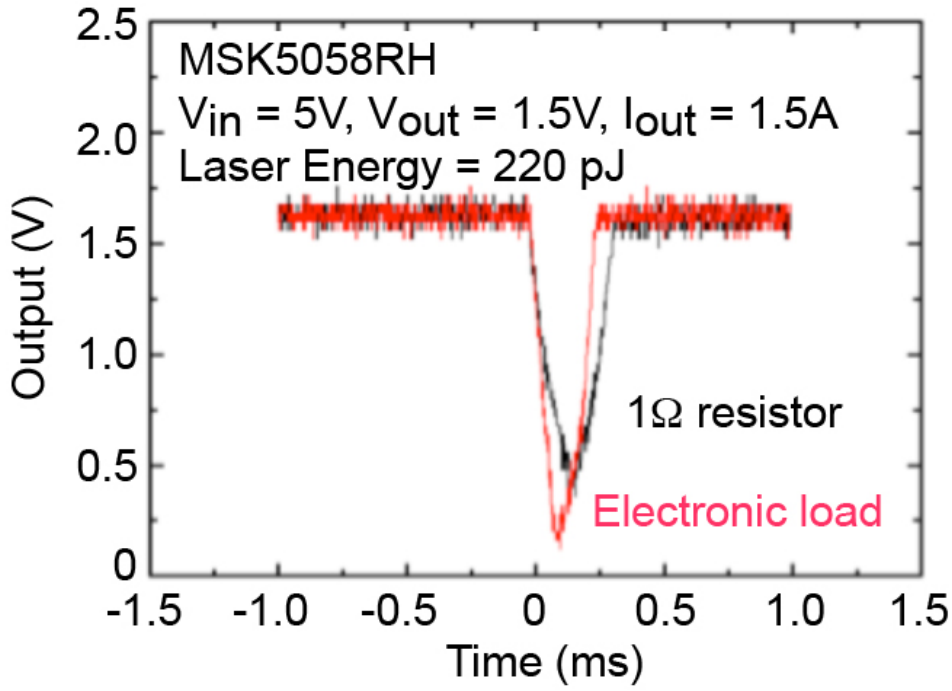


Figure 3.3-1. Impact of loading configuration on SET response during SET assessment. The MSK5058RH SET responses using an electronic load (red) and a passive, physical resistive load (black) are compared. Each provided a load current of 1.5A. All input and bias conditions were static. However, the added inductance of the external load increased the SET by nearly a quarter of a volt.

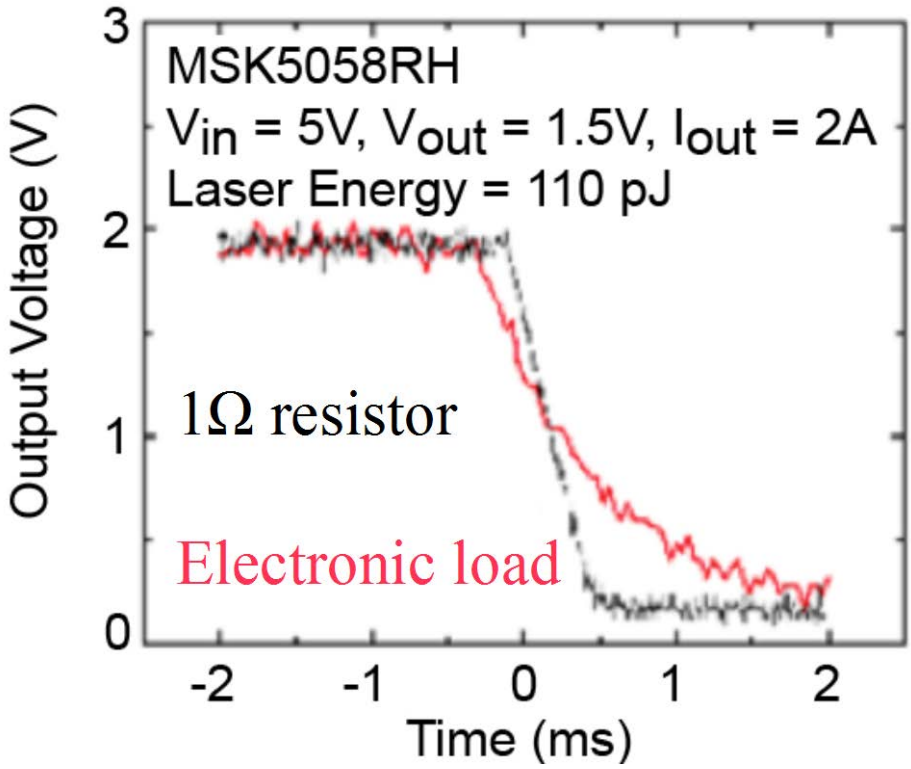


Figure 3.3-2. Pulsed laser-induced SETs for the MSK5059RH operating with V_{in} = 5 V, V_{out} = 1.8 V, I_{out} = 2 A (physical 1 Ω resistor vs. electronic load), laser energy = 110 pJ and laser pulse frequency = 100 Hz. Note the slower slew rate of the physical load.

Another recommendation can be made regarding the board layout and test setup. Test engineers need to pay attention to the use of power and ground planes. If possible, the device under test (DUT) has to be implemented with solid input and output voltage planes and a common ground plane to reduce resistive and inductive losses. Further, it is critical to place the capacitors (typically tantalum SMT capacitors) as close as possible to the input or output of the regulator. When capacitors are attached to the regulator with long, and especially problematic, thin traces the impedance the regulator is subjected to is more greatly influenced by the closest capacitor. Depending on the weight of the trace, tens of mΩ per inch can be added due to trace length. This is especially important when testing an LDO as part of a system or with multiple output capacitors, which is very common in power system architectures. When power and ground planes are executed within the layout, the regulator is subjected to the entire array of capacitance/impedance. Additional parasitics can influence the SET response, as it was the case for the ESR.

3.4 Thermal Shutdown, Temperature, and Combined Effects

In addition to their typical design topology involving a series pass element and a feedback circuit composed of a resistor divider to set the output voltage, a voltage reference and an error amplifier, flight-like linear regulator designs have built-in protection circuits to prevent damage from either excessive load current or operating temperature. This is important when implemented in power system architectures. Regulators are made to operate in "constant voltage mode" despite changes in input voltage or load conditions; however, when the temperature or current limit is surpassed, protection circuits are activated to prevent the device from failing. In particular, crossing the thermal threshold will often result in a shutdown mode (however, some designs will simply limit the current in an attempt to lower the junction temperature).

This type of shutdown can be triggered by a single event. An example of a radiation-induced shutdown event obtained from irradiation on a MSK5059 is illustrated in Figure 3.4-1. While the energy threshold for this event was relatively high, 110 pJ, making this an unlikely event in space, the phenomenon needs to be studied. A generic thermal shutdown circuit typically consists of a temperature sensor (NPN transistor) located near the power transistor. A voltage divider maintains a voltage across that transistor's V_{BE} that will correspond to a turn-on voltage at a given temperature threshold, often around 160°C. Once the turn-on threshold is reached, current is diverted away from the power stage, and the die cooled. Often a logic state is invoked, whereby a power cycle is required to regain regulation.

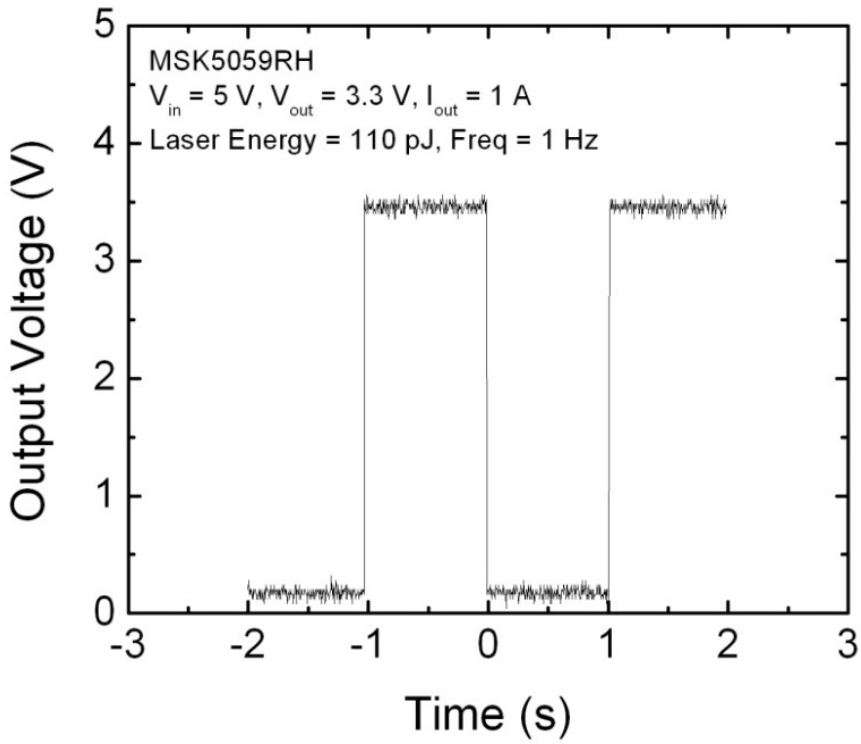


Figure 3.4-1. An illustrated example of a shutdown event provoked by a laser pulse on the MSK5059 regulator.

While further studies are in progress concerning the mechanism observed in Figure 3.4-1, we have empirically observed temperature related shutdown events, i.e., the energy (and thereby LET) threshold for shutdown events decrease as temperature increases. This intuitively makes sense. As the temperature increases a smaller transient across V_{BE} is required to induce a logical shutdown. This agrees with observations made on standard NPN regulators [9].

Finally, we would like to point out that it is also important to maintain an accurate measurement of die temperature during testing. Metal heat sinks (under the package) along with thermal grease often aid in decreasing die temperatures and help eliminate unrelated thermally induced events during radiation testing. As illustrated in Figure3.4-2, a capacitor's ESR is relatively stable at high temperatures, but increases dramatically at low temperatures [21].

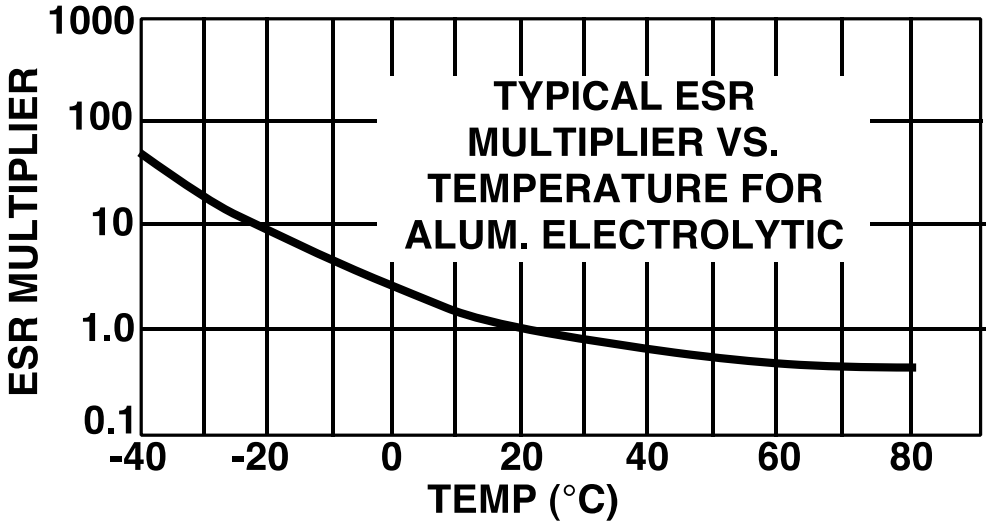


Figure 3.4-2. Typical 100kHz ESR multiplier values. Note the increase at lower temperatures. The multiplier is dependent upon the size of the capacitor and is exacerbated at higher temperature ratings.

4.0 SET TESTING RECOMMENDATIONS

Application requirements drive the design requirements for any given regulator implementation. As such, SET radiation qualification has to be performed in agreement with the specific application parameters the regulator is being targeted for, or at least at a minimum the worst case boundaries if there are multiple implementations. In this work, we demonstrated through simulations and experiments that many elements need to be considered to properly evaluate LDO voltage regulators against SET. Unfortunately, it is often the case that flight qualification tests are not performed correctly. Without consideration of those practical elements, SET testing lead to inadequate data or inconclusive interpretation. As a result, here is our recommended testing approach for SET testing of LDO linear regulators:

1. We recommend adequately measuring the ESR values of the output capacitor before SET testing and use a value that is close to the flight application across application temperature ranges. We have found that bounding the ESR values for the selected capacitor type is most appropriate, i.e., always test to the worst-case ESR value of the application-selected capacitor. If that is unknown, test to the worst case of the regulator datasheet. It is also important to examine and quantify all of the downstream capacitance. This exercise will often not affect the overall output capacitance value, but may affect the ESR (i.e., parallel resistance). Manufacturers tend to provide a range of values of ESR in the datasheet for which the LDO regulator is stable. However, as we demonstrated in the simulation and experimental observations, minimum change in ESR can cause quite a bit of variation in SET responses, even within the manufacturer's specifications. This becomes more relevant as more aggressively scaled digital components are considered for flight applications and have tighter transient input requirements.
2. We recommend that both output loads and capacitors be placed as close to the regulator's output as possible. Further, it is important to design the DUT board with input and output planes rather than traces. If that is not feasible, input power, output, and ground should be designed to have large, isolated traces.
3. We recommend performing full stability measurements for all test configurations and conditions prior to irradiation. At a minimum, turn-on, turn-off, and switching load characterizations should be performed. Those measurements are representative of loop stability. Figure 4.0-1 shows an example of an ESR within the manufacturer's specifications, yet still exhibits unacceptable oscillatory behavior during turn-on. Oscillations such as this could affect downstream electronics, e.g., field-programmable gate arrays (FPGAs) with stringent voltage requirements. While we have only observed this effect with simulations, being on the edge of stability could conceivably change the SET response of certain regulators.

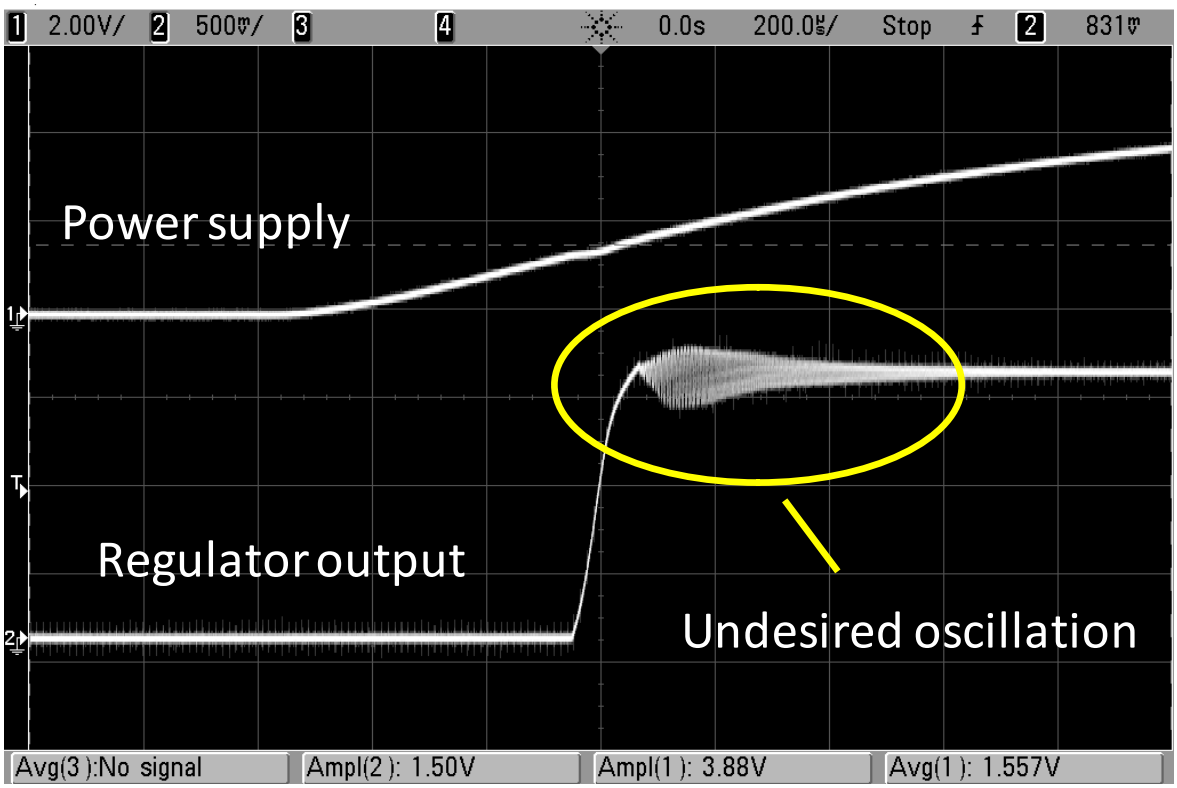


Figure 4.0-1. The 1.5 V MSK5920 turn-on curve with minimum load. Channel 1 is the input power supply and channel 2 is the regulator output. The output capacitor was a 220 µF with a measured ESR of 40 mΩ. A 0.1 Ω series resistor was inserted in series with the tantalum output capacitor. Note the damped ringing of few hundred mV of amplitude and several hundreds of µs in duration at the regulator output.

4. Once the pre-irradiation measurements have been completed and it is certain the DUT as implemented is stable, the DUT should be investigated for SET either testing precisely to the application, or the worst-case conditions. We have found the worst-case conditions for these regulators to be the following:
    a. Maximum ESR within the specified ESR limits
    b. Maximum output voltage
    c. Maximum load current
    d. Test temperature.

Then, based on the heavy ion data, a safe operating area based on acceptable peak amplitude and duration [19–20] can be determined and event rate calculated, depending on the mission requirements. Finally, when reporting upon the test results, document all operating, bias, and load conditions, including measured ESR and die temperature.

5.0 CONCLUSION

This paper has shown a few examples of how various elements such as loop stability, input voltages, load conditions, and ESR values for fixed values of output capacitor can considerably affect the SET responses of linear regulators. Based on experimental and simulation results, we provided a set of practical recommendations that have to be considered prior to and during SET testing for adequate part qualification based on both acquired data and observed effects.

We have shown the effect of ESR on LDO regulator SETs through the use of pulsed laser testing. Included in the test report is our recommendation to measure ESR prior to testing. These additional steps will ensure testing of stable circuits and allow users of the data to determine applicability of the test results to a given application.

While a direct comparison between data taken at the laser facilities and broad beam results would require painstaking analysis and a certain level of interpretation, our results agreed with observed broad beam effects (SET shapes and shutdown modes). We would also like to point out that the community's test standards (ASTM 1192-00 and JESD89) are far too general to augment with the details found in this paper. However, the authors do plan on generating a NASA test guideline in the future.

Finally, here is a list of key points that were extracted for this study:

- The impact of ESR is worse at low load (<100 mA)
- Higher output voltage configuration does not lead to higher transient amplitude
- Higher output voltage configuration leads to transient that are longer in duration
- High load configuration leads to transients that are higher in amplitude and shorter in duration
- Output capacitor value impacts both negative and positive transient duration.

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