National Aeronautics and Space Administration

Radiation Tests of Highly Scaled, High-Density, Commercial, Nonvolatile NAND Flash Memories—Update 2012

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1.0 INTRODUCTION

The space radiation environment poses a certain risk to all electronic components on Earth-orbiting and planetary mission spacecraft. In recent years, there has been increased interest in the use of high-density, commercial, nonvolatile flash memories in space because of ever-increasing data volumes and strict power requirements. They are used in a wide variety of spacecraft subsystems. At one end of the spectrum, flash memories are used to store small amounts of mission-critical data such as boot code or configuration files and, at the other end, they are used to construct multi-gigabyte data recorders that record mission science data.

Information on floating gates (FGs) is embedded by the presence or absence of trapped charge on an electrically isolated conductor. Nevertheless, flash memories are susceptible to upset and degradation from radiation, and more information is needed on their radiation response before they can be used extensively in space. Flash memories have been the subject of several ionizing radiation effects studies in recent years, regarding both total ionizing dose (TID) [1–4] and single-event effect (SEE) [4–8] experiments. In both cases, the complex control circuitry has been demonstrated to be the most vulnerable part of commercial devices. However, the degradation of the threshold voltage (V_{TH}) of a single cell in the FG array after exposure to ionizing radiation is a non-negligible issue, as it may lead to the corruption of the stored data. The functionality of flash memories begins to fail as TID accumulates during a space mission. Older generations of flash memories functionally failed during erase/write modes at approximately 10 krad(Si) [1]. In addition, different functional failures have been detected in some commercial devices depending on the mode of operation during radiation exposure, including reduced speed, higher leakage currents, increased standby power supply currents, variation in timing parameters, and possible loss of device functionality [7–9]. In addition, direct strikes from galactic cosmic rays (GCRs) and protons from solar flares can upset internal circuitry associated with structures such as the charge pump, state buffers, cache memory, or internal microcontrollers, as well as FG arrays. These upsets can result in incorrect read/write operation or even cause the device not to function until it is power-cycled, reinitializing all the internal circuitry.

At present, the industry trend is to continue with feature-size scaling. The impact of single-event upset (SEU) on highly scaled memories because of their shrinking dimensions and increasing densities has become a significant reliability concern. In advanced flash memories, one would expect the SEU cross section per bit to become smaller with shrinking feature sizes [2]. However, the SEU cross section for the FG arrays is becoming comparable to, if not larger, than that of the control logic. The SEU cross section can be dominated by either the FG array or the control logic, depending on the particular application [5]. In addition, because of thinner oxide layers, the total dose response is improved, although the tunnel oxides have not been scaled as aggressively as other oxides because of concerns about retention [2]. The last several generations of NAND flash memories have had only 7–10 nm tunnel oxides.

High-density, commercial, nonvolatile flash memories with NAND architecture are now available from several manufacturers. This report examines SEE and TID response in single-level cell (SLC) 32-Gb, multi-level cell (MLC) 64-Gb, and triple-level cell (TLC) 64-Gb NAND flash memories manufactured by Micron Technology with a feature size of 25 nm.

2.0 EXPERIMENTAL PROCEDURE

2.1 Device Descriptions

The part number, date code, and process feature size of the parts studied in this report are summarized in Table 2.1-1. In general, a NAND structure consists of 32 cells. SLC NAND stores two binary states (either a binary 1 or a binary 0) in a single cell, whereas MLC NAND can store four states (00, 01, 10, and 11) and TLC NAND can store eight states (111, 110, 101, 011, 100, 010, 001, and 000). To recognize the four states or eight states, special circuitry must be added to allow the amount of charge stored in the FG to be controlled within narrow limits during writing, and also to detect the different amounts of charge during reading. The programming circuits must deliver precise amounts of electrons to the FG, and the sense amps must distinguish between the four or eight small V_{TH} regimes. There is considerably more design margin with the SLC device, which leads to greater radiation robustness, reliability, and endurance compared to the MLC and TLC devices.

Table 2.1-1. Micron Technology NAND flash memories under study.

Part Number	Density (Gb)	Date Code	Feature Size (nm)
MT29F32G08ABAAA	32 SLC	1106	25
MT29F64G08CBAAA	64 MLC	1116	25
MT29F128G08EFAAAWP	2 x 64 TLC	1150	25

2.2 Test Facility and Procedure

2.2.1 SEE Measurements

Heavy ion SEU measurements were performed at the cyclotron facility in Texas A&M University (TAMU). This facility provides a variety of ion beams over a range of energies for testing. Table 2.2.1-1 lists the ion beams used in the measurements at TAMU. Linear energy transfer (LET) and range values are for normal incident ions. Test boards containing the device under test (DUT) were mounted to the facility test frame. Tests were done in air. The beam flux ranged from 2×10^2 to 5×10^5 ions/cm^{2}sec. These measurements complement our previous measurements at the cyclotron facility at Jyväskylä, Finland (RADEF).

The DUTs were etched to remove the plastic packaging and expose them to the ion beam. Removal of the plastic packaging did not affect the DUTs' parameters, such as standby current. The SEE data for NAND flash memories at both facilities were taken using a commercial memory tester called the JD Instruments (JDI) tester. The JDI algorithmic test vector (ATV) tester uses both custom application-specific integrated circuit (ASIC) and field-programmable gate array (FPGA) hardware with a built-in graphical interface. The JDI tester is fully capable of performing high-speed testing on memory systems using algorithmically generated test vectors. The maximum operating frequency of the JDI is a 50 MHz cycle time. The operating frequency during the measurements was 17 MHz. The DUT was biased only at 3.6 V (3.3 V nominal power supply, plus 10%) during irradiation. No measurements at 3.3 V or 3.0 V were performed. All the measurements were performed at room temperature.

All tests were conducted by first loading the DUT with an all "0" pattern and then verifying the pattern by reading it back from the device. The complete Read cycle for the Micron Technology 32-Gb SLC devices is around 20 minutes. During irradiation, the DUT was dynamically operated in Read mode. After irradiation and the final Read cycle , the device's power was cycled and the DUT was reread, checked for errors, and logged. This method ensured that the errors were from bit upsets in the FGs. Then the pattern was erased and rewritten to make the device ready for the next run.

Table 2.2.1-1. Ion beams used in SEE measurements at TAMU.

Ion	LET (MeV-cm²/mg)	Range (μm)
^{4}He	0.1	1386
^{14}N	1.3	199
^{40}Ar	8.3	123
^{128}Xe	51.8	120
^{197}Au	85.4	118

2.2.2 TID Measurements

Total dose measurements were done at room temperature using the Jet Propulsion Laboratory (JPL) cobalt-60 (Co-60) facility at a dose rate of 50 rad(Si) per second. For all measurements, the DUTs were under static bias (3.6 V) during irradiation; however, they were not actively exercised as this corresponds to the actual operating condition of an extended space mission where the devices are being exposed to radiation.

The TID data were taken using the JDI tester. All tests were conducted by first loading the DUT with an all "0" pattern and then verifying the pattern by reading it back from the device. In all measurements, the standby currents were measured for each dose increment. The study also counted bit errors, which were produced because of the shift in the threshold voltage. TID measurements were performed at room temperature in the following two modes:

1. Refresh mode (erase/program/read):
   a. Erase, write, and read to validate programmed numbers.
   b. Irradiate DUTs with static bias.
   c. Read numbers to ensure data retention.
   d. Repeat steps a to c for each radiation increment.
2. No Refresh mode (read only):
   a. Erase, write, and read to validate programmed numbers.
   b. Irradiate DUTs with static bias.
   c. Read numbers to ensure data retention.
   d. Repeat steps b to c for each radiation increment.

3.0 SEE TEST RESULTS

Two types of radiation-induced events were measured while performing read operations during irradiation: SEU and single-event functional interrupt (SEFI). Three samples were measured.

3.1 SEUs

During SEU measurements, the beam flux was set to approximately 2×10^2 to 5×10^5 ions/cm^2-sec and the DUT was irradiated for 5–15 seconds in order to reduce the probability of SEFIs. The measurements of the three samples showed excellent agreement, indicating that part-to-part variations were not an issue. Therefore, cross sections from three samples of the same device were averaged together in the SEE data reported. Measurements were performed with heavy ions having an LET range of 0.1–60 MeV-cm^2/mg at normal incidence and horizontal rotation of 60 degrees (horizontal rotation is defined as a rotation of the device about the vertical axis of the device).

3.1.1 32-Gb SLC

Figure 3.1.1-1 shows the average SEU cross section for three samples of Micron Technology 32 Gb SLC devices. The measurements of the three samples showed excellent agreement, indicating that part-to-part variations were not an issue. The saturated FG SEU cross section per bit is on the order of 1×10^{-10} cm^2/bit. The error bars are smaller than the size of the plotting symbols. Only data measured at normal incidence are shown in Figure 3.1.1-1. Additional data at horizontal rotation of 60 degrees were obtained but not included in Figure 3.1.1-1. These data suggest that SEU susceptibility of the FGs follows the cosine law, but there is some uncertainty because an angular measurement was done for only one ion species (Ar). For comparison purposes, Figure 3.1.1-1 shows the FG SEU cross section for the Micron Technology 1, 4, and 8 Gb SLC NAND flash memories. All measurements were performed at normal incidence. The error bars are smaller than the size of the plotting symbols. The SEU cross section presented in Figure 3.1.1-1covers feature sizes from 120–25 nm. The threshold LET doesn't change with scaling. At LETs below 8 MeV, there are no noticeable differences between SEUs and threshold LETs for the 1, 4, 8, and 32 Gb devices. In Figure 3.1.1-2, we display the cross section versus feature size for Micron Technology 1, 4, 8, and 32 Gb for LETs above 8 MeV-cm^2/mg. Note that similar to low LET data points (LET below 8 MeV-cm^2/mg) there are no noticeable differences in SEUs in the range of 120–72 nm feature size; however, there is a reduction in the FG SEU cross section at 50 nm feature size and an increase at 25 nm. This indicates that the scaling effect is effective below a certain feature size, in this case below 72 nm.

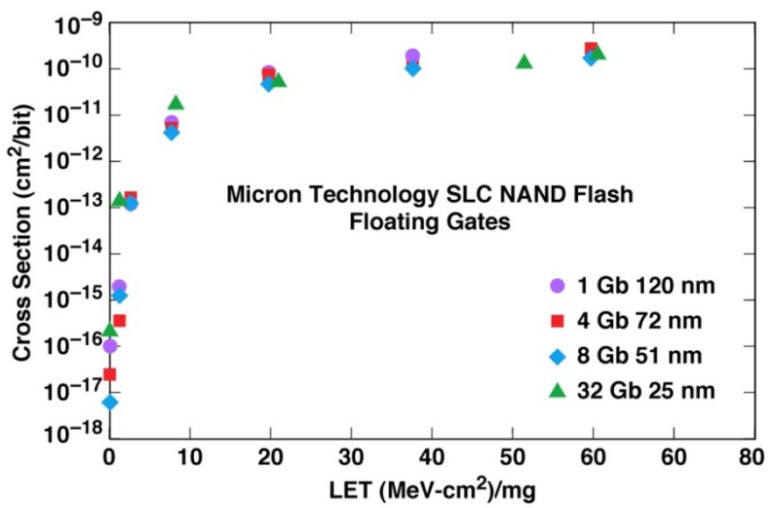

Figure 3.1.1-1. FG SEU cross sections for Micron Technology SLC NAND flash memories. The error bars are smaller than the size of the plotting symbols.

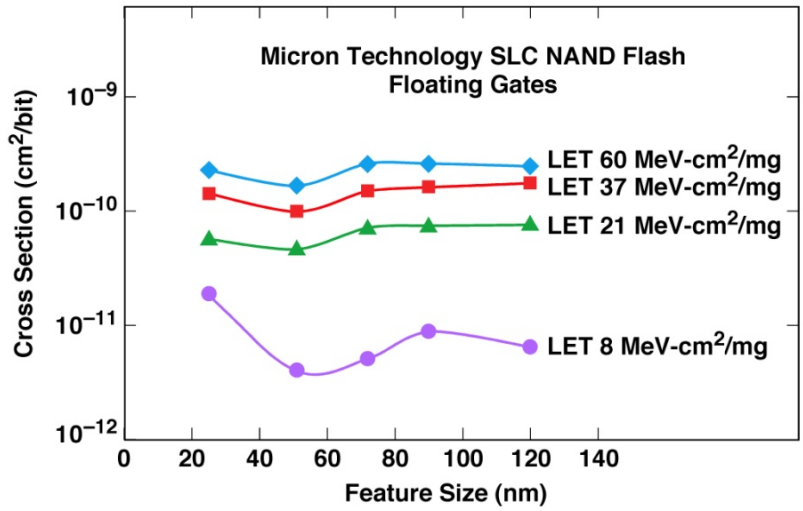

Figure 3.1.1-2. FG SEU cross sections for Micron Technology SLC NAND flash memories verses feature size.

3.1.2 64-Gb MLC

Figure 3.1.2-1 shows the average FG SEU cross section for three samples of Micron Technology 64 Gb MLC NAND flash memory. The saturated FG SEU cross section per bit is on the order of 3×10^{-10} cm^2/bit. The error bars are smaller than the size of the plotting symbols. For comparison purposes, Figure 3.1.2-1 also shows the FG SEU cross section for Micron Technology 32 Gb MLC devices. This comparison does not support scaling of cross section in the region of 32–25 nm.

As was mentioned in Section 2, there is a considerably more design margin with SLC, which leads to greater radiation robustness, reliability, and endurance compared to MLC. The differences in SEU susceptibility between SLC and MLC devices are clearly noticeable by comparison with data presented in Figure 3.1.2-2. The SLC 32 Gb is less susceptible than is the MLC 32 Gb part.

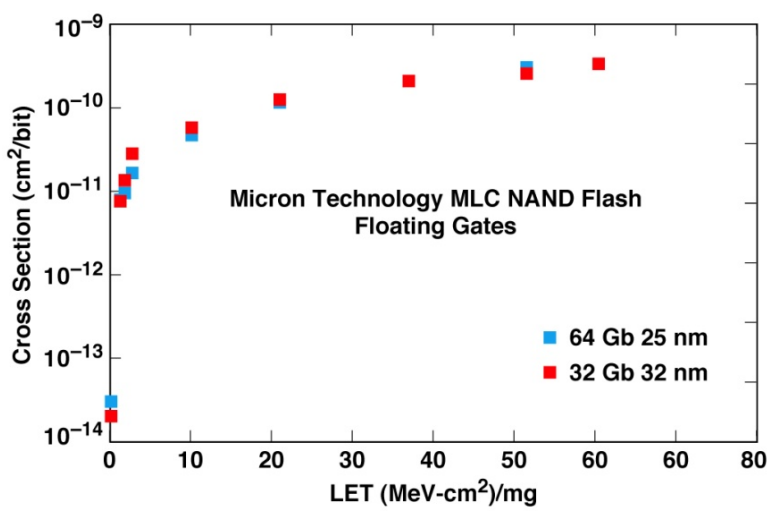

Figure 3.1.2-1. FG SEU cross sections for Micron Technology 64 Gb MLC NAND flash memory. FG SEU cross section for Micron Technology 32 Gb MLC is shown for comparison. The error bars are smaller than the size of the plotting symbols.

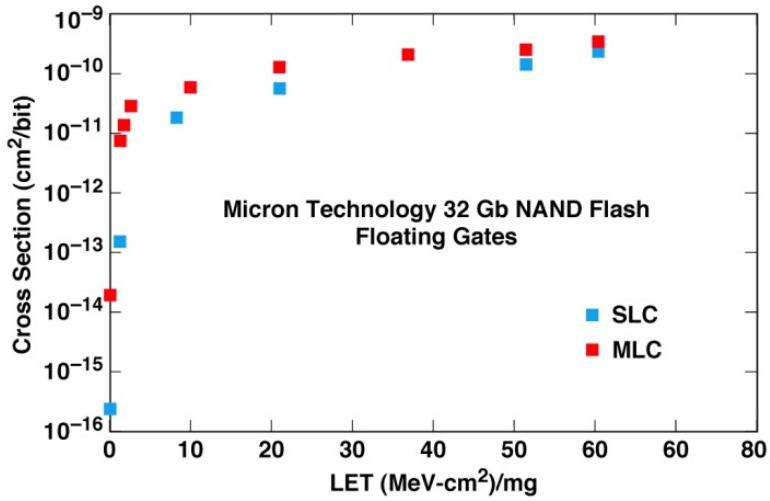

Figure 3.1.2-2. Comparison of FG SEU cross sections for Micron Technology 32 Gb SLC and MLC NAND flash memories. The error bars are smaller than the size of the plotting symbols.

3.1.3 64-Gb TLC

Figure 3.1.3-1 shows the average FG SEU cross section for three samples of Micron Technology 64-Gb TLC NAND flash memory. The saturated FG SEU cross section per bit is on order of 9×10^{-10} cm^2/bit. The error bars are smaller than the size of the plotting symbols.

As was mentioned in Section 2, there is a considerably more design margin with SLC, which leads to greater radiation robustness, reliability, and endurance compared to multiple bit per cell devices. The differences in SEU susceptibility among SLC, MLC, and TLC devices are clearly noticeable by comparison of data presented in Figure 3.1.3-2. The SLC 32-Gb is less susceptible than is the MLC 32-Gb part and the MLC 32-Gb is less susceptible than is the TLC 64-Gb part.

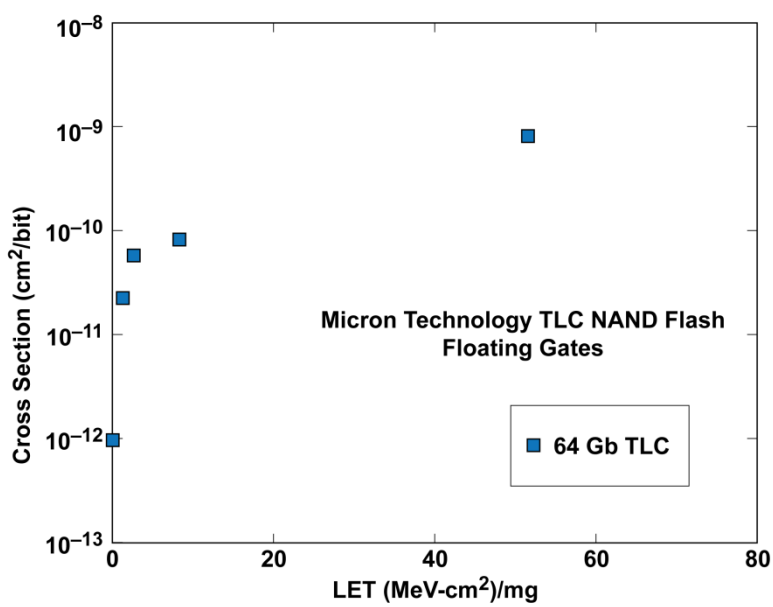

Figure 3.1.3-1. FG SEU cross sections for Micron Technology 64 Gb TLC NAND flash memory. The error bars are smaller than the size of the plotting symbols.

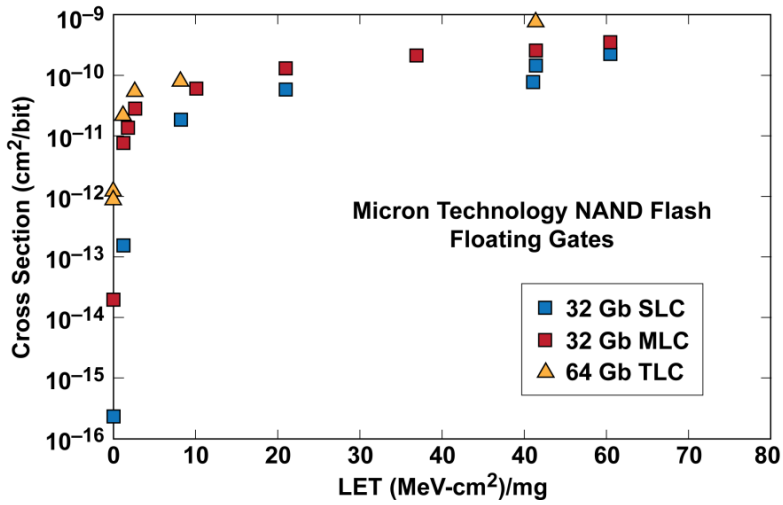

Figure 3.1.3-2. Comparison of FG SEU cross sections for Micron Technology 32-Gb SLC, 64-Gb MLC and TLC NAND flash memories. The error bars are smaller than the size of the plotting symbols.

3.2 SEFIs

3.2.1 32-Gb SLC

During SEFI measurements, the beam flux was set to approximately 5×10^3 ions/cm^2 per second and the DUT was irradiated until occurrence of SEFI. After occurrence of SEFI, irradiation was stopped. For each sample, three SEFIs were collected. Figure 3.2.1-1 shows the SEFI cross section for the Micron Technology 32-Gb SLC flash memory. The error bars are approximately 2 sigma (95%) and result from Poisson statistics. SEFIs were observed at a LET of 10.1 MeV-cm^2/mg, but no SEFIs were observed at a LET of 1.8 MeV-cm^2/mg. The SEFI LET threshold is between 1.8 and 10.1 MeV-cm^2/mg.

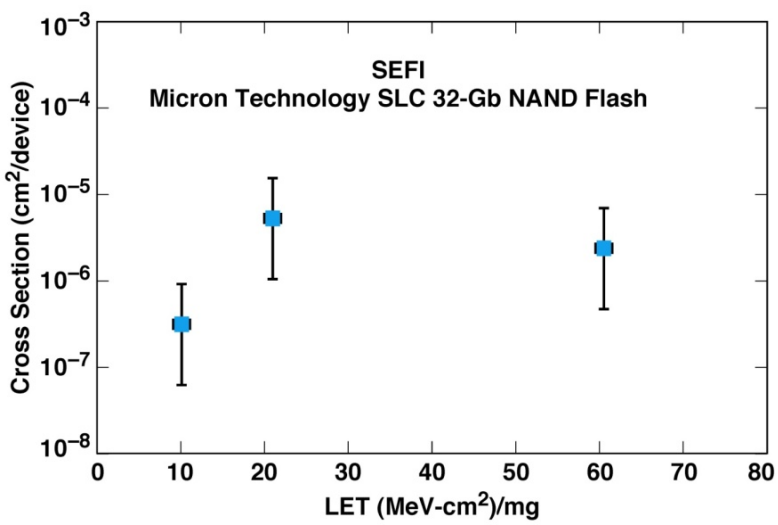

Figure 3.2.1-1. SEFI cross section for Micron Technology 32-Gb SLC NAND flash memory. Measurements were performed at RADEF.

3.2.2 64-Gb MLC

Figure 3.2.2-1 shows the SEFI cross section for the Micron Technology 64-Gb MLC flash memory. The error bars are approximately 2 sigma (95%) and result from Poisson statistics. The same SEFIs, as those seen with the 32-Gb SLC parts, were observed at a LET of 10.1 MeV-cm^2/mg, but no SEFIs were observed at a LET of 1.8 MeV-cm^2/mg. The SEFI LET_{th} is between 1.8 and 10.1 MeV-cm^2/mg.

Figure 3.2.2-2 compares the SEFI cross sections for the Micron Technology 32-Gb SLC and MLC NAND flash memories. Similar to FG SEU results, the SLC parts are less sensitive to SEFIs compared to MLC parts.

The analysis of SEFIs was complicated because the signature, recovery mechanism, and consequence to the device operation varied greatly, depending on exactly how the device functionality was altered. Typical SEFI events resulted in a large number of errors while trying to read the device. Some events will selfrecover once the device is reread. Other SEFIs require a power cycle and the part to be reinitialized to return to normal operations.

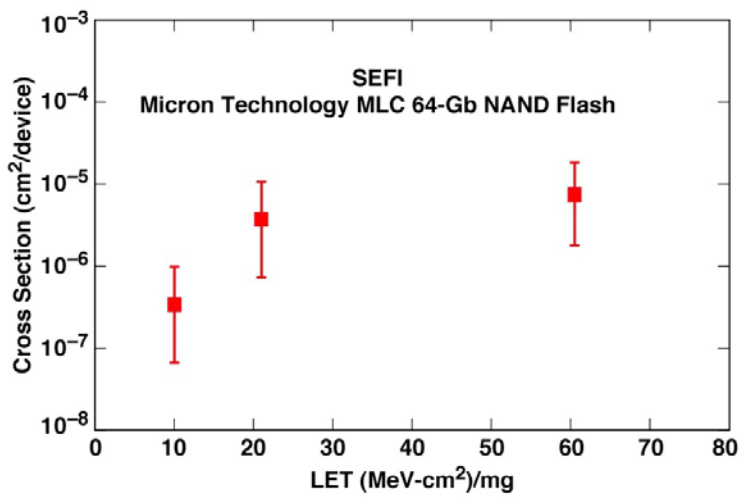

Figure 3.2.2-1. SEFI cross section for Micron Technology 64-Gb MLC NAND flash memory. Measurements were performed at RADEF.

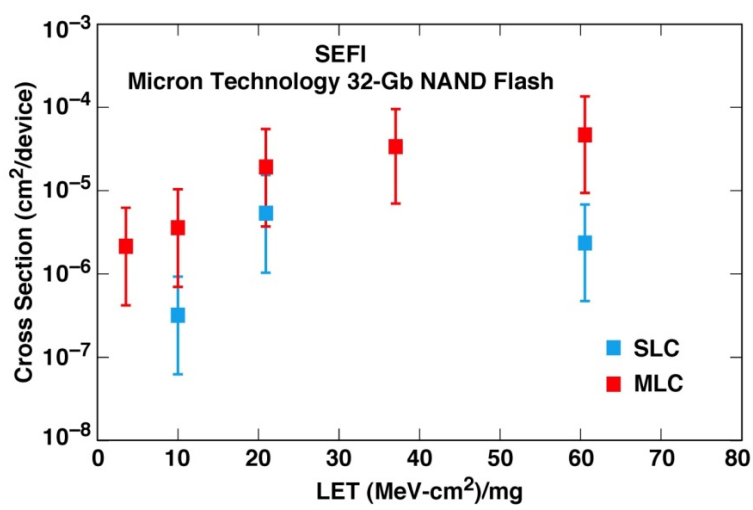

Figure 3.2.2-2. Comparison of SEFI cross sections for Micron Technology 32-Gb SLC and 64-Gb MLC NAND flash memories.

4.0 TID TEST RESULTS

TID measurements were performed in Refresh and No Refresh mode. Three samples were measured. Parts were biased at 3.6 V and irradiated with a rate of 50 rad per second using JPL's Co-60 source.

4.1 Refresh Mode

4.1.1 32-Gb SLC

In Refresh mode, two Micron Technology 32-Gb SLC parts were irradiated at 5, 15, 35, 40, and 50 krad(Si). One sample failed post 40 krad(Si) erase; the other sample failed erase function post 50 krad(Si). Figure 4.1.1-1 displays the average standby current for Micron Technology 32-Gb SLC parts.

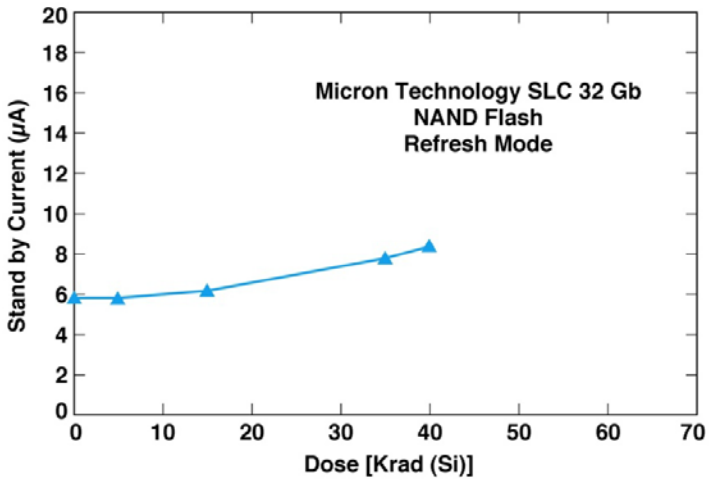

Figure 4.1.1-1. Standby current results versus dose for Micron Technology 32-Gb SLC NAND flash memory in Refresh mode.

4.1.2 64-Gb MLC

Two samples of the Micron Technology 64-Gb MLC were irradiated up to 20 krad(Si) in Refresh mode. Figure 4.1.2-1 displays the percentage of erroneous bits versus dose for two samples of Micron Technology MLC 64-Gb parts in Refresh mode. Figure 4.1.2-2 shows the average standby current for the two samples of Micron Technology MLC 64-Gb in Refresh mode.

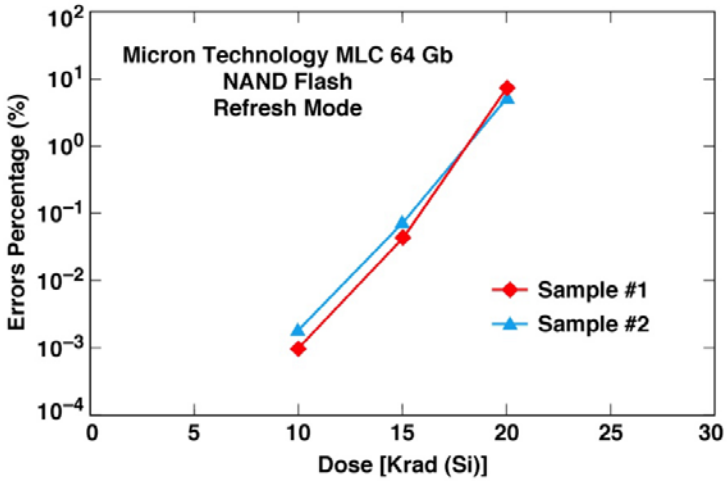

Figure 4.1.2-1. Percentage of bit errors versus dose for Micron Technology 64-Gb MLC NAND flash memories in Refresh mode.

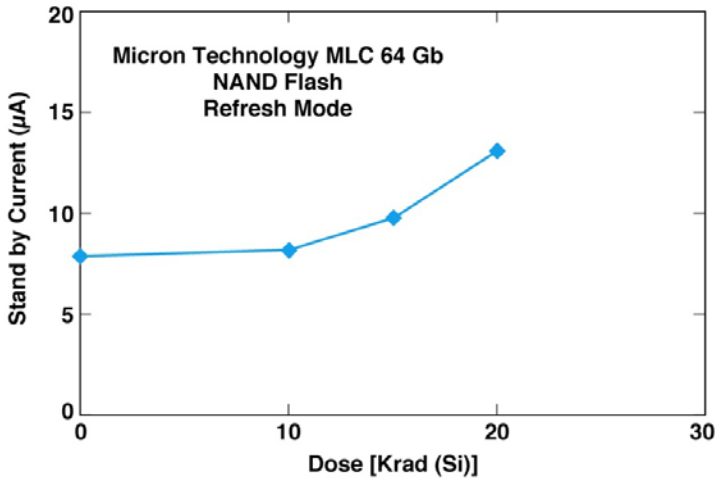

Figure 4.1.2-2. Standby current results versus dose for Micron Technology 64-Gb MLC NAND flash memory in Refresh mode.

4.2 No Refresh Mode

4.2.1 32-Gb SLC

In No Refresh mode, the DUTs were subjected only to Read mode after irradiation. Three samples of the Micron Technology 32-Gb SLC were irradiated up to 75 krad(Si). Samples failed at 55, 75, and 70 krad. Table 4.2.1-1 summarizes the bit error TID results for the three samples. Figure 4.2.1-1 displays the percentage of erroneous bits versus dose for the three samples.

Figure 4.2.1-1 shows the rapid buildup of bit errors up to approximately 50–65 krad(Si) for the 32-Gb DUTs that had been programmed to all "0" prior to irradiation. Two samples failed post irradiation erase function at 55 and 70 krad(Si). One sample was functional up to 75 krad(Si). For this sample, at approximately 50 krad(Si), a large number of the FGs are read as "1." The remaining cells initially programmed to "0" are partially discharged but still read as "0." After approximately 50 krad(Si), the erased cells gradually change to "0" and error percentage reduces. This effect can be attributed to a reduction in the voltage from the charge pump during read operation because of TID damage [10]. In the NAND architecture, a FG cell is read by applying 0 V to its gate and biasing all the other cells that belong to the same series of 32 FGs to a voltage high enough to guarantee that both erased and programmed cells are turned on. This voltage is generated by a charge pump circuit during read operation. If the voltage

Table 4.2.1-1. Summary of bit–error TID results for Micron Technology 32-Gb SLC NAND flash memory in No Refresh mode showing separate samples.

TID (Krad)	Errors (Sample #1)	Errors (Sample #2)	Errors (Sample #3)
0	0	0	0
5	6	34	23
15	20	103	84
25	151	289	296
50	171,774	6,379	905
55	Failed at 55 krad(Si)	4,533	7,987
60	–	3,940	79,994
65	–	2,813	465,817
70	–	26	Failed at 70 krad(Si)
75	–	Failed at 75 krad(Si)	–

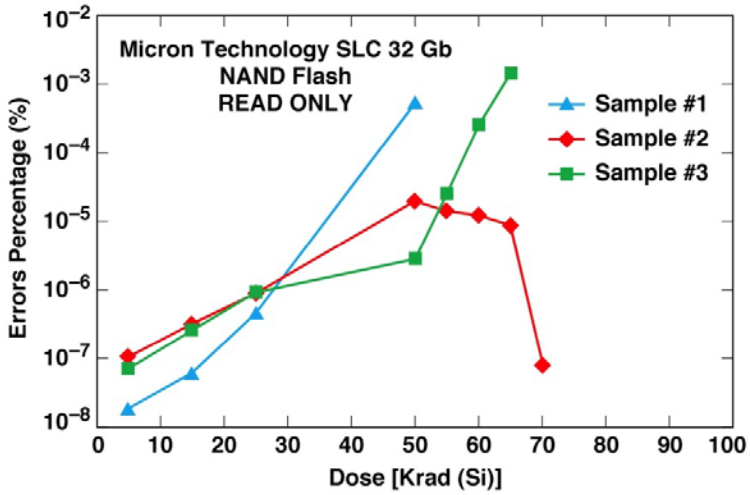

Figure 4.2.1-1. Percentage of bit errors versus dose for Micron Technology 32-Gb SLC NAND flash memories in No Refresh mode.

provided by this element is lower than the design limit, some of the cells in the string will be read as programmed ("0"), regardless of their actual status. This is the likely cause of the drop in apparent number of errors around 50 krad(Si) in Figure 4.2.1-1. Similar behavior has been reported in the x-ray TID measurements of STMicro 1-Gb SLC NAND flash memory [10] and Co-60 TID measurements of Micron Technology 32-Gb MLC NAND flash memory [9].

The standby current measurements for 32-Gb SLC samples used in No Refresh mode measurements are summarized in Table 4.2.1-2, and the standby current versus the dose for No Refresh mode is shown in Figure 4.2.1-2.

Annealing measurements on the Micron Technology 32-Gb SLC parts were performed at room temperature. Annealing began after 45 krad(Si) level and continued for 155 hours while the DUT was biased at 3.6 V. Figure 4.2.1-3 displays bit error measurements versus time for the Micron Technology 32-Gb SLC NAND flash memory. The figure shows the FG error rate percentages normalized to the number of errors at 45 krad(Si) level at the beginning of annealing measurements. The results are rather surprising. Contrary to the previous published annealing measurements [11], these results show a slow annealing.

For comparison purposes, in Figure 4.2.1-4 we show the percentage of bit errors versus dose for the Micron Technology 1, 4, 8, and 32 Gb SLC NAND flash memories. The measurements were performed in No Refresh mode (read only). For a particular TID dose level, the number of errors scales with feature size.

Table 4.2.1-2. Summary of standby current versus dose for Micron Technology 32-Gb SLC NAND flash memory in No Refresh mode.

TID (Krad)	Standby Current (μA) (Sample #1)	Standby Current (μA) (Sample #2)	Standby Current (μA) (Sample #3)
0	5.69	5.26	5.47
5	5.83	5.41	5.24
15	6.08	5.76	5.59
25	7.02	6.35	6.11
50	21.41	22.33	6.88
55	–	29.74	8.07
60	–	39.03	10.07
65	–	52.02	13.16
70	–	66.66	17.80

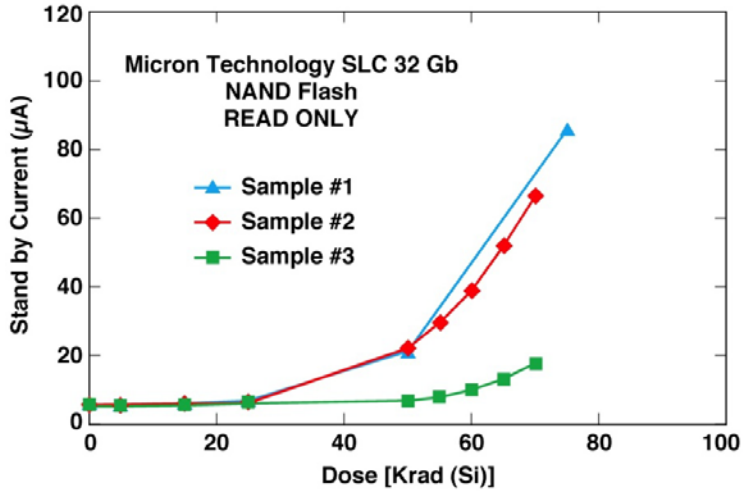

Figure 4.2.1-2. Standby current results versus dose for Micron Technology 32-Gb SLC NAND flash memory in No Refresh mode.

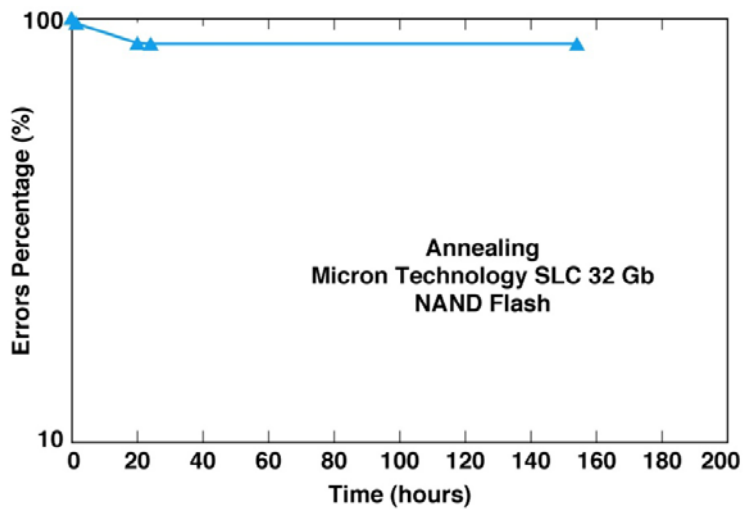

Figure 4.2.1-3. Results of annealing measurements of the Micron Technology 32-Gb SLC flash memory. Data are normalized to number of error bits at 45 krad(Si) at the start of annealing measurements.

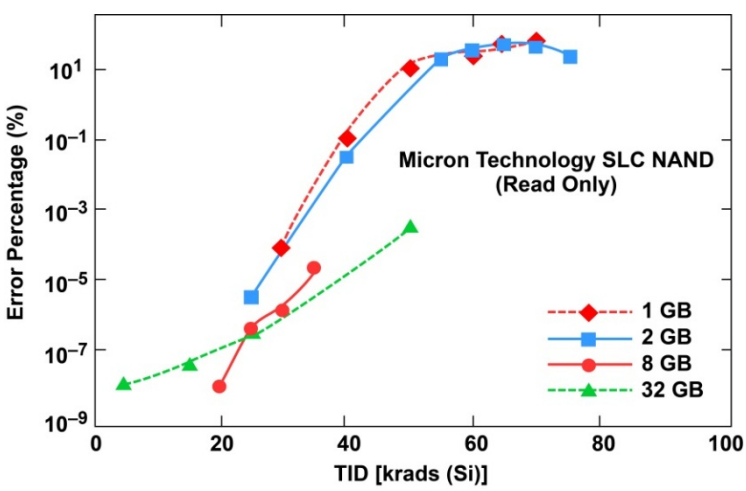

Figure 4.2.1-4. Percentage of data errors versus dose for Micron Technology 1, 2, 8 & 32Gb SLC NAND flash memory.

4.2.2 64-Gb MLC

For the 64-Gb MLC parts, the TID measurements were performed on three samples up to 50 krad(Si) in No Refresh mode with an irradiation rate of 50 rad per seconds. Table 4.2.2-1 summarizes the bit–error TID results for three samples of the Micron Technology 64-Gb MLC parts. Figure 4.2.2-1 displays the percentage of erroneous bits versus the dose for the three samples. There is excellent agreement among the three samples.

Table 4.2.2-2 summarizes the standby current measurements for 64-Gb MLC samples used in No Refresh mode. Figure 4.2.2-2 displays the standby current versus the dose for No Refresh modes. There is excellent agreement between three samples.

Annealing measurements on the Micron Technology 64-Gb MLC parts were performed at room temperature. Annealing begun after 50 krad(Si) level and continued for 100 hours while the DUT was biased. Figure 4.2.2-3 shows the percentage of error in bit rates normalized to the number of errors at 50 krad(Si) level at the beginning of annealing measurements for two samples.

Table 4.2.2-1. Summary of bit–error TID results for Micron Technology 64-Gb MLC NAND flash memory in No Refresh mode showing separate samples.

TID (Krad)	Errors (Sample #1)	Errors (Sample #2)	Errors (Sample #3)
0	0	0	0
5	3,220,222	1,908,402	5,971,891
15	2,591,367,027	1,900,091,077	2,477,828,990
25	6,155,474,245	8,086,873,453	10,310,452,117
50	53,841,999,974	54,326,351,685	48,369,368,017

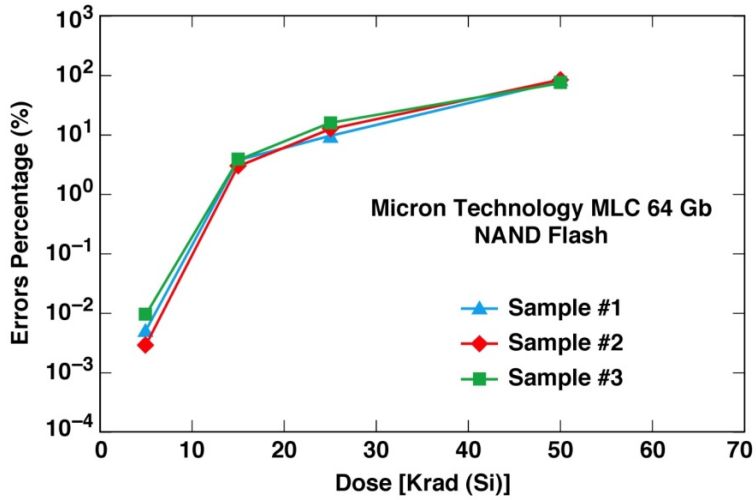

Figure 4.2.2-1. Percentage of bit errors versus dose for Micron Technology 64-Gb MLC NAND flash memories in No Refresh mode.

Table 4.2.2-2. Summary of standby current versus dose for Micron Technology 64-Gb MLC NAND flash memory in No Refresh mode.

TID (Krad)	Standby Current (µA) (Sample #1)	Standby Current (µA) (Sample #2)	Standby Current (µA) (Sample #3)
0	6.14	6.08	5.96
5	6.67	6.53	6.81
15	8.81	8.25	8.07
25	13.62	12.57	11.98
50	106.90	97.94	91.03

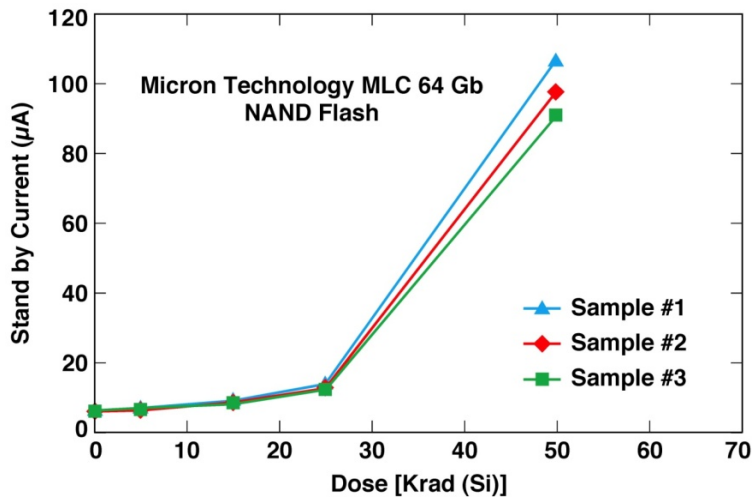

Figure 4.2.2-2. Standby current versus dose for Micron Technology 64-Gb MLC NAND flash memories in No Refresh mode.

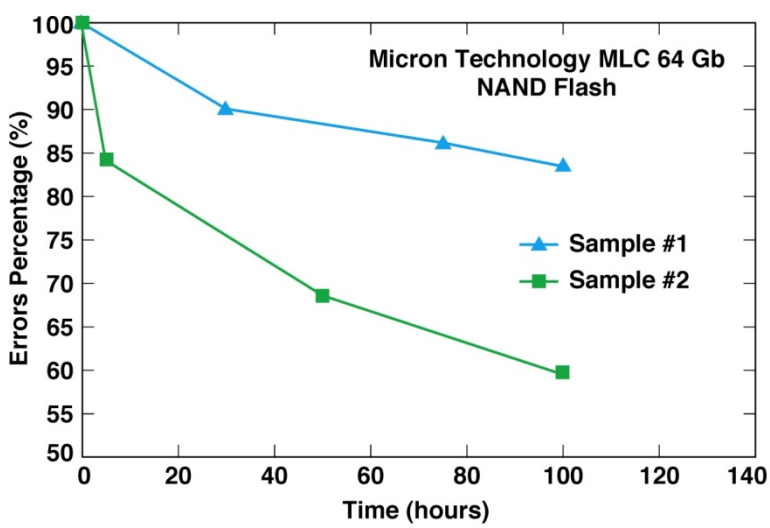

Figure 4.2.2-3. Results of annealing measurements of the Micron Technology 64-Gb MLC flash memory. Data are normalized to number of error bits at 50 krad(Si) at the start of annealing measurements.

5.0 DISCUSSION

In new advanced flash memory technology, the cells are n-channel transistors, with an additional FG that can store electrons. For SLC parts, a "0" or "1" is determined by the V_{TH} of the cell. The V_{TH} can be manipulated by the amount of charge put on the FG of the flash cell. Placing charge on the FG will increase the V_{TH} of the cell. When the V_{TH} is high enough to pass a design value, the cell will be read as programmed. No charge or V_{TH} less than the design value will cause the cell to be sensed as erased. The actual value of the design voltage is confidential and depends on the selected technology and manufacturer. The MLC flash works the same way as SLC flash, except there are three design values. The V_{TH} is used to manipulate the state of the flash. Once again, the amount of charge on the FG is what determines the V_{TH}. Co-60 irradiation of flash memories leads to charge injection into FG, charge trapping in the oxides, and charge loss from the programmed FGs. The charge trapping component is typically small because of the thin oxide thickness of the highly scaled FGs. The neutralization of trapped charges may arise due to annealing effects after exposure to Co-60.

As discussed in [12–13], there are two main mechanisms causing charge loss from programmed FGs. The first one is the charge generation/recombination in the oxides surrounding the FGs. The second contributor is the emission of electrons stored in the FGs after having gained energy from impinging radiation. The photoemission of electrons from the programmed FGs strongly contributes to charge loss at high doses. It has been discussed in [12] that the devices with smaller feature sizes experience a smaller photoemission current during irradiation. Because of this, advanced devices with smaller feature size are less sensitive to TID effects than the older generation of flash memories with larger feature size.

In the heavy ion tests, all the single bit errors in the FGs are zero-to-one errors. Upset in flash memories also occurred in the control circuitry, causing complex errors at the block level as well as address errors [1, 4–5]. When a single high energy ion strikes an FG, it will leave a highly dense track of electrons and holes around it. Therefore, carriers are denser and recombination is more efficient with high LET ions. In other words, the mechanisms of charge trapping in the oxide and charge loss from the programmed FGs are different from the above described for Co-60 irradiation. Because of the scaling and reduced feature sizes, the advanced high-density memories have smaller area capacitors, and hence lower critical charges. The critical charge is device-dependent and can vary from 0.005 to about 2.5 pC. In general, for unhardened devices, the critical charge decreases with reduced feature sizes and it follows the l2 scaling rule [14]. Considerable work has been done showing that the critical charge for scaled devices is expected to be lower for more advanced devices [15]. This often leads to the conclusion that SEU will be far more severe for highly scaled devices. However, this has not been observed for high-performance devices such as memory devices. Other factors such as decreases in charge collection depth or device architecture cause less charge to be collected as devices are scaled to smaller feature size.

6.0 CONCLUSION

This study tested the advanced, commercial, high-density 32-Gb SLC, 64-Gb MLC, and 64-Gb TLC NAND flash memories from Micron Technology. All the parts are built on a 25 nm process.

Heavy ion measurements were performed with LET range of 1.8–60 MeV-cm^2/mg on the 32-Gb SLC and 64-MLC NAND flash memories with normal incident as well as horizontal rotations of 60 degrees. The measurements at angles indicate that device susceptibility follows the cosine law, but there is some uncertainty because a complete set of angle tests was done with only one ion species. In comparing the SEU cross section of the 32 Gb SLC with the SEU cross section for the Micron Technology 1, 4, and 8 Gb SLC NAND flash memories, we noted that at LETs below 8 MeV-cm^2/mg, there are no noticeable differences between SEUs and threshold LETs for 1, 4, 8, and 32 Gb devices. Also, similar to low LET data points (LET below 8 MeV-cm^2/mg), there are no noticeable differences in SEUs in the range of 120–72 nm feature size; however, there is a reduction in the SEU cross section at 50 nm feature size and an increase in the SEU cross section at 25 nm. This indicates that scaling effect is effective below a certain feature size, in this case below 72 nm. The SLC devices are less sensitive to SEUs than MLC devices.

TID response of these flash memories from Micron Technology was also tested. These parts were irradiated up to 85 krad(Si). The charge pump was still functional at high-dose levels—an improvement compared to the older generation of flash memories in which the charge pump failed at about 10 krad(Si). In general the TID response improves with scaling.

7.0 REFERENCES

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