ANALOG AND MIXED SIGNAL ICs for use in FUTURE SPACE MISSIONS

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Mars Science Laboratory (Curiosity rover)
Launched: Nov. 26, 2011
Landing: Aug. 5, 2012

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NEPAG is actively involved with the procurement process - parts users and standards organizations join hands to ensure timely delivery of reliable parts from suppliers.
NEPAG ACTIVITIES

Questions/Requests for Information from Flight Projects
- Provide answers/solutions via telecon
- Increase Awareness of NEPAG
- Contact Design Engineers, PEs, MAMs, OCE (Explore Use of CISCO Meeting Place)
- Explore Publishing Parts Selection List
- Publish EEE Parts Bulletin

Critical Parts Shortage Bulletin
- Process Owner: GSFC
- GSFC Contact: J. Brusse
- JPL Contact: L. Risso

NEPP/NEPAG Organized Meetings/Workshops/Evals
- Strengthen Critical Parts Shortage Process:
  - Workout Financial Side of Transactions, Familiarity with DoD/EMALL
  - Update Vendor Inventory Page
- Update NASA A/D Converters Guide
- Organize Technical Meetings with Vendors/Experts
  - MAPLD
- New Technology Insertion; Lead-Free: ETW (Electronics Technology Workshop); FPGAs; BMEs; Other

DLA Audit of Manufacturers
- Contribute as Subject Matter Experts:
  - Gain Knowledge; Develop Contacts; Opportunity to Address Any Project Issues with That Supplier; etc.
- GSFC, JPL, MSFC, LaRC
- Explore Expertize at Other Centers
- Update SAS Database
- JAA Sign-Off
- Manufacturers’ Qual Data Review
- DLA SMD Review
- Documents Review; Other

DLA/JEDEC Support
- Add Class Y to 38535

NEPAG Teams
- DC/DC Converters; MIL-PRF-38535; MIL-PRF-38534; Counterfeit Parts; etc.
- One NASA Database for Audit Reports (GSFC)
- Training of NASA Parts Engineers
- Look Into Setting up a Technical Chat Line
- Capture Knowledge on NEPAG Website
- NASA to lead G12 Task Group

Weekly Telescons
- Moderator: M. Sampson
- Coordinator: S. Agarwal
- Create Database by Telecon Subject/Topic
- Explore New Resources for Telecon Topics – Periodic Updates on NEPP Tasks?

Support to NASA Flight Projects

Consult with NEPAG Community
Conduct Applied Research

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• NASA Review of Pre-released SMDs for Space Products
  - Understanding between NASA and DLA Land and Maritime-VA: NASA to provide comments within 10 days.
  - NASA comments considered essential by DLA Land and Maritime.
  - The in-house experts (Parts specialists, radiation specialists, packaging specialists, reliability engineering, and others) are called upon to support this effort.
  - New technology data review
    ▪ Suppliers using MIL-PRF-38535, Appendix H for dual-use technology
    ▪ Commercial parts developed for space customers
    ▪ An early NASA and space community involvement in new product definition, SMD development
  - SMDs reviewed to date in FY12: 20
• DLA Audits Support
  – DLA Land and Maritime-VQ (formerly DSCC) is the designated DoD entity that has **authority to approve or disapprove suppliers**. There are two parts to an audit: certification (capability demonstration) and qualification (successfully building product).
  – Agencies like NASA, Air Force, NRO bring **technical expertise** to audits.
  – Audits to be supported by space community are **decided on the NEPAG telecons**. We support audits as subject matter experts, gain personal knowledge, make contacts, and **resolve flight project issues**.
  – Audit team spends most of audit time on production floor, test floor, etc. to talk to operators, engineers, and witness operation or test being performed. Review supplier chain management.
  – Audit findings reported on NEPAG telecons. High-level summary of audits supported by NASA entered into NASA **SAS** (supplier assessment system) database.
  – Only a small portion of audits conducted by DLA are supported.
Recent Findings

- **Microcircuits**
  - Recent Findings from Audits, New Technology Data Reviews
    - **Disabled Chip Burn-ins.** Recent audit for QML device discovered chip was disabled during static burn-in; thus, it was not drawing any current. *Recommendation:* For new SMDs, add statement within burn-in paragraphs stating that parts shall be kept in their enabled state during burn-in.
    - **Class Q 160-hr/125°C Burn-in.** Interpreted as static burn-in (even for CMOS technology). *Recommendation:* Provide clarification in MIL-STD-883, Test Method 5004.
    - **At Frequency (Dynamic) Burn-ins.** Test equipment limitation cited for not doing burn-ins at application frequency. *Recommendation:* Burn-in task group to discuss and provide guidance. When SMD says that part can be used at 200 MHz, doing burn-in at 6 MHz (cited as burn-in equipment limitation frequency) is not going to be meaningful!
    - **Two Static Burn-ins.** Some manufacturers do electrical testing between two static burn-ins, whereas others do electricals after completing both static burn-ins. *Recommendation:* Provide clarification in MIL-STD-883, Test Method 5004.
    - **Thermal Imaging.** For a device with hot spots, thermal resistance, junction-to-case would be much higher than guidelines in MIL-STD-1835. One supplier used thermal imaging to find hot spots on the die. *Recommendation:* Assign a task group to evaluate effectiveness of thermal imaging at product development stage.
Recent Findings (Contd.)

- **Class M**
  - **Removal of Class M.** We have been told that class M parts with Q marking are equivalent to class Q parts. However, most SMDs from QML suppliers have both classes as shown in Table II of SMDs. Is one part, one part number still a requirement?  
  
  **Recommendation:** Keep class Q and remove class M from new SMDs.

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**Communication with one of the suppliers (June 1, 2012)**

- **NASA Comment:** Table IIA shows electricals for three classes: M, Q and V. Since, this is a brand new QML part and you will be the only supplier, you should consider offering it as Class V and Class Q. Remove Class M from the table to avoid confusion.

- **Supplier’s response:** We agree that the Class M information is unnecessary and that we will NOT be offering a Class M version of this part now or in the future. If DLA wants to remove it, then we are fine with it.

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**MIL-PRF-38535J, Para 6.4.27 Class M.**

- Items which have been subjected to and passed all applicable requirements of appendix A herein and are documented on an SMD. This product is intended for military applications.
Task Group- 2011-01
SMD Electrical and Burn-in Guidelines

• **Charter for Task Group.** Develop JEDEC document for guidance to suppliers and users that includes recommendations on Deltas, SMD electrical parameters, and Burn-in. Also, provide recommendations for any needed changes to MIL-STD-883.

1. **Burn-In**
   a. types required - dynamic and static/HTRB
   b. burn-in specified by technology or product type
   c. junction temperatures to be achieved
   d. burn-in conditions - voltages, frequency, etc.

2. **Delta Requirements**
   a. definition - critical parameters selected to provide a measure of product and process stability
   b. selection of delta parameters

3. **Electrical Measurements**
   a. parametrics
   b. functional
   c. selection of limits based on ???
   d. parameters guaranteed
      1) but not tested
      2) by design
      3) by characterization data
      4) data required to validate guaranteed position
NASA Inputs to B.I. Task Group

1. Clarify burn-in requirements for space products in Table I of Method 5004: specifically, screening steps 3.1.10, 3.1.12, footnote 9/ and footnote 10/. As written, it implies that dynamic burn-in is a requirement. However, it is not always done. Moreover, for certain functions, such as a precision voltage reference, how would you design a dynamic burn-in? Requirements need to be reviewed and updated.

2. HTRB vs Static Burn-in. No mention of Static burn-in in Table I of Method 5004. We all know that digital products are subjected to Static burn-ins, often two: one for low condition (Static I) and the other for high condition (Static II). Add reference to static burn-in(s) as appropriate.

3. How are burn-in voltage, frequency, etc. supposed to be determined?

4. Are any manufacturers using low temperature burn-in? If yes, low-temp burn-in option should be included in screening spec.

5. What Ea should be used for new technology? Some manufacturers using fixed Ea of .7eV.

6. Time-temperature regression tables, e.g. Table I in Method 1015, should be reviewed. What Ea are they based on? Is that still valid?
7. Restricted temperature parts: What and how are burn-in temperatures determined?

8. Dynamic burn-in for high-speed devices. What frequency should be used?
Future Space Missions

- Analog and Mixed Signal Devices
  - Some Challenges
    - **Dual Use Technology.** Infusion of selected commercial device functions into QML system. Parts might not operate over full military temperature range. Moreover, there may be hot spots on the die.
      *Recommendation:* Review SMDs (see slide 15). Use techniques such as thermal imaging to look for hot spots and make necessary adjustments to thermal resistance values.
    - **Testing high-speed and high-resolution A/D converters.** Would be challenging for users to perform reliability and radiation-testing.
      *Recommendation:* Consider forming consortia with manufacturer and other users. Request new JEDEC task group be opened to address this challenge – what can be tested, how, and what is good enough?
    - **Upscreening of PEMs, lower grade hermetic parts.** Many challenges: electrical testing, type of burn-in, glass transition temperature (for PEMs), third-party management, etc.
      *Recommendation:* Ask manufacturer if they would consider doing it (sufficiently high quantities might justify it). Form consortia. Consider application-specific testing.
    - **Counterfeit Parts.** World-wide problem.
      *Recommendation:* Buy parts from franchised/authorized distributors.
    - **Supply Chain Management.** Self audits are an issue (see slide 16).
      *Recommendation:* Work with (in case of the United States) DLA Land and Maritime. Handling and ESD issues take on increasingly important role.
Future Space Missions (contd.)

• Analog and Mixed Signal Devices
  – Some Challenges (contd.)
    ▪ **New technology evaluation.** How to evaluate?
      *Recommendation:* Use MIL-PRF-38535, Appendix H. Some suppliers perform wafer level reliability (WLR) assessment.
    ▪ **New package configurations; e.g., CGAs (Column Grid Arrays).** Parts standardization effort has severely lagged behind advancements in packaging technology. A/D suppliers have announced products in CGA configuration but no mil standards are in place to establish requirements after columns have been installed. Are CGA parts an assembly, rather than a part? Often, users buy LGAs (Land Grid Arrays) and then get the columns attached.
      *Recommendation:* JEDEC task group is addressing CGA issues. DLA audit team discussing CGA issues with suppliers. Use caution when buying LGAs and getting columns installed – original manufacturer’s warranty may become void.
    ▪ **Signal-integrity capacitors for high-speed A/D converters.** For signal-integrity considerations, tiny low-voltage capacitors are used inside IC packages. Usually commercial capacitors of BME (base metal electrode) construction.
      *Recommendation:* JEDEC task group with task of defining screening and qualification requirements for BME capacitors.
    ▪ **New materials.** Materials such as underfills used in new packages would need to be evaluated.
Future Space Missions (contd.)

• Analog and Mixed Signal Devices
  – Some Challenges (contd.)
    ▪ **Budgetary Pressures.** Will continue – particularly challenging for high-reliability, non-repairable missions.
    ▪ **Implementation of requirements.** Self Do the tests/screens done meet the intent of specification?
      Recommendation: Perform audits as necessary.
## A New Trend – Supply Chain Management

<table>
<thead>
<tr>
<th>Operation</th>
<th>Responsible Party</th>
</tr>
</thead>
<tbody>
<tr>
<td>Die design</td>
<td>Manufacturer</td>
</tr>
<tr>
<td>Fabrication</td>
<td>Operation A (could be performed by the mfr or Company A)</td>
</tr>
<tr>
<td>Package design</td>
<td></td>
</tr>
<tr>
<td>Package manufacturing</td>
<td>Operation B</td>
</tr>
<tr>
<td>Wafer lap and dice</td>
<td>Operation C</td>
</tr>
<tr>
<td>Assembly</td>
<td>Operation D</td>
</tr>
<tr>
<td>CGA column attach</td>
<td>Operation E</td>
</tr>
<tr>
<td>Solderability</td>
<td></td>
</tr>
<tr>
<td>Screening/electrical/package</td>
<td>Operation F</td>
</tr>
<tr>
<td>Tests</td>
<td></td>
</tr>
<tr>
<td>Complete electricals per SMD</td>
<td>Operation G</td>
</tr>
<tr>
<td>Internal water vapor content</td>
<td>Operation H</td>
</tr>
<tr>
<td>Radiation testing</td>
<td>Operation I</td>
</tr>
<tr>
<td>And so on....</td>
<td></td>
</tr>
</tbody>
</table>
Operating Temperature Ranges, Use Caution
(Not all parts guaranteed over mil temp range)

Example: DLA SMD 5962-99607

<table>
<thead>
<tr>
<th>Device type</th>
<th>Generic number</th>
<th>Circuit function</th>
<th>Access time</th>
</tr>
</thead>
<tbody>
<tr>
<td>01</td>
<td>8Q512</td>
<td>512K X 8-bit rad-hard low voltage SRAM (MIL Temp)</td>
<td>25 ns</td>
</tr>
<tr>
<td>02</td>
<td>8Q512</td>
<td>512K X 8-bit rad-hard low voltage SRAM (Extended Temp)</td>
<td>25 ns</td>
</tr>
<tr>
<td>03</td>
<td>8Q512</td>
<td>512K X 8-bit rad-hard low voltage SRAM (MIL Temp)</td>
<td>20 ns</td>
</tr>
<tr>
<td>04</td>
<td>8Q512</td>
<td>512K X 8-bit rad-hard low voltage SRAM (Extended Temp)</td>
<td>20 ns</td>
</tr>
<tr>
<td>05</td>
<td>8Q512E</td>
<td>512K X 8-bit rad-hard low voltage SRAM (MIL Temp)</td>
<td>20 ns</td>
</tr>
<tr>
<td>06</td>
<td>8Q512E</td>
<td>512K X 8-bit rad-hard low voltage SRAM (Extended Temp)</td>
<td>20nS</td>
</tr>
</tbody>
</table>

Operating case temperature, (TC) (Device 01, 03, and 05) ................... -55° C to +125° C
Operating case temperature, (TC) (Device 02, 04, and 06) ................... -40° C to +125° C

(Bottom line: This SMD is implying that there may be a performance issue at low temperatures. Use caution for operation at low temperatures. Work with the manufacturer, get product test/characterization data.)

Some other Memories, 5962-01533 and 5962-01511 are specified as follows:
Device type 01, -40C to +125C; Device types 02 and 03, -40C to +105C.
These may have performance problems at both low and high ends.
Background

In 2009, big push to bring the Xilinx Virtex-4 (a non-hermetic part) into QML system as Class V device. NASA and others not in favor; it would have created massive confusion. Mike Sampson conceived idea of new Class Y for non-hermetic space parts to provide QML coverage for Xilinx Virtex-4 and similar devices.

New G-12 Task Group, TG 2010-01, formed in early 2010 to address non-hermetic devices for space. Shri Agarwal was asked to lead.

Challenging task:
- Far more involved than typical G12 tasks
- Required development of new concept
- Used system-on-a-chip (SoC) — one of the most complicated devices
- Needed to be simple and easily understood
- Possessed sketchy testing and board assembly boundaries
- Needed to procure standard QML product as quickly as possible.
New QML Class “Y”

- An attempt to bring advancements in packaging technology into QML system.
- Advancements in packaging technology and increasing functional density and operating frequency have resulted in single-die SoCs with non-hermetic flip-chip construction, in high-pin-count ceramic column grid array packages
  - “Poster Child” example: Virtex-4 (V-4) FPGAs from Xilinx
  - Such products were evaluated for radiation and reliability; have drawn attention of the space user community
- Question: How do we bring V-4 and similar microcircuits into QML system as space products?
  - Can’t be Class V – those are hermetic devices
  - Intend to put V-4 like products for space users in a new category: “Class Y”.
  - G-12 opened Task Group to develop Class Y
- What if we dropped Class Y effort?
  - Would be major loss for space community and QML program at large because industry would be limited to ordering via Source Control Drawings (SCDs) – counterproductive to Mission Assurance, prevents standardization, and is expensive.
Infusion of New Technology into the QML System
G12 Class Y Effort at a Glance

Task Group Activities
- Review M. Sampson Idea
- Class Y Concept Development
- EP Study (DLA-VA)
- Coordination Meeting at DLA Land & Maritime (April 2012)
- Add Class Y Requirements to 38535 and 883 (DLA-VA)
- Manufacturer Certification to QML-Y (DLA-VQ)

Task Group Inputs
- Government
- Manufacturers
- Primes
- Others

Newly Formed Task Groups with Class Y Interest
- JC13.2 Electronic Parameters & B.I. Standardization
- JC13.2 Flip-chip Package BGA / CGA** Requirements
- G12 & G11 Passives Device Requirements in 38535

Other Task Groups with Class Y Interest
- G12 Plastics Subcommittee
- JC13.2 5004/5 vs. 38535 Tables & 883 vs. 38535 Comparison
- JC13 Overlapping Device Definitions 38534 vs. 38535

- Aeroflex (October 2011)
- Xilinx (February 2012)
- Honeywell (May 2012)
- BAE (October 2012)
- Non-Hermetic Conference Jan. 2012, Orlando
- CMSE (Feb. 2012), LA Conference

* PIDTP = Package Integrity Demonstration Test Plan
** BGA / CGA = ball-grid array / column-grid array
Conclusion

• Challenging times ahead for mission assurance
• Budget constraints
  – Do more with less
  – More so, for non-repairable missions
• Communication
  – AMICSA
  – NEPAG
  – JEDEC
  – Other means
• Flexibility needed
  – Especially when it comes to adapting new technology