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Reliability Considerations for Ultra- Low Power Space Applications

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Purpose

- **Higher performance, lower operating and stand-by power characteristics of Ultra-Low Power (ULP) microelectronics are not only desirable, but are also needed to meet low power consumption design goals of future space systems.**
- **The integration of ULP components in such systems, however, must be balanced with the overall risk posture of the project.**
- **The ability of ULP components to meet high reliability goals and withstand spacecraft environments must be sufficiently understood.**

Outline

- **Introduction & Motivation**
- **Spacecraft Technology Developments**
- **ULP Microelectronics**
- **Scaling & Performance Trade-Offs**
- **Reliability Considerations**
- **Spacecraft Environments**
- **Summary & Conclusions**

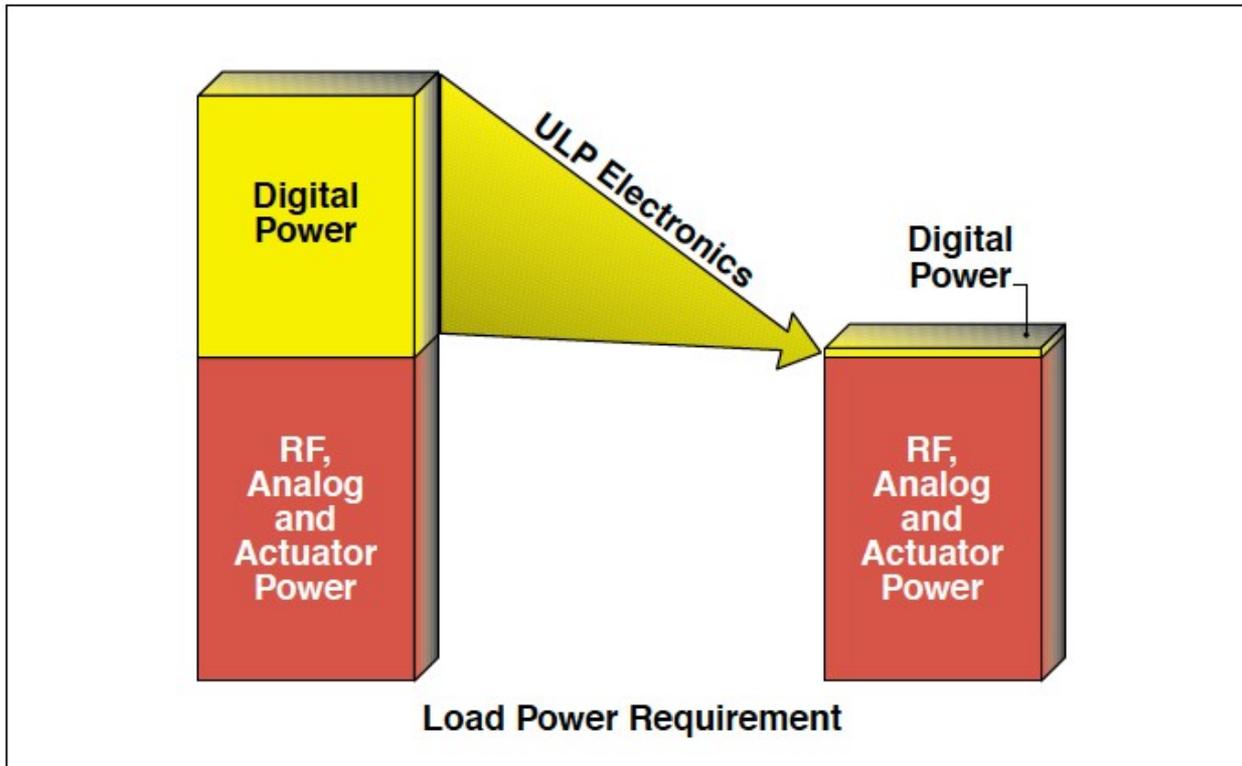
Introduction

- **NASA, the aerospace community, and other high reliability (hi-rel) users of advanced microelectronic products face many challenges as technology continues to scale into the deep sub-micron region and ULP devices are sought after.**
- **Technology trends, ULP microelectronics, scaling and performance tradeoffs, reliability considerations, and spacecraft environments will be presented from a ULP perspective for space applications.**

Spacecraft Design

- **Goals:**
 - **Reduction in system power requirements**
 - Do more with less
 - **Reduction in mass**
 - Solar arrays
 - Spacecraft bus
 - Batteries
 - Heat sinks
 - **Enhanced performance and capabilities**
 - Computational enhancements
 - Data processing
 - Data storage

Spacecraft Design – ULP Benefits



- ULP electronic architectures can significantly reduce the power required for digital processing.
- Load power reductions of 20-40% or more, resulting in either mass savings or increased power available for other functions.

Radiation in Space

- **Total dose from trapped radiation belts and solar flares**

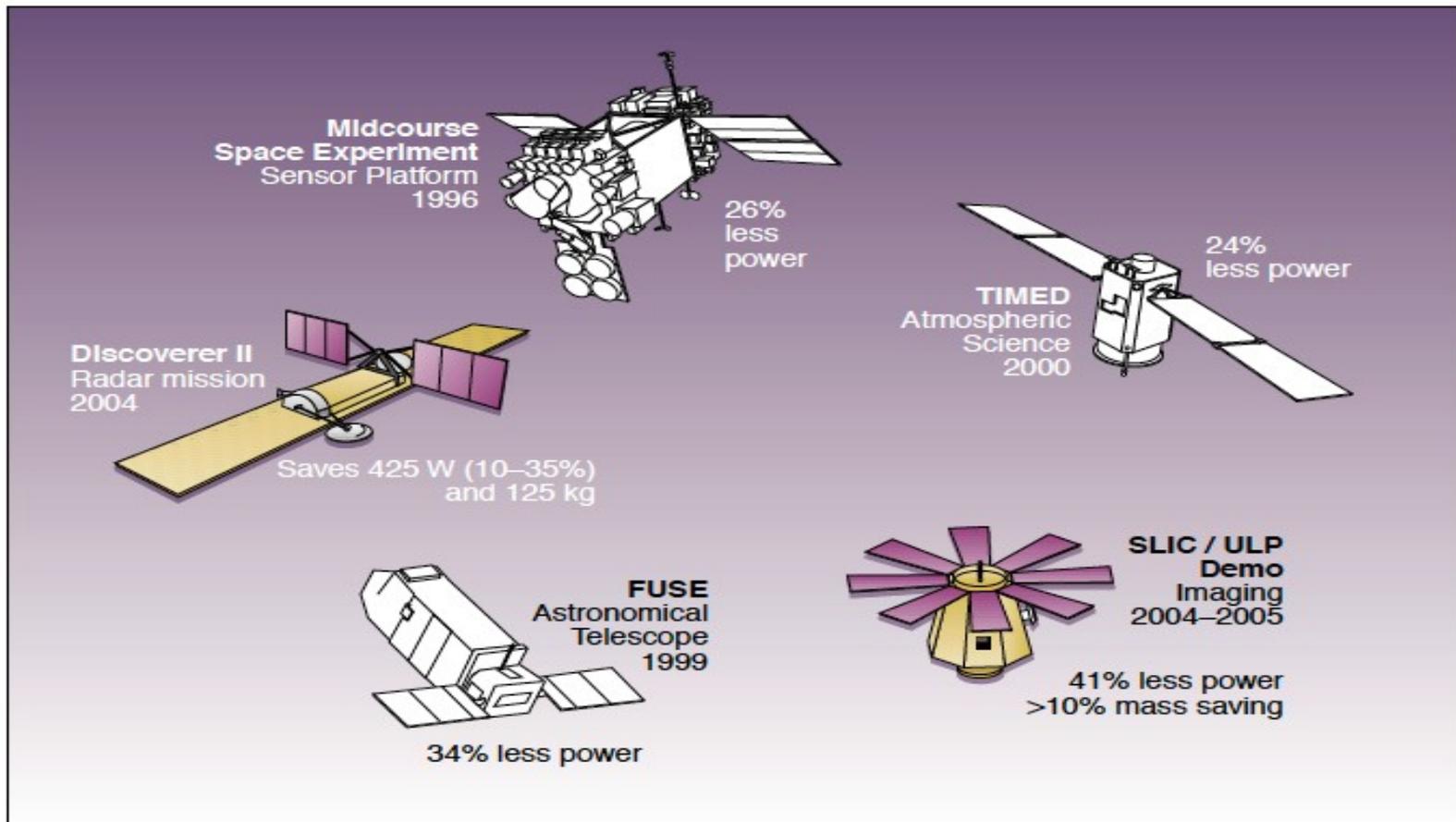
Mission requirements: 5 – 20 krad for typical missions

**> 50 krad for exploration missions
near Jupiter**

***Low-power CMOS is more affected by isolation
leakage than conventional designs***

- **Single-event upset effects from galactic cosmic rays, solar flares, and high-energy protons**
 - **Similar to soft-error problem in terrestrial applications**
 - **However, galactic cosmic rays have much higher charge deposition density**
 - **These effects will be discussed later in the presentation**

Power Savings with ULP Electronics

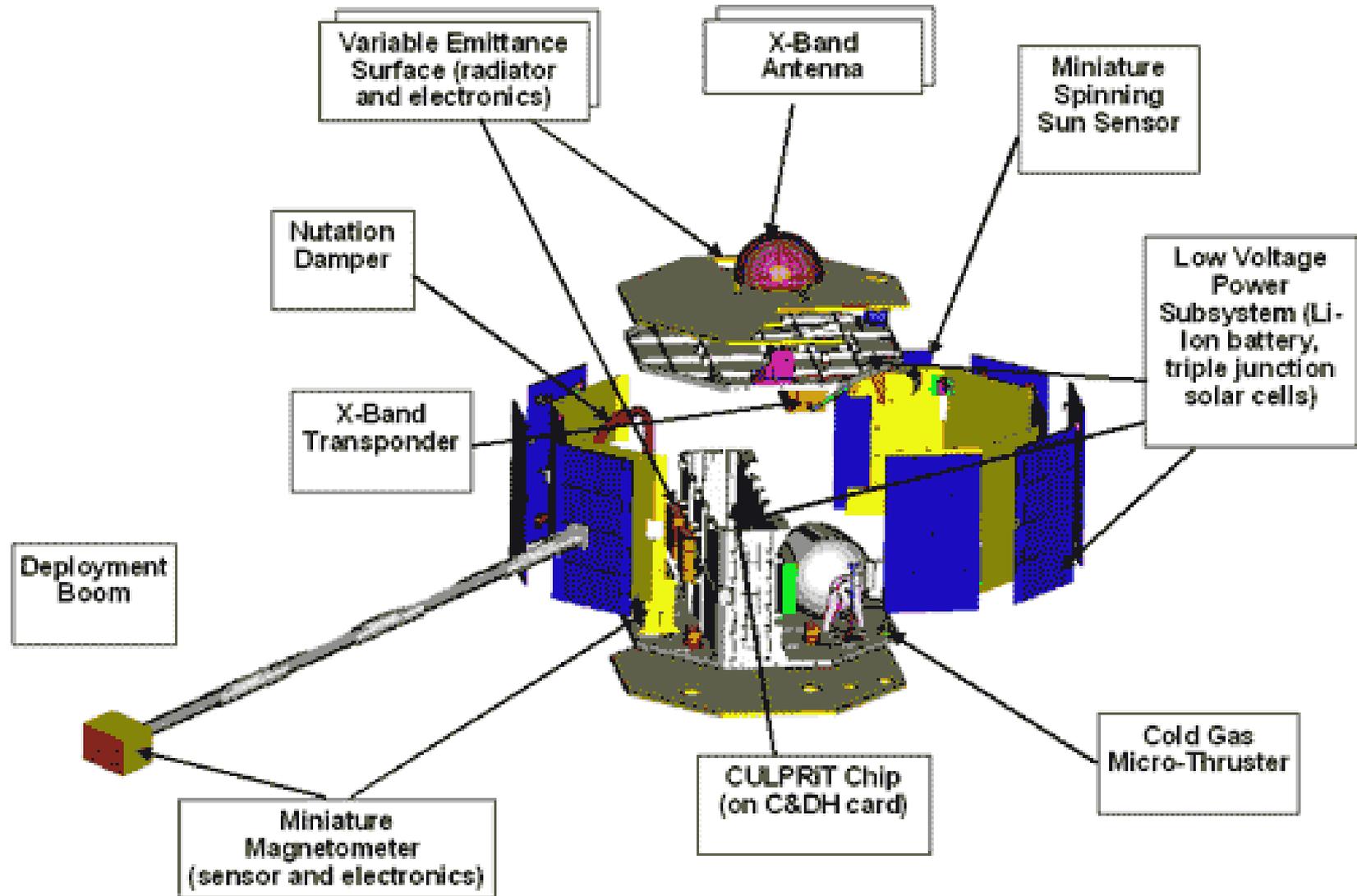


- The best percentage power reductions will be for relatively small, moderate bandwidth spacecraft with passive sensors.
- ULP technology enables large amounts of LP on-board digital processing (e.g., image compression).

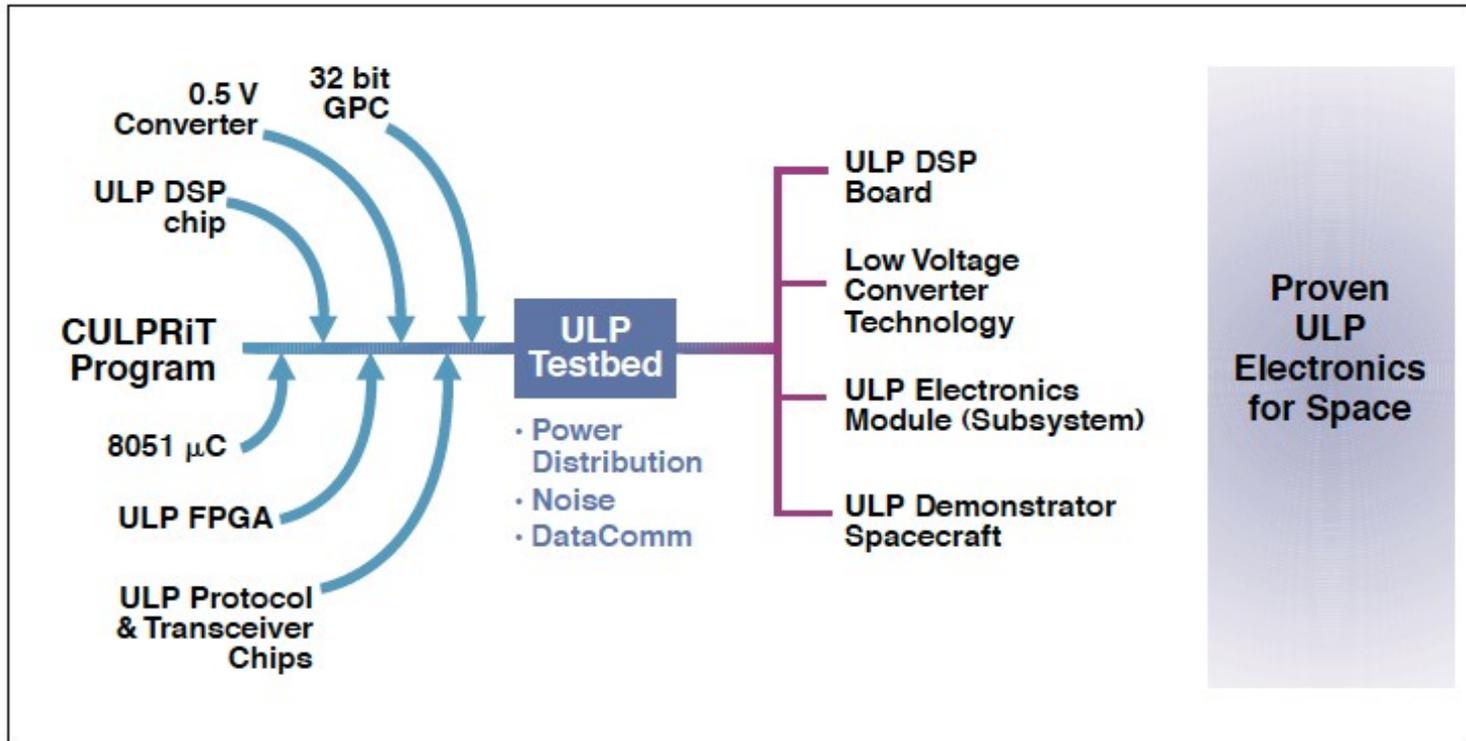
Technology Demonstration

- **NASA's three Space Technology 5 (ST5) micro-satellites completed their planned 90-day mission in 2006.**
 - **Lithium-Ion Power System for Small Satellites**
 - The Low-Voltage Power System used a low-mass Li-Ion battery with triple junction solar cells.
 - **Ultra Low-Power Demonstration**
 - CMOS Ultra-Low Power Radiation Tolerant (CULPRiT) technology – A Reed-Solomon channel encoder that operated at 0.5 Volts (0.35um CMOS technology)
 - Designed to greatly reduce power consumption while achieving a radiation tolerance of ~100kRad total dose, SEU \approx 40 MeV LET by design and latch-up immunity
 - Over 300 million telemetry frames processed without a failure

ST5 Technology Demonstration



Roadmap for ULP Implementation



- Achieving ULP benefits in space applications
- More work needed for ULP FPGAs, subsystem communication interfaces, and mixed analog and digital ULP circuits

CubeSat & NanoSat Space Missions

- **CubeSats are a class of research spacecraft called nanosatellites.**
- **NASA has selected 20 small satellites to fly as auxiliary cargo aboard rockets that either have launched or are planned to launch in 2012.**
- **The proposed CubeSats come from universities across the country, NASA field centers and Department of Defense organizations.**
- **The cube-shaped satellites are approximately four inches long, have a volume of about one quart and weigh 2.2 pounds or less.**
- **The satellites are expected to conduct technology demonstrations, educational research or science missions.**

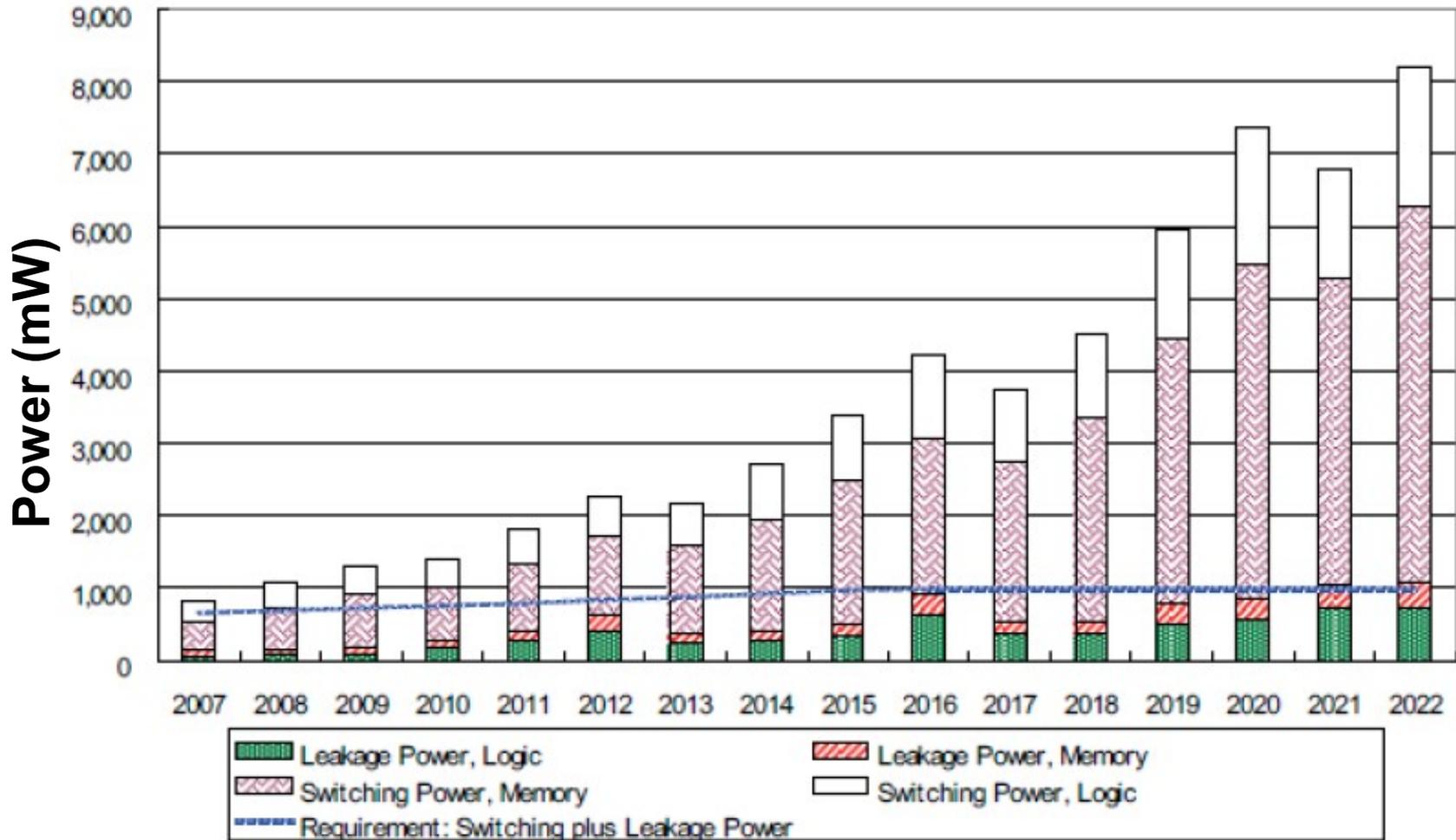
ULP Microelectronics

- **Devices that have a milli- or micro-watt power consumption:**
 - $P_{total} = P_{ac} + P_{dc}$
 - **Supply voltage <1 V**
- **ULP market drivers:**
 - **Portable and wireless devices requiring extended battery life**
 - **Remote space-based sensors**
 - **Biomedical devices**
 - **Ultra-Low Power computation**
 - **Energy management circuits**
 - **Memory technologies**
 - **DRAM**
 - **SRAM**
 - **Flash**

Power Consumption

- Overall power consumption is a top concern for devices used in space applications because of system power limitations.
- Power consumption is a major restriction in chip design.
 - Static leakage is a particular concern
- Changes necessary to reduce power consumption may be at the circuit level as well as with the process parameters.
- Process changes to modify the threshold voltage reduce current drive and thus, power consumption.
- Sub-threshold circuit operation is one approach to lowering power consumption.
- *The reliability and radiation aspects of using ULP devices in space must be considered.*

Trends in Power Consumption



CMOS Power Consumption

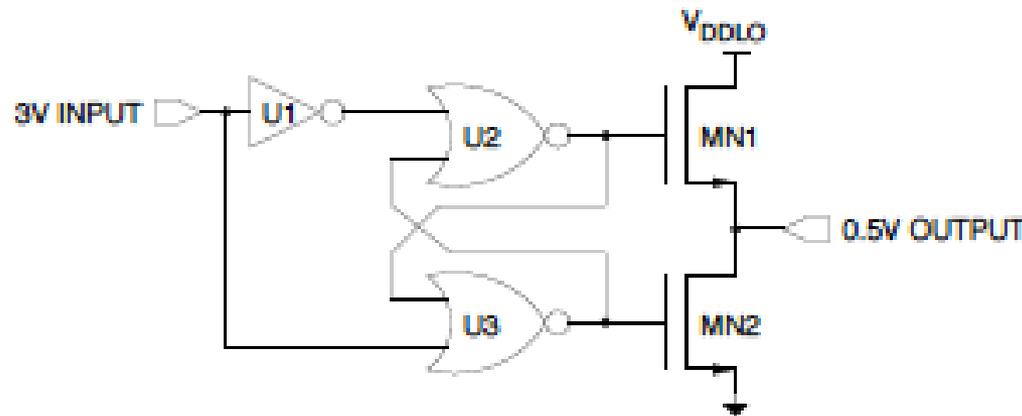
- Total power dissipated is the sum of both dynamic (Switching) power and the static (Leakage) power dissipation.

$$P_D = (K * C_L * V_{dd}^2 * f) + (I_l * V_{dd})$$

- K is the switching factor
 - C_L is the average node capacitance loading of the circuit
 - V_{dd} is the supply voltage
 - f is the switching frequency
 - I_l is the DC leakage current
- P_{AC} dominates for circuits with high activity.
 - P_{DC} dominates for circuits with low activity.
 - The most effective way to reduce power consumption in active circuits is to reduce the supply voltage.

ULP Microelectronic Interface

- For a variety of reasons it is often desirable to interface such low voltage devices to conventional electronics operating at nominal supply voltages of 5 V or 3.3 V (Typical CCA voltages).



Typical Down Shifter Circuit

- Use of an NMOS transistor as a pull-up device in a source follower configuration.
- The output driver arrangement requires complementary drive signals for the two NMOS transistors, which is accomplished by simply adding an inverter, U1.
- Cross coupled NOR gates, U2 and U3, are added to prevent an overlap between the gate drive signals for the NMOS output transistors.

Design Trade-offs with ULP Devices

- **ULP Microelectronics Main Concerns:**
 - **Process variation**
 - Reduction in supply voltage increases the effect of process variations leading to timing delay spread and decreased noise margin.
 - **Static leakage power consumption**
 - The current that leaks out of transistors that are left in the “on” state when they’re not being used.
 - On-chip energy management.
 - **Trades between supply voltage, threshold voltage, device dimensions, delay performance, activity rate and power consumption**
 - Transistors are mostly biased in the sub-threshold region to reduce static and dynamic power consumption.

Variability Issues with ULP Devices

- **Process**

- As CMOS scaling approaches the 25nm node, random threshold voltage (V_t) variation caused by statistical variation in the number of dopant atoms may lead to more than 100mV of V_t variation.

- **Voltage**

- The voltage margin of V_t sensitive circuits, such as flip flop circuits that DRAMs use for sense amps and SRAMs use for cells, is reduced compared to higher power designs.

- **Temperature**

- A temperature variation of 100°C could cause sub-threshold currents to increase more than four orders of magnitude.

- ***Each of these factors are accentuated at lower technology nodes and operating voltages.***

Reducing the Effect of Variability in ULP Devices

- **Redundancy and ECC**

- Essential in avoiding DRAM sense amp and SRAM cell failures caused by excessive intra-die V_t mismatches and in allowing for the minimum V_{dd} for successful operations
- On-chip ECC for repairing random defects

- **Symmetric Layouts for Flip-Flop Circuits**

- Tight controls of channel length and width will help reduce V_t variation and V_t mismatch.

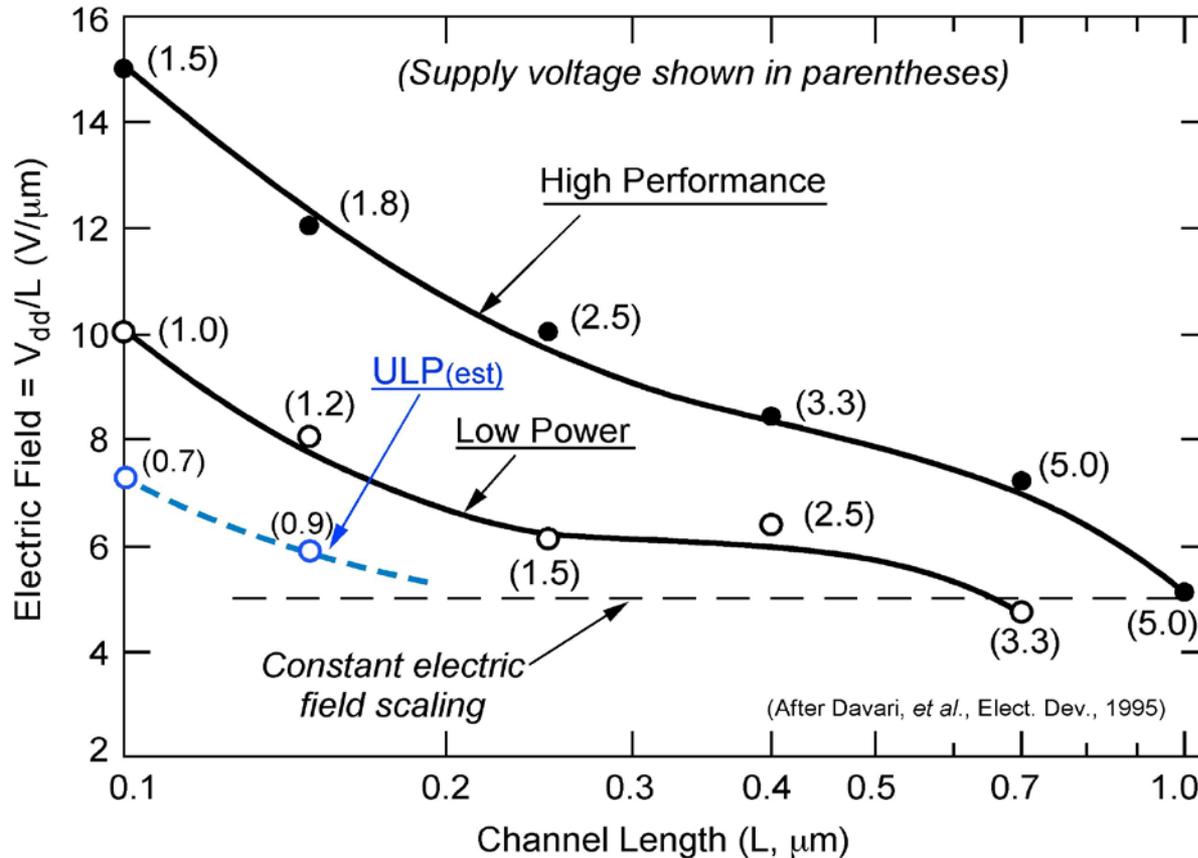
- **Control of Internal Supply Voltages**

- Suppression of and compensation for variations of design parameters (V_t , V_{dd} , temperature) through controls of internal voltages with on-chip voltage converters

- **Optimize Power Supply Voltage**

- V_{dd} must be kept sufficiently high to account for intra-die variations in V_t (and V_t mismatch) to minimize timing and voltage margin differentials.

CMOS Scaling Branches

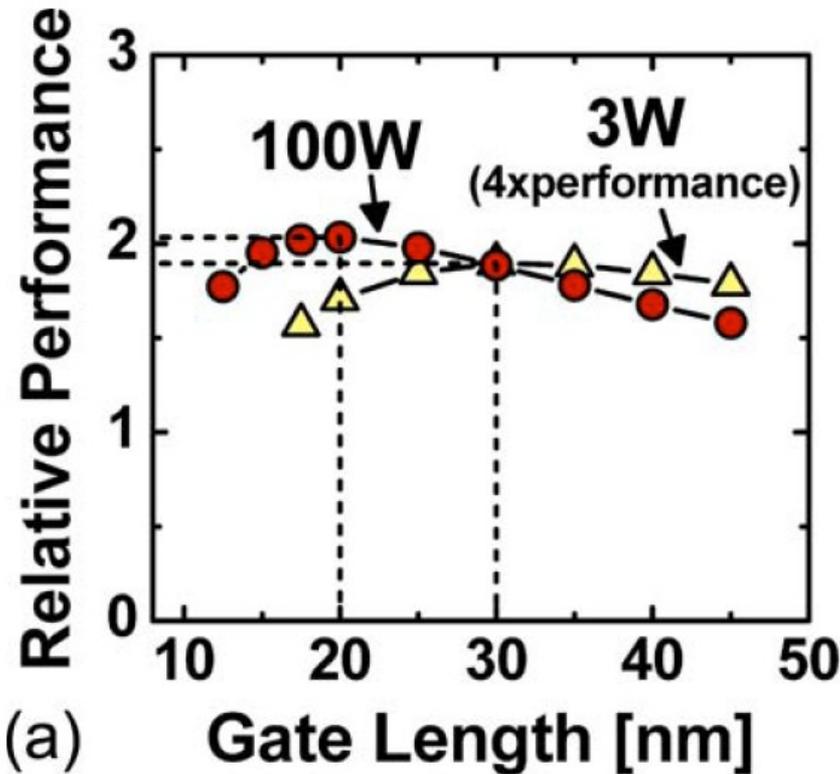


- Channel electric field is important for device scaling.
- Older studies considered high-performance and low power.
- ULP trends are compared in this figure with older work.

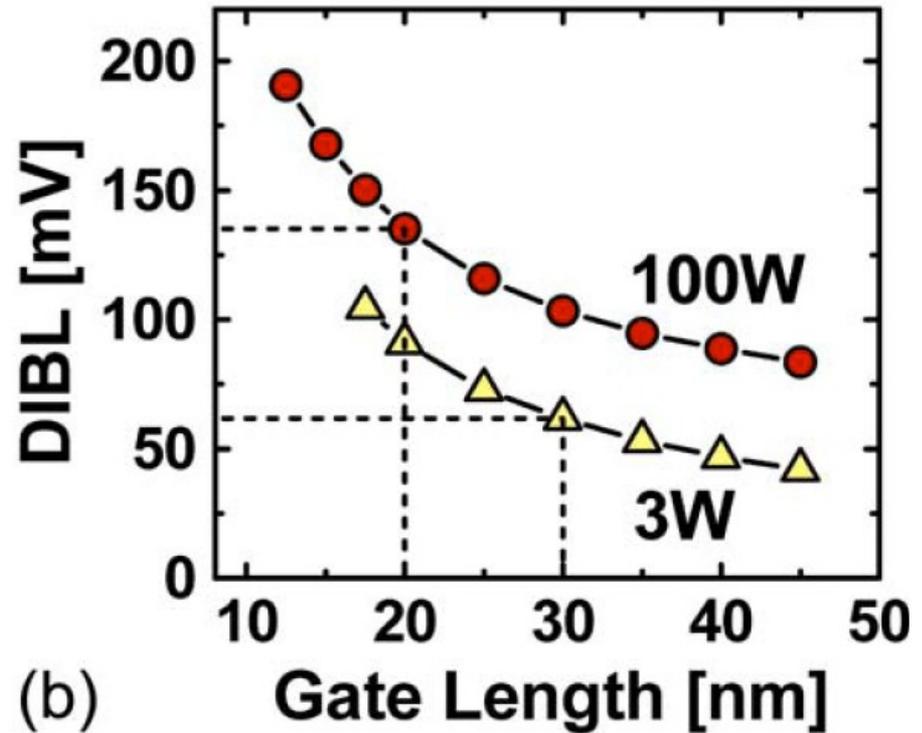
Fundamental Effects of Scaling

- **Fundamental Scaling Effects:**
 - **Gate length**
 - Drain-induced barrier lowering (DIBL) requires longer gate length for low-power designs.
 - **Static leakage power**
 - Transistor sub-threshold leakage
 - Gate current (tunneling in thin gates)
 - On-chip energy management
 - **Trades between supply voltage, threshold voltage, device dimensions, delay performance, activity rate and power consumption**
 - Transistors are mostly biased in the sub-threshold region to reduce static and dynamic power consumption.

An Example at the 22 nm Node



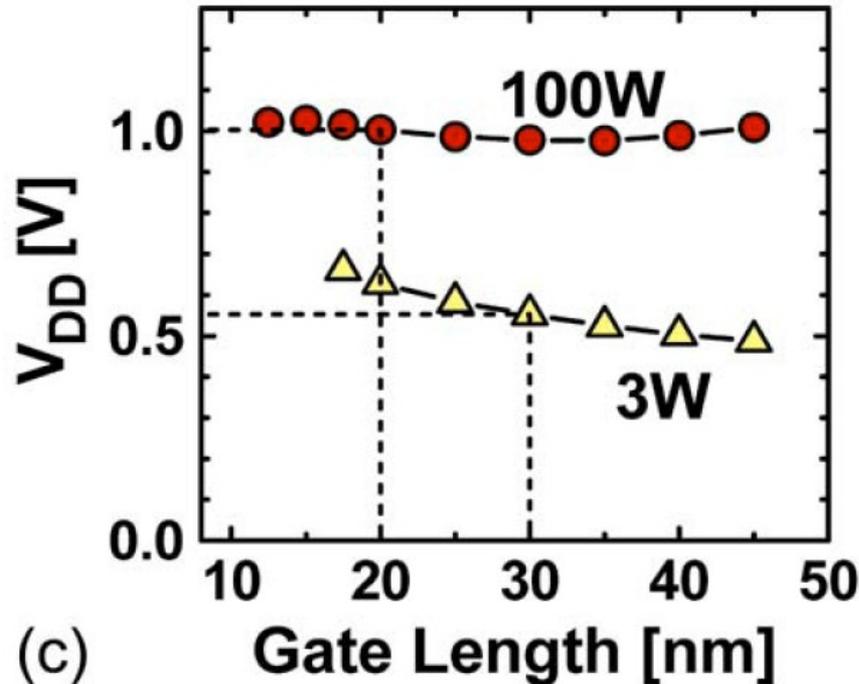
(a)



(b)

- Gate length dependence of (a) performance and (b) short-channel effects in 22 nm bulk MOSFET technologies optimized for processor chips of two different power levels (3W & 100W).
- For the low-power case, optimal performance occurs at much larger gate lengths, dramatically reduced DIBL, and lower voltages.

An Example at the 22 nm Node (Cont.)



(c)

- Gate length dependence of (c) voltage in 22 nm bulk MOSFET technologies optimized for processor chips of two different power levels (3W & 100W).
- For the low-power case, optimal performance occurs at much larger gate lengths, dramatically reduced DIBL, and lower voltages.

CMOS Scaling Trends

Application	Primary Design Concerns	Power Supply Voltage	Gate Threshold Voltage	Reliability Issues
High performance	Switching speed	< 1 V	0.3	Electromigration on Contact integrity
Mainstream	Maximum functionality density	1 to 1.2 V	0.4	Percent defect ratio of electrical test
Low power	Low total power dissipation	< 1 V	0.25	Percent defect ratio of electrical test
Memory	Low leakage and low standby current	3.3 V (internal back bias generator are often used to decrease leakage current)	0.5	Retention time for dynamic memories; early bit failures in large density SRAMs

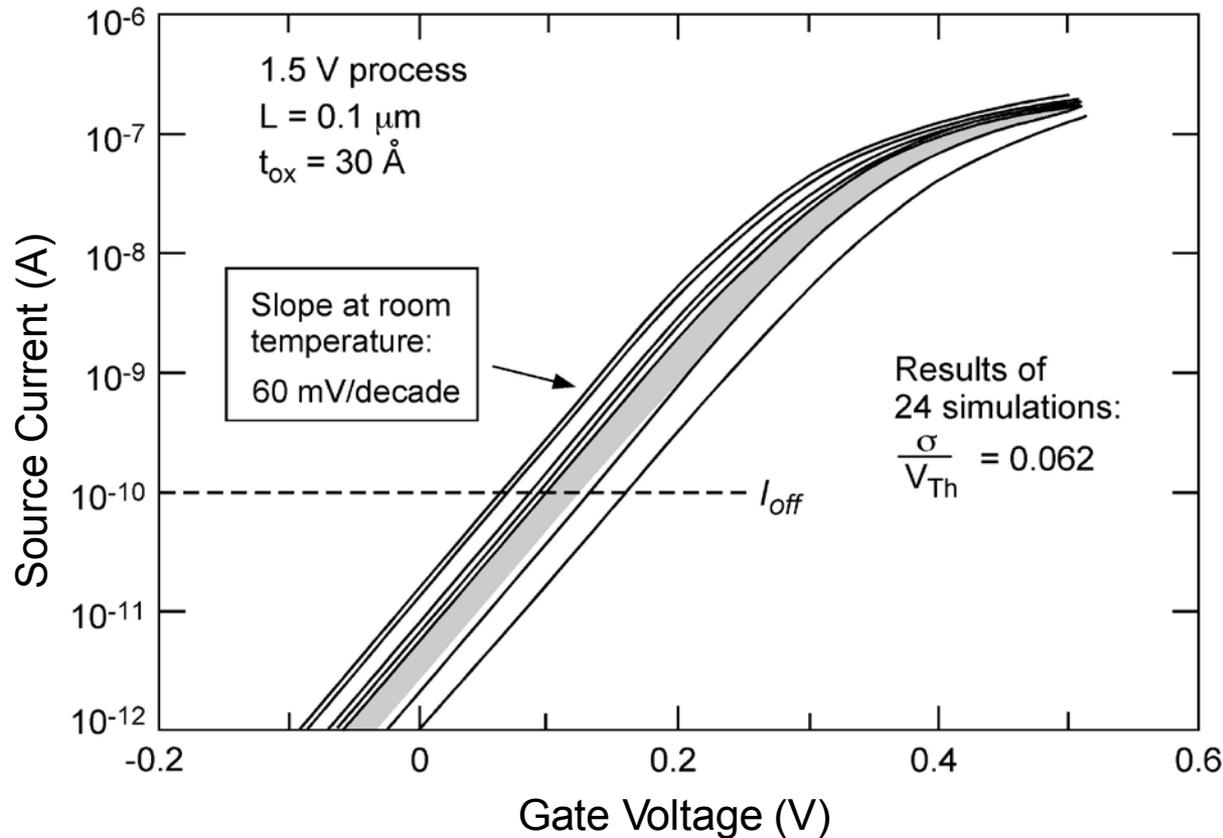
Effects of Processing Variation on Reliability

Historical Process Variations	Emerging Process Variations
<ul style="list-style-type: none">• Patterning proximity effects• Line edge and line width roughness• Surface roughness (polishing)• Variations in gate oxide thickness• Fixed charge and oxide traps	<ul style="list-style-type: none">• Random dopant fluctuations• Variations in implants and anneals• Variations associated with strain• Gate material granularity

K.J. Kuhn, et al., 2011

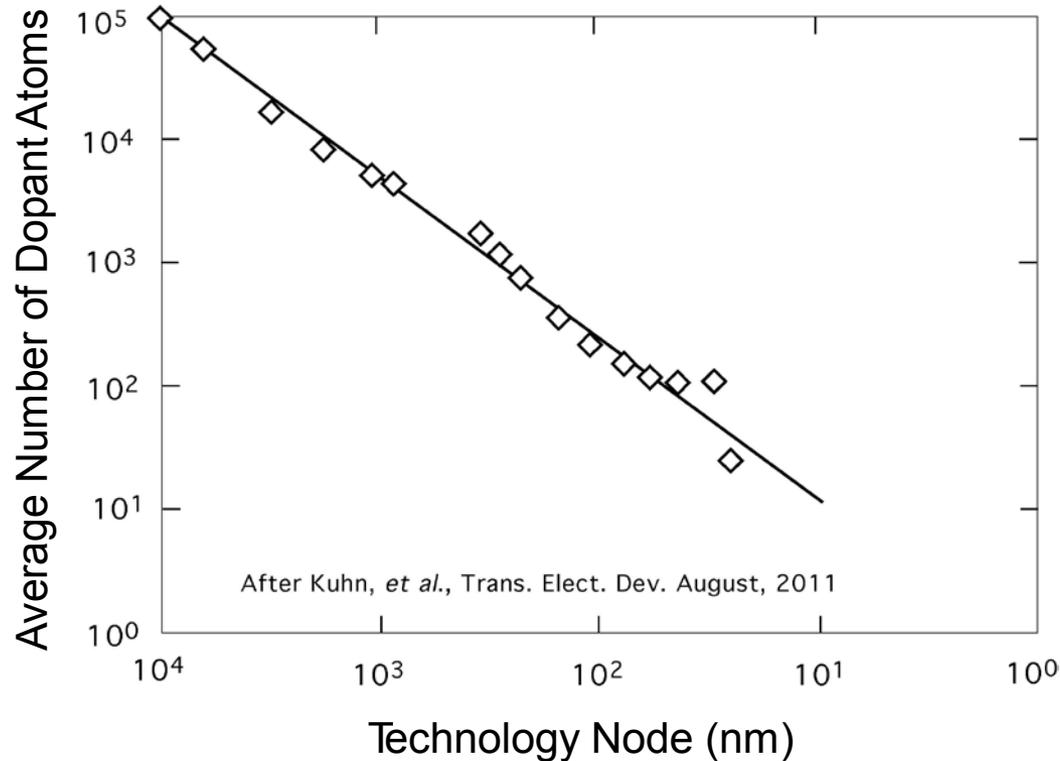
- **Many of the historical issues have been solved by clever improvements in processing.**
 - The difficulty of coping with corner rounding and geometrical limitations associated with lithography has been overcome by designing devices in pairs for feature sizes of 65 nm and below.

Statistical Fluctuations in V_{th}



- Sub-threshold slope showing the effect of statistical fluctuations in threshold voltage on the on/off current ratio
- Reduces noise margin
- More severe at higher temperatures

Number of Dopant Atoms (High Performance CMOS)



- **Very few dopant atoms are present in highly scaled CMOS.**
- **ULP transistors have larger geometry, reducing this limitation.**

Dominant Reliability Issues (FEOL)

- **Front-End Processing**
 - Random dopant fluctuations
 - Significant process changes to continue Moore's Law
 - Hafnium oxide metal gate transistors (< 65nm)
 - Strained crystalline structure (< 90nm)
 - Potential new failure mechanisms
 - TDDB, contact integrity, hot-carrier degradation
- **For Space Applications:**
 - Confirm manufacturer follows design rules and that their process technology provides adequate reliability margins.

Dominant Reliability Issues (BEOL)

- **Back-End Processing:**
 - **Metallization**
 - Voids, grain boundaries, thinning of metallization over non-planar regions
 - **Electromigration**
 - Clock drivers and I/O circuits where higher currents are required
 - Vias in copper interconnects
 - Low-k dielectrics used in more advanced processes (metal can migrate within dielectric materials)
 - **Packaging**
 - More advanced packaging techniques (BGAs, PGAs, CGAs)
 - Stress risers at corner regions (cracking, intermittent or open contacts)
 - Non-hermetic plastic packaging (moisture transport)
 - Thermal expansion coefficient of the die and packaging
- **For Space Applications:**
 - Apply appropriate screening and qualification methodology for the application
 - Derate appropriately for space applications

Relationship of Foundries & End-Manufacturers

Methods to obtain parts for space use through commercial foundries, which are the only option for highly scaled ULP processes:

- **Parts manufactured through working agreements with mainstream producers of hi-rel parts**
 - **Arrangement between the foundry and producer depends on the contracts between them**
- **Trusted foundries**
 - **Government establishes the relationship between the specific foundry and the designers**
- **Parts produced on modified commercial processes**
 - **Changes are made to the process for specific wafers or wafer runs that are used for hi-rel (often radiation-hardened processes)**

Tests & Evaluations for ULP Device Source Selection

Three distinct steps are in the overall process of selecting and qualifying advanced ULP CMOS parts for space applications:

- Establishment of the source selection requirements for the mfr.**
- Determination of qualification requirements for testing and evaluating the parts produced by the process**
 - May include monitoring process control or reliability test vehicles (generally destructive)**
- Specific screening tests on the final product that include tests directly related to the circuit application and the environmental requirements.**
 - Applied to all flight parts, and must be done under carefully controlled conditions; they cannot be destructive, but may result in elimination of some parts from the flight lot that do not pass the screening tests.**

Tests & Evaluations for ULP Device Selection

Mechanism	Approach Used by Vendor	Additional Steps and Processes for Space Use	Specific Screening Methods
Front-end processing	Specific failure mechanisms evaluated with test structures Statistical process evaluation	Review and track reliability data from vendor	None for this category
Back-end processing	Specific failure mechanisms evaluated with test structures (metallization, bonding and vias)	Review and track reliability data from vendor	None for this category
Packaging	Packaging yield and failure mechanisms	Review and track reliability data from vendor Construction analysis	Additional temperature cycling tests
Overall process reliability	Yield of final product (relative values may be adequate for this evaluation)	Evaluation and additional electrical testing of final devices by customer	Additional temperature cycling test Additional burn-in testing

Single-Event Effects

- **Upset of flip-flops and storage elements**
 - Single upsets can usually be handled with error correction.
 - Multiple-bit upsets are more difficult to deal with.
 - For highly scaled devices, a single ion can produce more than 100 upsets.
- **Functional interrupt (SEFI)**
 - “Scrambles” part of the device operation
 - Lower probability than ordinary upsets
 - Can be difficult to detect.
 - Increasingly difficult as chip designs become more complicated
- **Latchup**
 - Difficult problem because of high charge density of galactic particles
 - Less important for advanced low power designs with low voltage
 - Latchup holding voltage usually > 0.8 V
 - However, higher voltages occur at I/O nodes

Radiation hardening by design can reduce SEE effects

Penalties: high cost, much larger chip area.

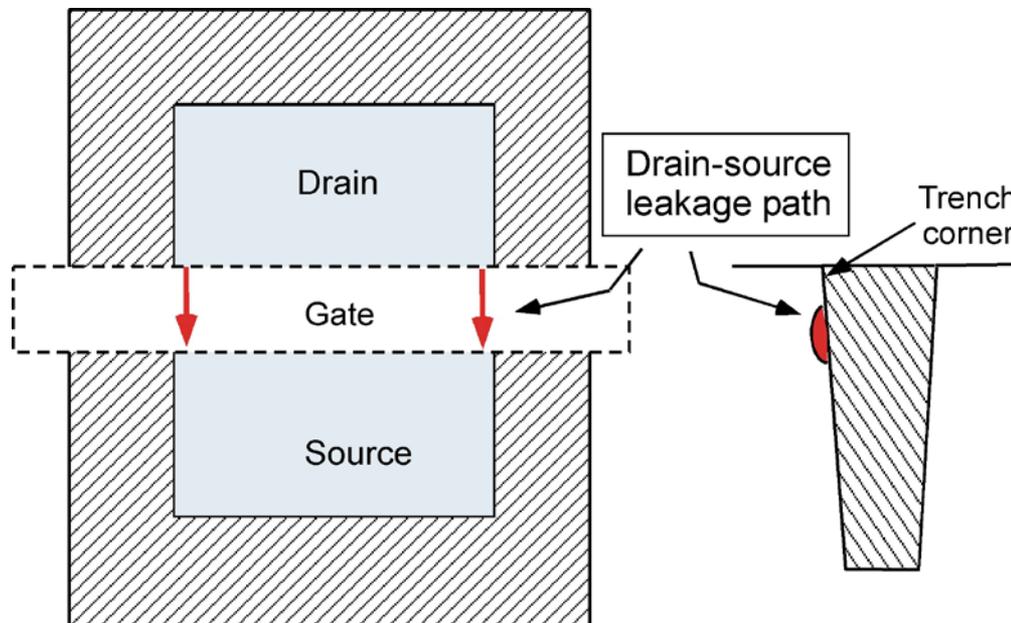
Single-Event Effects

- **Can only be described statistically**
 - Relatively constant probability for galactic cosmic rays
 - Governed by cross section for “ion hits”
 - Related to cell area and critical charge
- **Solar flares introduce another statistical layer**
 - Systems have to be designed to deal with the higher flux from a large flare.
 - Typically persists for about one day
 - Adds an element of conservatism to the effective error rate
- **Device scaling effects are complex**
 - Critical charge decreases with scaling, increasing susceptibility.
 - Device area is lower with scaling, decreasing susceptibility.
 - Collected charge is lower as voltage and area are reduced.

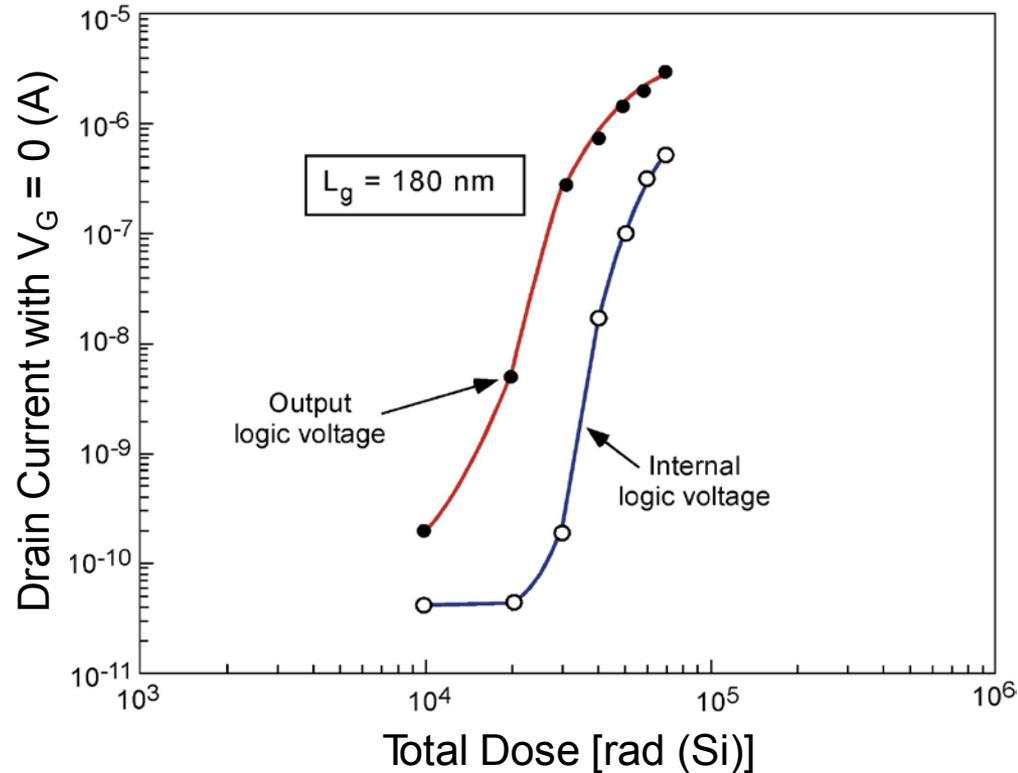
The net effect is that the upset rate – per cell – isn't affected very much. However, the upset rate per device increases because there are so many more devices on a chip.

Total Dose Damage and Scaling

- Total dose damage produces changes in gate threshold voltage.
 - Magnitude depends on the square of the oxide thickness.
 - Scaling has nearly eliminated its importance for advanced CMOS.
- Total dose also affects shallow trench isolation oxides.
 - Causes leakage current between source and drain
 - Also may affect isolation between transistors
 - This is potentially more important for ULP devices.



Trench Leakage vs. Total Dose



- ***Low power devices are more sensitive to the low source-drain leakage current that occurs after irradiation.***

Calculated Processor Upset Rates for Scaled Processors at Older Nodes

- Solar flares, proton upset effects will increase the actual upset rate

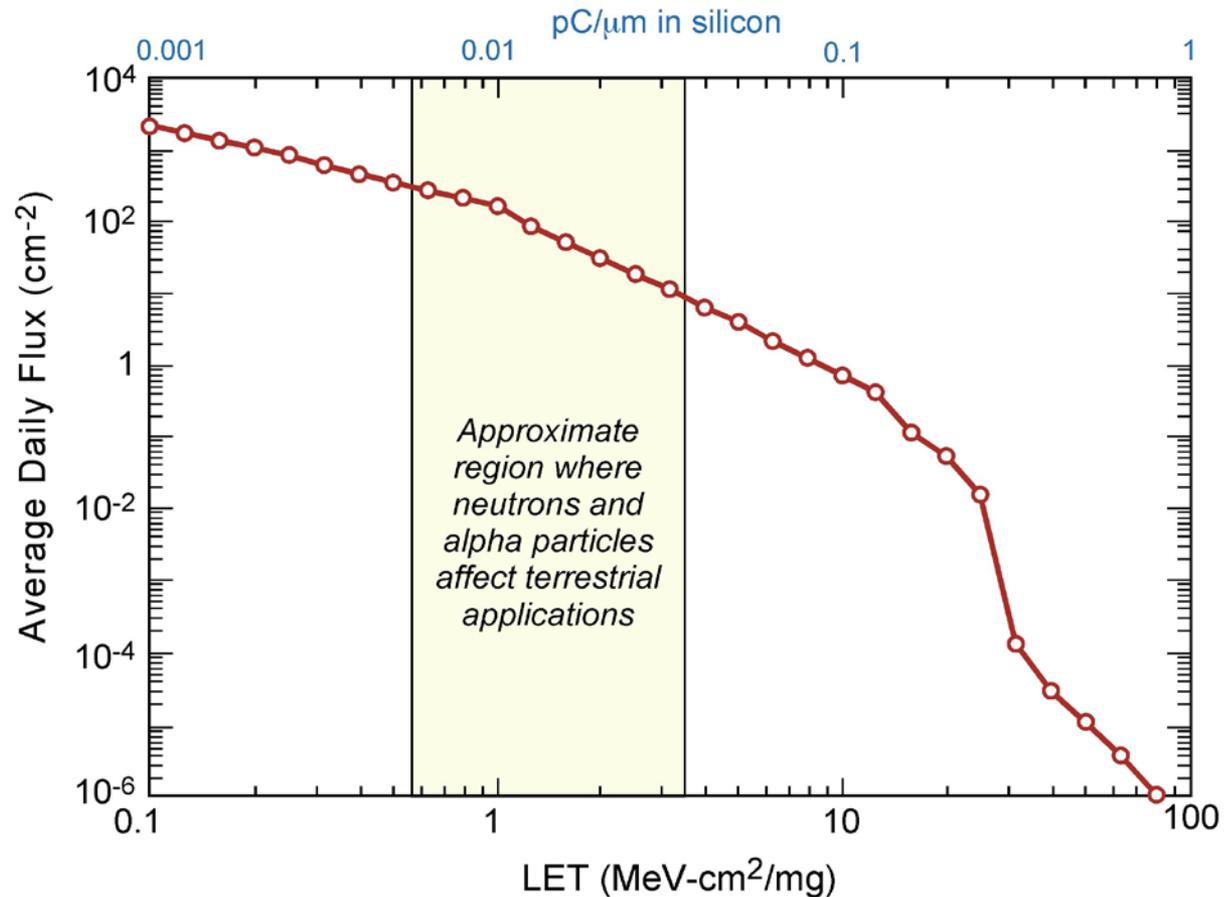
Processor Upset Rates from Galactic Cosmic Rays
(solar minimum*)

Technology	Processor	Feature Size (μm)	Calculation Errors (per year)	Crashes (per year)
Bulk (design hardened)	RAD6000	0.5	0.7	~ 0.2
Bulk (design hardened)	RAD750	0.25	2.5	~ 0.7
Bulk (commercial)	PC750	0.22	120	2.2
SOI (commercial)	PC7457	0.13	4	< 0.1

*Rates are 4X lower during solar maximum

Comparison with Terrestrial Soft Errors

- The deposited charge from galactic cosmic rays is about one order of magnitude higher than that of the particles producing conventional soft errors.
- Soft-error hardening by commercial manufacturers doesn't solve the problem in space.



Summary & Conclusions

- **ULP microelectronic architectures can significantly reduce the power required for digital processing.**
- **Overall load power reductions of 20-40% or more**
 - Reduces mass (can also reduce solar cell array size)
 - Increases power available for other function
- **ULP design impact on Reliability**
 - Lower supply voltages, but larger transistor area
 - Designs are more sensitive to temperature and statistical variations in threshold voltage.
 - Lower voltage and reduced power should improve reliability, as long as temperature and noise margin limitations can be accommodated.
 - Continue to Derate appropriately for space applications.
- **Only limited information is available on space radiation effects for ULP microelectronics.**
 - Work on conventional CMOS suggests that upset rates will be similar.
 - Total dose damage in isolation regions may be more important for ULP devices.

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