National Aeronautics and
Space Administration

Jet Propulsion Laboratory
California Institute of Technology
Pasadena, California

Scaled CMOS Reliability and Considerations for Spacecraft Systems: Bottom-up and Top-down Perspectives

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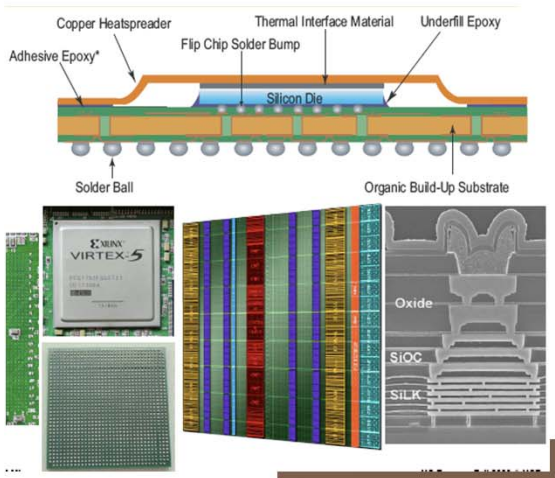
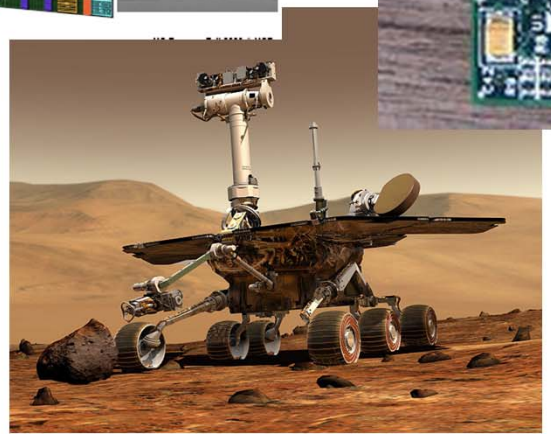
Purpose

- **Top-down system and bottom-up component reliability approaches should both be implemented for a robust, reliable spacecraft system design.**





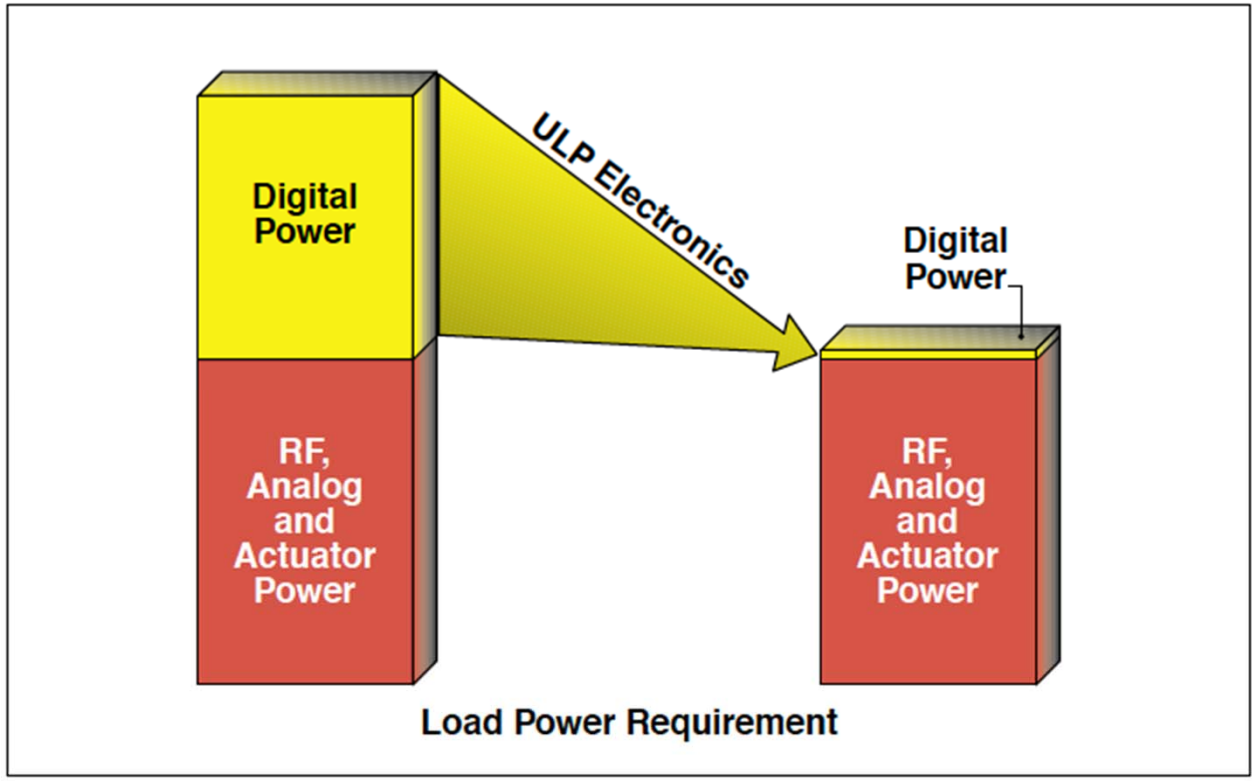
Outline

- Spacecraft Technology Developments
- Spacecraft Systems: Scaled CMOS Reliability Bottom-up Considerations
  - CMOS scaling trends
  - Variability issues with scaled ultra-low power CMOS devices
  - Front-end processing reliability issues
  - Back-end processing reliability issues
  - Screening and derating
- Spacecraft Systems: System-Level Reliability Top-down Considerations
  - Design margin and reliability analyses
  - Thermal margin stack-up
  - System design, thermal management and reliability
- Summary & Conclusions

Spacecraft Design

- Goals:
  - Reduction in system power requirements
    - Do more with less
  - Reduction in mass
    - Solar arrays
    - Spacecraft bus
    - Batteries
    - Heat sinks
  - Enhanced performance and capabilities
    - Computational enhancements
    - Data processing
    - Data storage

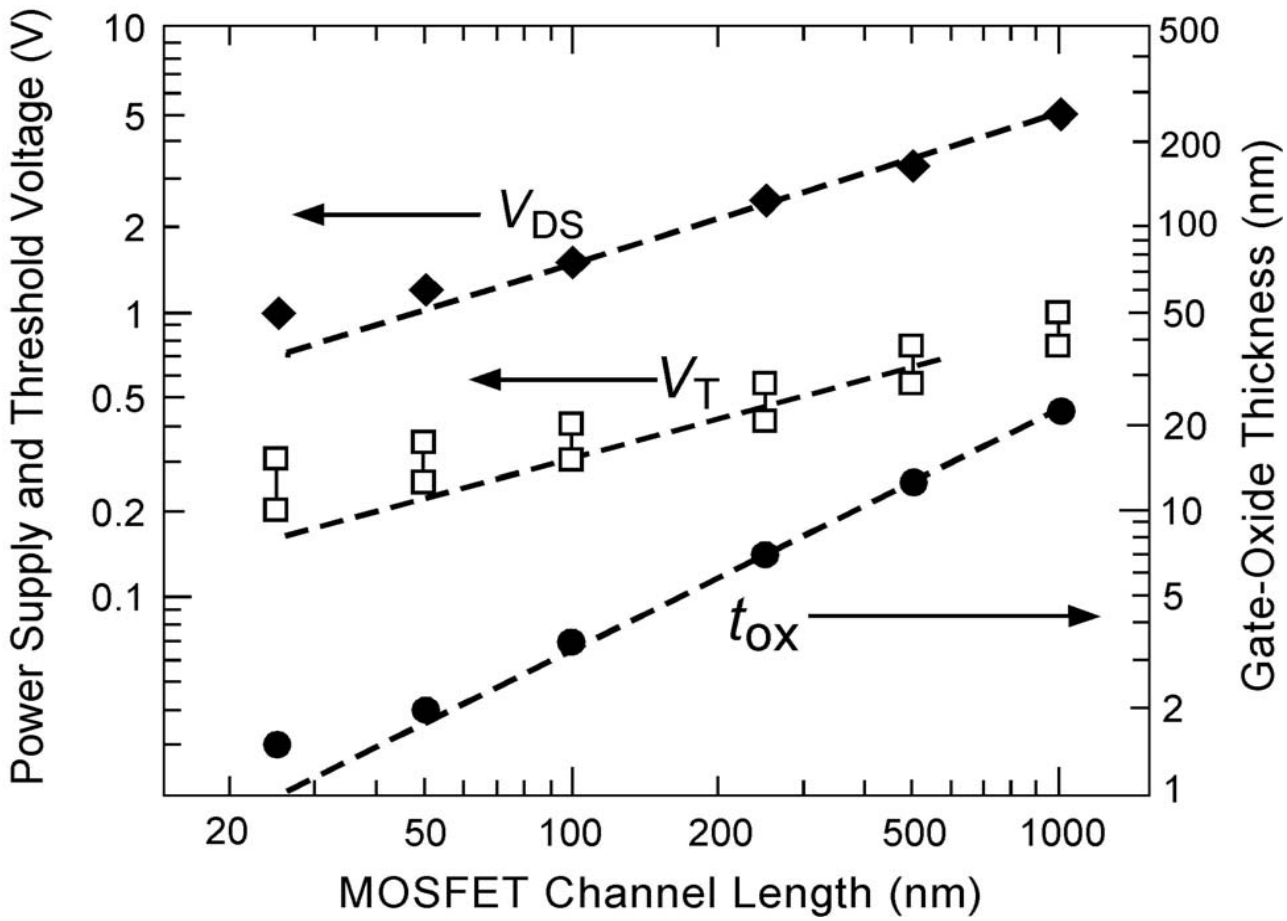
Spacecraft Design – Scaled ULP Benefits



- **Scaled CMOS ULP electronic architectures can significantly reduce the power required for digital processing.**
- **Load power reductions of 20-40% or more, resulting in mass savings or increased power available for other functions**

CMOS Scaling Trends

- **Scaling trends for power supply voltage, gate threshold voltage, and channel length**

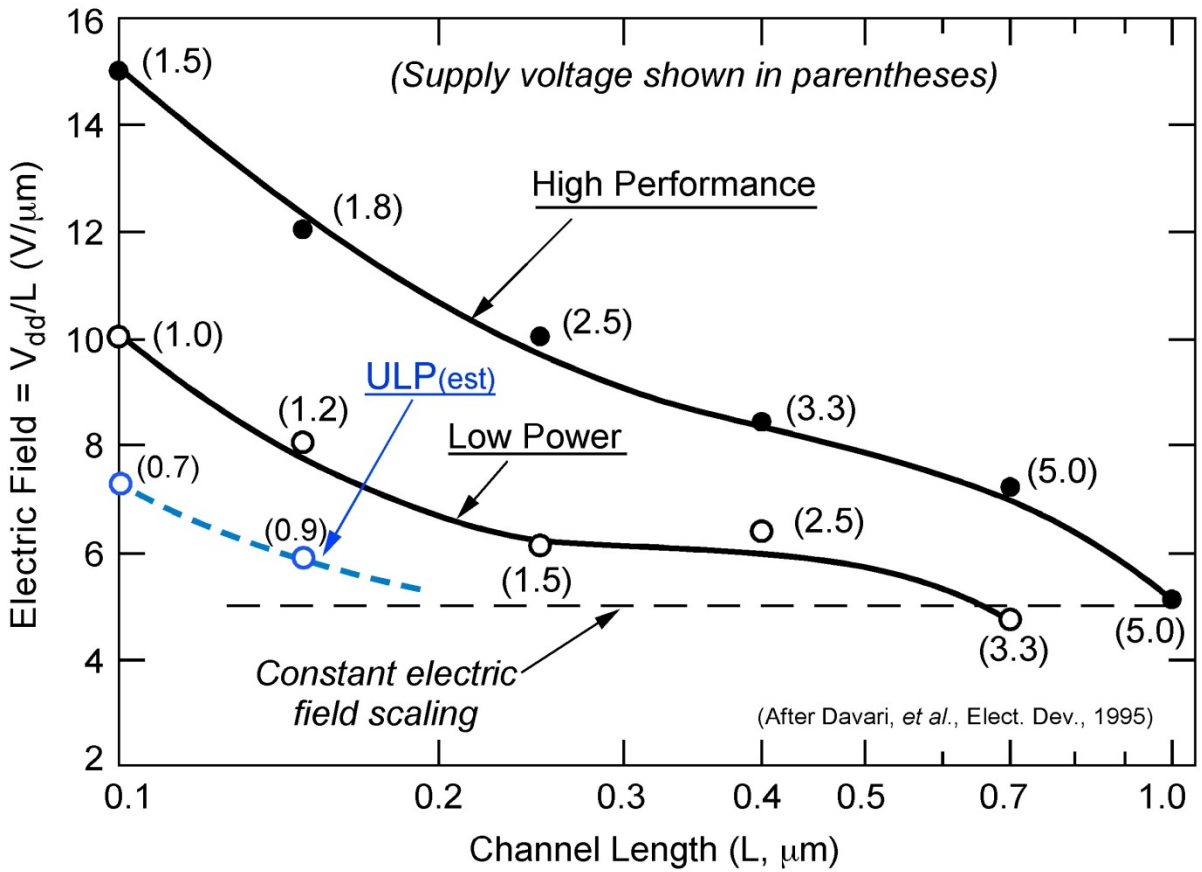


Y. Taur, et al., *1997*

CMOS Scaling Trends

Application	Primary Design Concerns	Power Supply Voltage	Gate Threshold Voltage	Reliability Issues
High performance	Switching speed	< 1 V	0.3	Electromigration Contact integrity
Mainstream	Maximum functionality density	1 to 1.2 V	0.4	Percent defect ratio of electrical test
Low power	Low total power dissipation	< 1 V	0.25	Percent defect ratio of electrical test
Memory	Low leakage and low standby current	3.3 V (internal back bias generator are often used to decrease leakage current)	0.5	Retention time for dynamic memories; early bit failures in large density SRAMs

CMOS Scaling Branches



- **Channel electric field is important for device scaling.**
- **Older studies considered high-performance and low power.**
- **ULP trends are compared in this figure with older work.**

B. Davari, et al., 1995

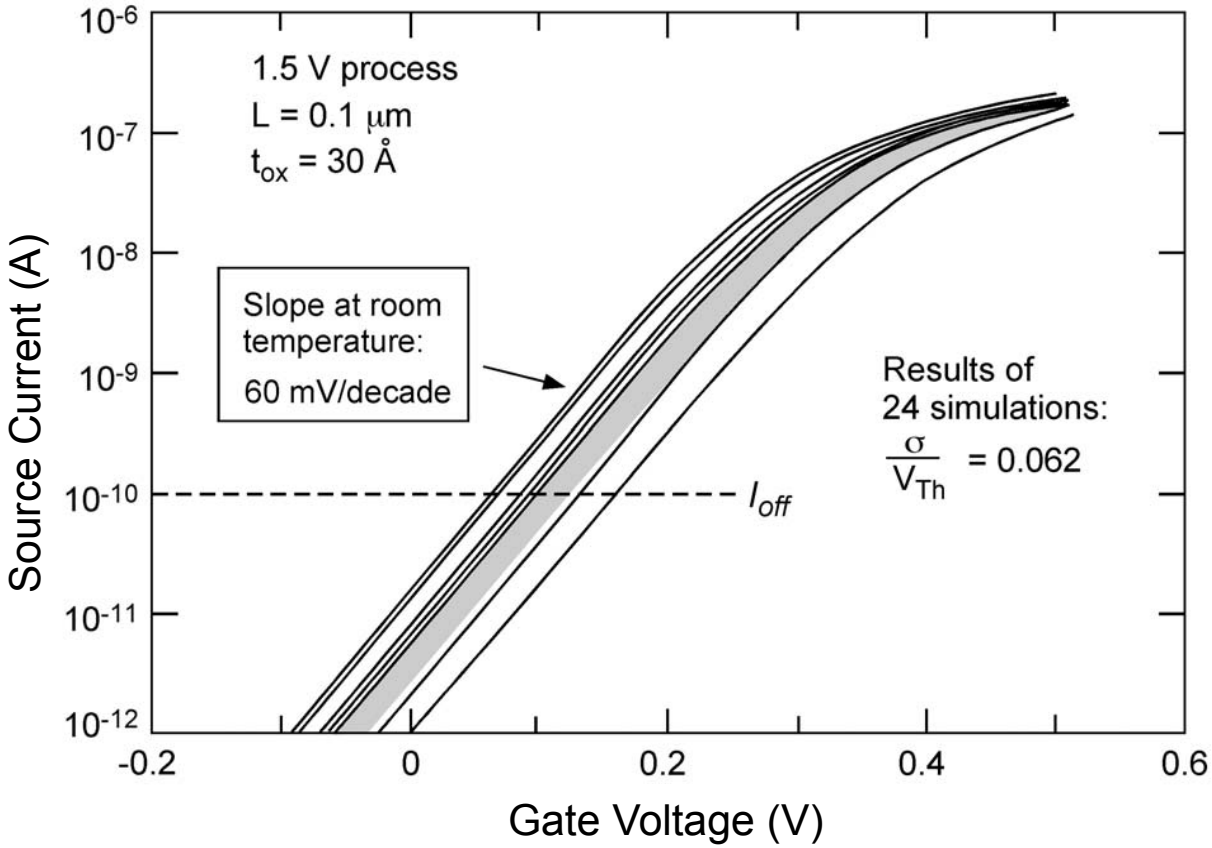
Variability Issues with Scaled CMOS ULP Devices

- **Process**
  - As CMOS scaling approaches the 25nm node, random threshold voltage (Vt) variation caused by statistical variation in the number of dopant atoms may lead to more than 100mV of Vt variation.
- **Voltage**
  - The voltage margin of Vt sensitive circuits, such as flip flop circuits that DRAMs use for sense amps and SRAMs use for cells, is reduced compared to higher power designs.
- **Temperature**
  - A temperature variation of 100°C could cause sub-threshold currents to increase more than four orders of magnitude.

- ***Each of these factors are accentuated at lower technology nodes and operating voltages.***

K. Itoh, et al., 2007

Statistical Fluctuations in Vth



- **Sub-threshold slope showing the effect of statistical fluctuations in threshold voltage on the on/off current ratio**
- **Reduces noise margin**
- **More severe at higher temperatures**

Y. Taur, et al, 1997

Reducing the Effect of Variability in Scaled CMOS ULP Devices

- **Redundancy and ECC**
  - Essential to avoid DRAM sense amp and SRAM cell failures caused by excessive intra-die Vt mismatches and to allow minimum Vdd for successful operations
  - On-chip ECC for repairing random defects
- **Symmetric Layouts for Flip-Flop Circuits**
  - Tight controls of channel length and width will help reduce Vt variation and Vt mismatch.
- **Control of Internal Supply Voltages**
  - Suppression of and compensation for variations of design parameters (Vt, Vdd, temperature) through controls of internal voltages with on-chip voltage converters
- **Optimize Power Supply Voltage**
  - Vdd must be kept sufficiently high to account for intra-die variations in Vt (and Vt mismatch) to minimize timing and voltage margin differentials.

K. Itoh, et al., 2007

Effects of Processing Variation on Reliability

Historical Process Variations	Emerging Process Variations
• Patterning proximity effects • Line edge and line width roughness • Surface roughness (polishing) • Variations in gate oxide thickness • Fixed charge and oxide traps	• Random dopant fluctuations • Variations in implants and anneals • Variations associated with strain • Gate material granularity

K.J. Kuhn, et al., 2011

- **Many of the historical issues have been solved by clever improvements in processing.**
  - **The difficulty of coping with corner rounding and geometrical limitations associated with lithography has been overcome by designing devices in pairs for feature sizes of 65 nm and below.**

Dominant Reliability Issues (FEOL)

- **Front-End Processing**
  - Random dopant fluctuations
  - Significant process changes to continue Moore's Law
    - Hafnium oxide metal gate transistors (< 65nm)
    - Strained crystalline structure (< 90nm)
    - Potential new failure mechanisms
  - TDDB, contact integrity, hot-carrier degradation

- **For Space Applications:**
  - Confirm manufacturer follows design rules and that their process technology provides adequate reliability margins.

Dominant Reliability Issues (BEOL)

- **Back-End Processing:**
  - **Metallization**
    - **Voids, grain boundaries, thinning of metallization over non-planar regions**
  - **Electromigration**
    - **Clock drivers and I/O circuits where higher currents are required**
    - **Vias in copper interconnects**
    - **Low-k dielectrics used in more advanced processes (metal can migrate within dielectric materials)**
  - **Packaging**
    - **More advanced packaging techniques (BGAs, PGAs, CGAs)**
    - **Stress risers at corner regions (cracking, intermittent or open contacts)**
    - **Non-hermetic plastic packaging (moisture transport)**
    - **Thermal expansion coefficient of the die and packaging**
- **For Space Applications:**
  - **Apply appropriate screening and qualification methodology for the application**
  - **Derate appropriately for space applications**

Relationship between Foundries & End-Manufacturers

Methods to obtain parts for space use through commercial foundries, the only option for highly scaled ULP processes:

- **Parts manufactured through working agreements with mainstream producers of hi-rel parts**
  - **Arrangement between foundry and producer depends on contracts between them**
- **Trusted foundries**
  - **Government establishes relationship between specific foundry and designers**
- **Parts produced on modified commercial processes**
  - **Changes are made to process for specific wafers or wafer runs used for hi-rel (often radiation-hardened processes)**

Tests & Evaluations for Scaled CMOS ULP Device Source Selection

Three distinct steps in the overall process of selecting and qualifying advanced Scaled CMOS ULP parts for space applications:

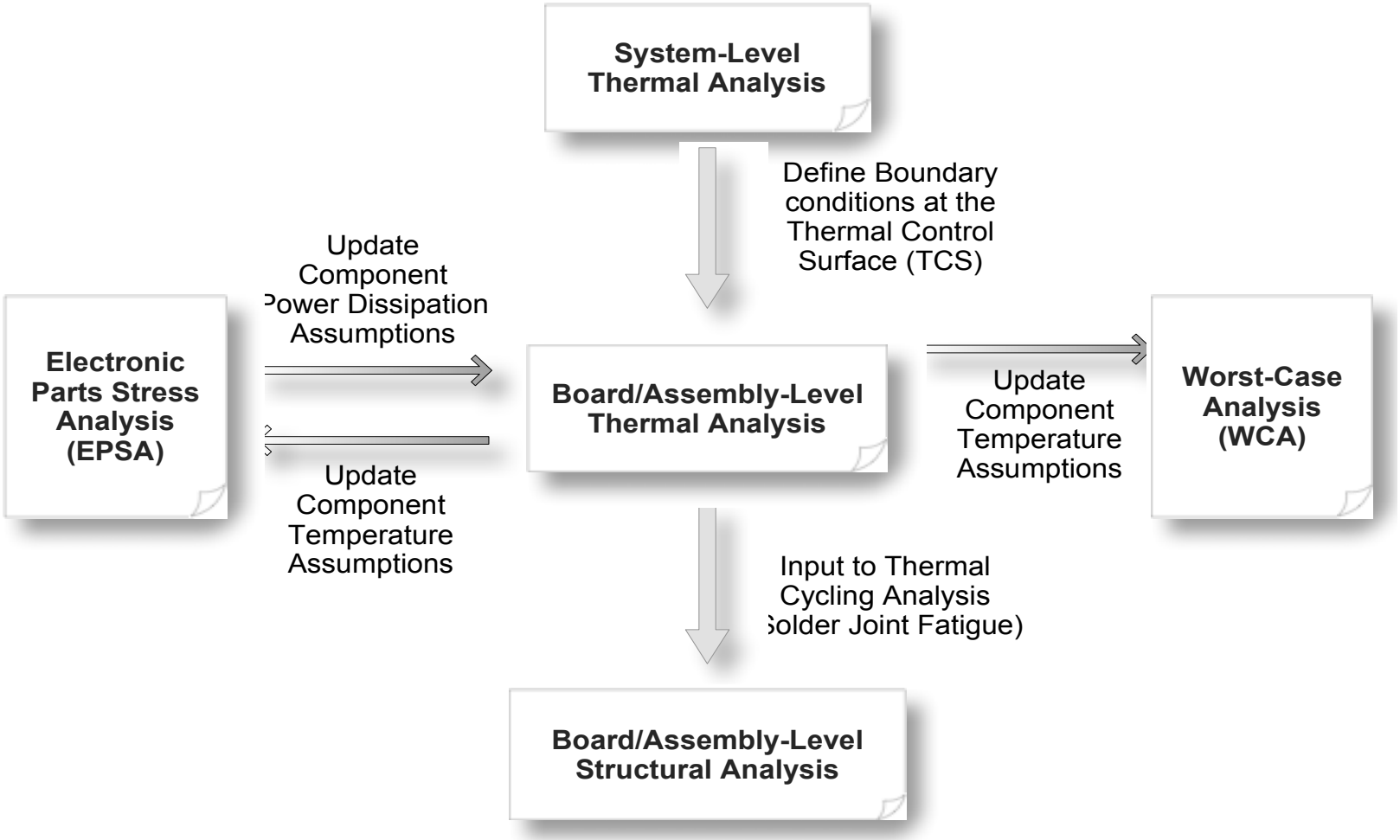
- **Establishment of source selection requirements for the mfr.**
- **Determination of qualification requirements for testing and evaluating parts produced by the process**
  - **May include monitoring process control or reliability test vehicles (generally destructive)**
- **Specific screening tests on final product includes tests directly related to circuit application and environmental requirements.**
  - **Applied to all flight parts, and must be done under carefully controlled conditions; cannot be destructive, but may result in elimination of some parts from flight lot that do not pass screening tests**

Tests & Evaluations for Scaled CMOS ULP Device Selection

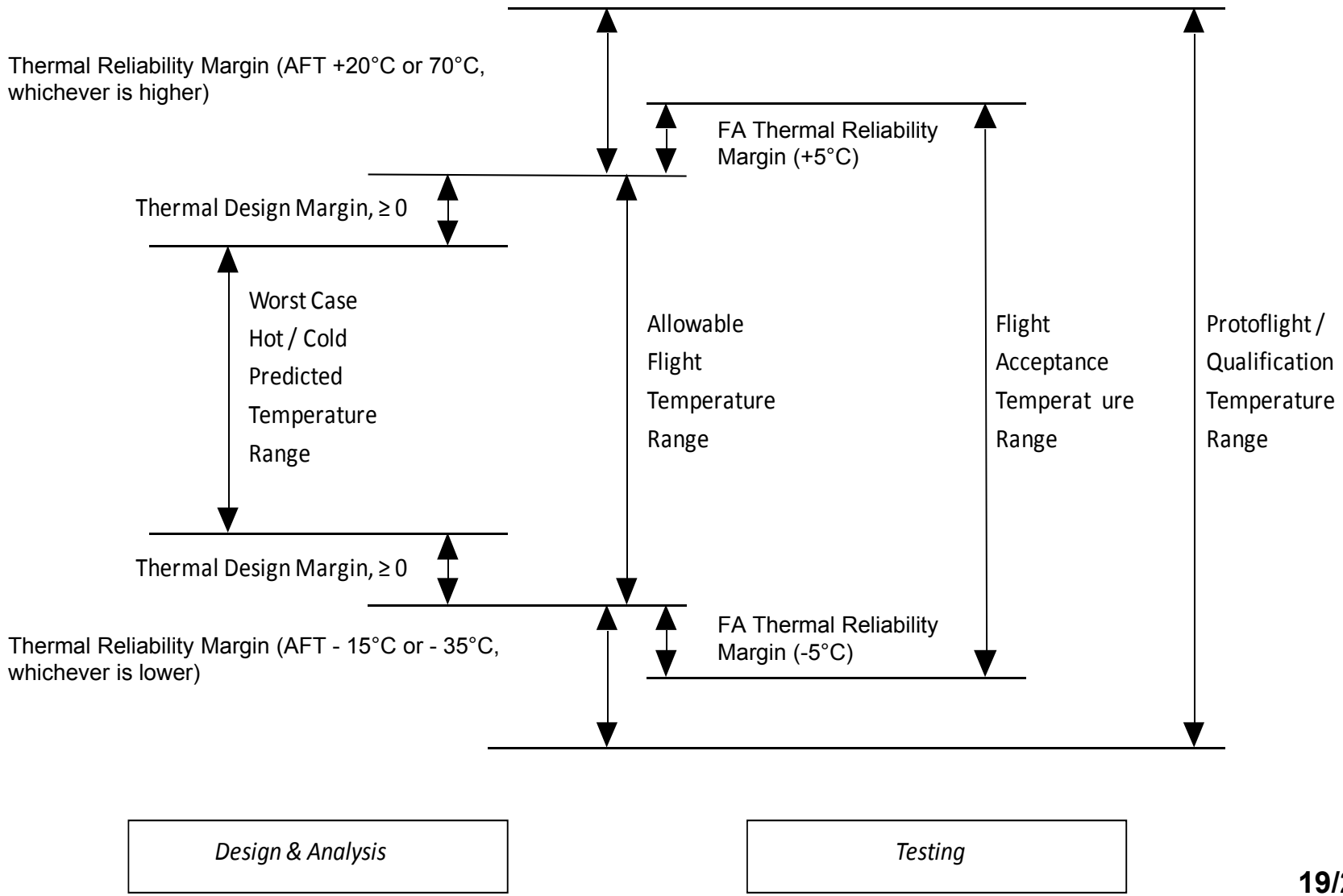
Mechanism	Approach Used by Vendor	Additional Steps and Processes for Space Use	Specific Screening Methods
Front-end processing	Specific failure mechanisms evaluated with test structures Statistical process evaluation	Review and track reliability data from vendor	None for this category
Back-end processing	Specific failure mechanisms evaluated with test structures (metallization, bonding and vias)	Review and track reliability data from vendor	None for this category
Packaging	Packaging yield and failure mechanisms	Review and track reliability data from vendor Construction analysis	Additional temperature cycling tests
Overall process reliability	Yield of final product (relative values may be adequate for this evaluation)	Evaluation and additional electrical testing of final devices by customer	Additional temperature cycling test Additional burn-in testing

Design Analyses Information Flow

- **Commonly performed reliability analyses are Thermal Analysis (TA), Electronic Parts Stress Analysis (EPSA), Worst-Case Analysis (WCA), Board Level Structural Stress Analysis, and Reliability Design Estimates.**

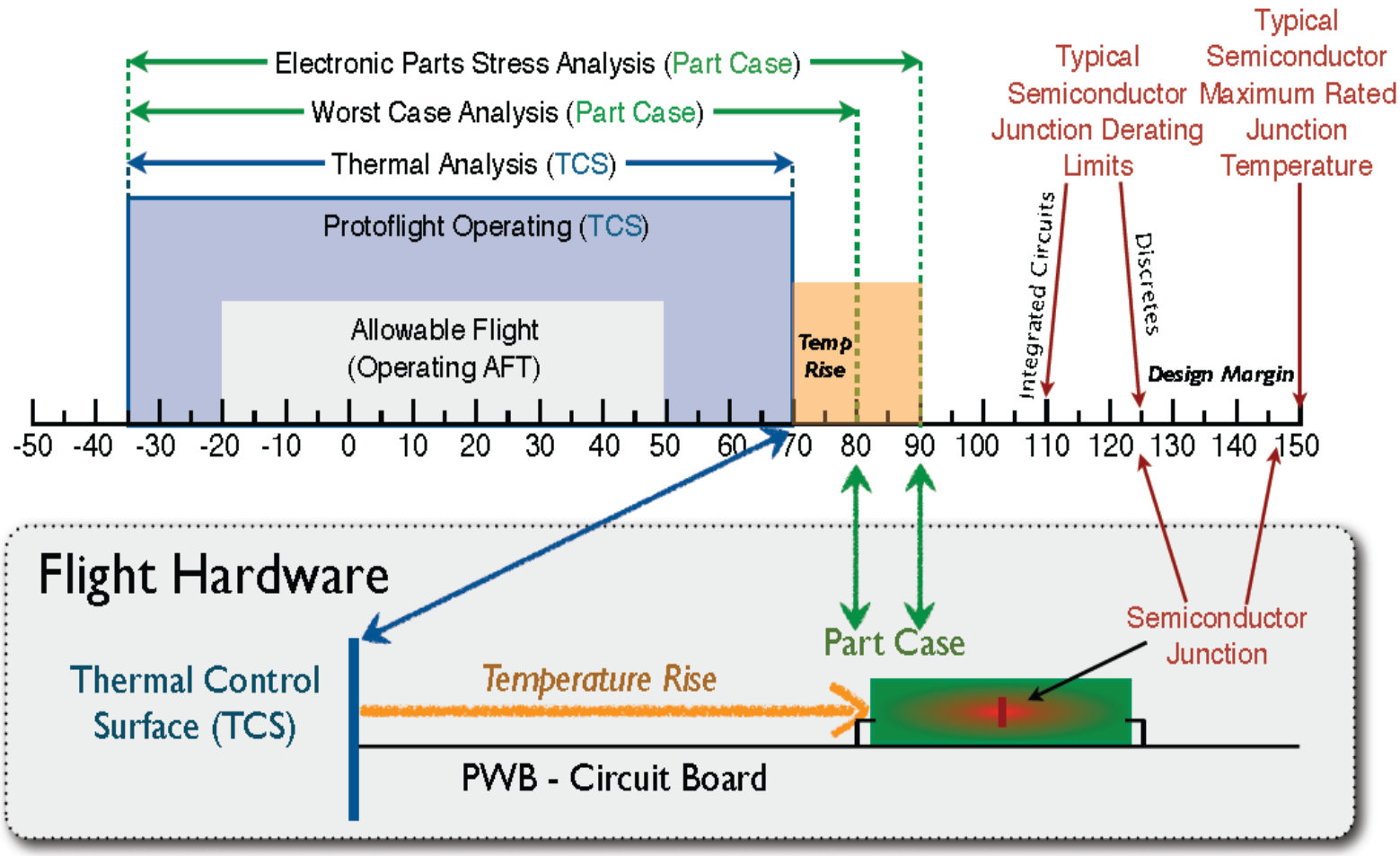


System-Level Reliability and Qualification Margins (Example)



Integrated Thermal Margins

- **System design margin must be considered in aggregate**
- **Margin is cumulatively stacked to comprise a robust system design to improve reliability and reduce uncertainty**



System Design, Thermal Management and Reliability

- System reliability can largely be improved through optimized thermal management and a deep understanding of the anticipated operating environment.
  - Operating stresses on components
  - Material properties and their behavior over temperature
  - Potential failure mechanisms and physics-of-failure
  - Maintaining adequate process controls at all levels
  - Analyzing past performance data (screening, qualification, and lot-to-lot variability)
  - Understanding performance degradation at steady state temperatures and/or extended thermal cycles
  - Designing in adequate thermal margins to account for uncertainty

Summary & Conclusions

- New space missions will increasingly rely on more advanced technologies because of system requirements for higher performance, particularly in instruments and high-speed processing.
- Component-level reliability challenges with scaled CMOS in spacecraft systems from a bottom-up perspective have been presented.
- Fundamental "Front-end" and "Back-end" processing reliability issues with more aggressively scaled parts have been discussed.
- Effective thermal management from system-level to the component-level (top-down) is a key element in overall design of reliable systems.
- Thermal management in space systems must consider a wide range of issues, including thermal loading of many different components, and frequent temperature cycling of some systems.
- **Both perspectives (top-down and bottom-up) play a large role in robust, reliable spacecraft system design.**