Total Dose Effects on Bipolar Integrated Circuits at Low Temperature

A. H. Johnston, *Fellow, IEEE*, R. T. Swimm, and D. O. Thorbourn

***Abstract* – Total dose damage in bipolar integrated circuits is investigated at low temperature, along with the temperature dependence of the electrical parameters of internal transistors. Bandgap narrowing causes the gain of npn transistors to decrease far more at low temperature compared to pnp transistors, due to the large difference in emitter doping concentration. When irradiations are done at temperatures of -140 °C, no damage occurs until devices are warmed to temperatures above -50 °C. After warm-up, subsequent cooling shows that damage is then present at low temperature. This can be explained by the very strong temperature dependence of dispersive transport in the continuous-time-random-walk model for hole transport. For linear integrated circuits, low temperature operation is affected by the strong temperature dependence of npn transistors along with the higher sensitivity of lateral and substrate pnp transistors to radiation damage.**

***Index terms* - linear integrated circuits, low temperature, space radiation, total dose effects.**

I. Introduction

Certain types of space missions require that microelectronics operate at temperatures well below the normal design range considered by commercial manufacturers. One example is exploration of the Martian surface, where the latest spacecraft – Curiosity – will be able to operate during night-time darkness, because of on-board nuclear power generators. Other missions with cold temperature requirements include exploration of the polar regions of the moon, and missions to asteroids. Because there are no trapped belts, solar flares are the dominant source of radiation for those missions.

This paper investigates the performance of bipolar integrated circuits at low temperature, including combined effects of reduced temperature and radiation damage. Although there are missions where devices remain at low temperature for extended periods after they are exposed to radiation, for Mars surface exploration the temperature will remain low for only about 15 hours, about ½ the length of a Martian day (24.7 hours). Thus, we have two concerns: how does a relatively intense flare affect device performance, and how does the integrated effect of many flares over a complete solar cycle affect performance at low temperature over the mission lifetime?

The research in this paper was carried out at the Jet Propulsion Laboratory, California Institute of Technology, under contract with the National Aeronautics and Space Administration (NASA).

The authors are with the Jet Propulsion Laboratory, California Institute of Technology, Pasadena, CA 91109. E-mail allan.h.johnston@jpl.nasa.gov; randall.t.swimm@jpl.nasa.gov; dennis.thorbourn@jpl.nasa.gov.

The total dose for missions in deep space or Mars surface exploration is dominated by the few intense flares that may occur during deployment. The dose rate for intense flares is on the order of 0.05 to 0.1 rad(SiO_2)/s [1]. Thus, radiation tests for these applications can be done at somewhat higher dose rates than for missions in LEO orbits, where total dose is dominated by transits through the South Atlantic anomaly region of the earth's trapped proton belts.

II. Characteristics of Typical Bipolar Devices

A. Oxide Properties

Oxides in bipolar devices serve two purposes: passivation of the underlying silicon region, and screening of dopants during fabrication. Much thicker oxides are required for the mainstream process used in linear bipolar circuits – intended for voltage applications up to ±18 V – because the n-pocket isolation step early in the process requires boron diffusion to a depth of about 12 µm. After subsequent processing steps, the thick oxide remains over the emitter-base junction of lateral and substrate pnp transistors, but not the npn transistors. Typical oxide thicknesses are shown in Table 1. Note that much thinner oxides are present in high-speed linear ICs, with lower voltage ratings.

Table 1. Typical Oxide Thicknesses of Bipolar Devices

Technology	Voltage Rating	t_{ox} (µm)
Discrete bipolar transistor	Various	0.2 – 0.3
Mainstream Linear IC	±18 V	0.7 – 0.8 (pnp) 0.15 – 0.25 (npn)
High-speed Linear IC	5 V	0.15 – 0.3

A scanning electron microscope was used to measure the thick oxides in two of the circuits types used in this study. The National LM111 had an oxide thickness of 0.71 µm; the oxide thickness of the Analog Devices OP27 was 0.65 µm.

B. Doping Levels

Doping levels affect radiation sensitivity as well as temperature effects. The doping profile of substrate pnp transistors from two manufacturers of the LM111 comparator are shown in Fig. 1.

Although it is not shown in the figure, the emitter doping level of the npn transistor in that process is > 10^{20} cm^{-3}. The large difference in emitter doping of the pnp and npn transistors affects the temperature dependence of gain, increasing the sensitivity of the npn transistor to temperature compared to that of the pnp transistors.

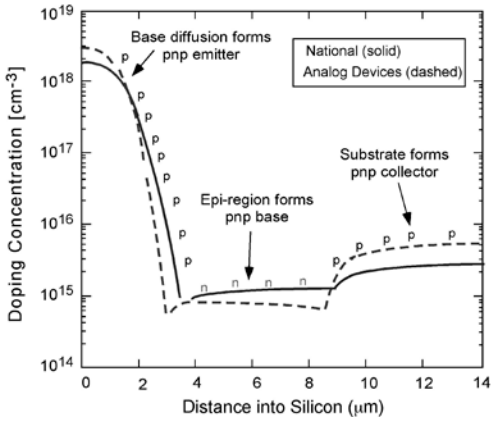

Fig. 1. Doping profiles of LM111 substrate transistors.

The low emitter doping concentration is the result of the "compromise" approach for fabrication of pnp transistors without adding additional processing steps. Not all bipolar ICs are fabricated that way (e.g., the XFCB process from Analog Devices [2]), but the older processing method is still widely used because of low cost and flexible use conditions over a wide voltage range.

III. Temperature Dependence (Experimental)

A. Basic Transistors

The dependence of gain on temperature for substrate pnp, lateral pnp, and vertical npn transistors from a National LM111 comparator is shown in Fig. 2 over a much wider temperature range than that considered by the manufacturer. The substrate pnp gain decreases only about 30% at low temperature, while the npn gain decreases more than a factor of ten at -160 °C. The lateral pnp transistor gain shows a slight increase at lower temperature, but changes far less than the npn transistor.

Although lateral pnp transistors have a stronger temperature dependence than the substrate transistor, they are usually used in circuit blocks that are less dependent on gain compared to the other two transistor types, partly because of the difficulty of optimizing its performance.

Thus, the decrease in npn gain is usually the dominant factor in determining how a specific circuit will operate at temperatures below the normal operating range.

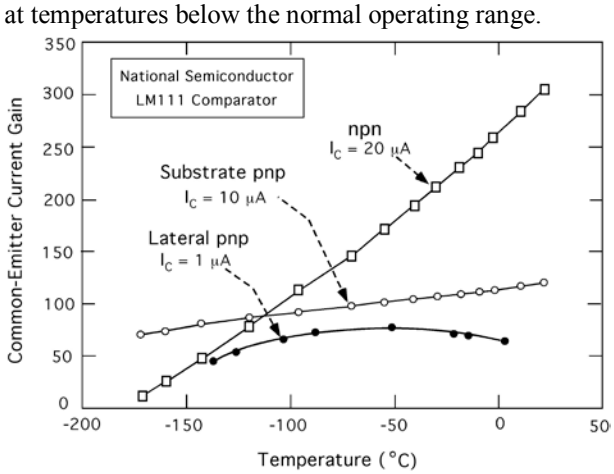

Fig. 2. Typical dependence of gain on temperature for the substrate pnp, lateral pnp, and second-stage npn transistor of the LM111 comparator.

B. Circuit Properties

The behavior of circuits at low temperature varies widely, depending on the design of sub-circuit elements. Three basic circuits will be considered in this paper.

LM111 Comparator. Input bias current is the parameter that is most affected by temperature. Non-standard measurements of input bias current were made, applying a small offset voltage to separate the pnp transistors from the loading effects of npn transistors in the second stage (see Ref. 3). Figure 3 shows that the device continues to function normally down to -165 °C; it ceases to operate at lower temperatures because the very low gain of the second-stage npn transistors require more current than the input (substrate pnp) voltage follower can provide. Note that the power supply current remains relatively constant over this extended temperature range.

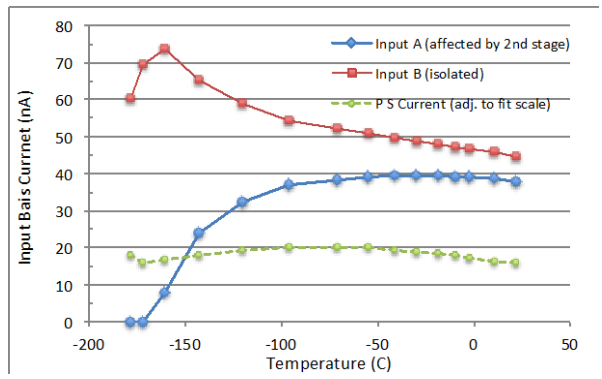

Fig. 3. Effect of temperature on input bias current and power supply current of the LM111 comparator.

Only small changes were observed in input offset voltage, even at -160 °C. Thus, this part can be used at unusually low temperature with only moderate derating of input parameters.

OP-27 Op-Amp. More complex behavior is observed for other circuit types. A realistic comparison of their low-temperature performance should be benchmarked to their specifications, not just overall functionality. The OP27A (which uses a compensated input stage) is a precision op-amp with specification limits for input bias current below 100 nA over the MilSpec temperature range (-55 to 125 °C). The dependence of input bias current on temperature is shown in Fig. 4; it continues to function at -160 °C, similar to the low temperature behavior of the LM111.

However, the power supply current decreases by a relatively large amount at low temperature. Figure 5 compares the temperature dependence of that parameter for the OP27 and the LM111. It is apparent from these results that the OP27 is being "starved" at low temperature. This is due to the design of the input compensation and current sources of that circuit, which use npn voltage followers to couple internal currents [4]. Although that approach is adequate over the MilSpec temperature range considered by the manufacturer, the npn gain is about an order of magnitude lower at the very low temperatures we are considering here.

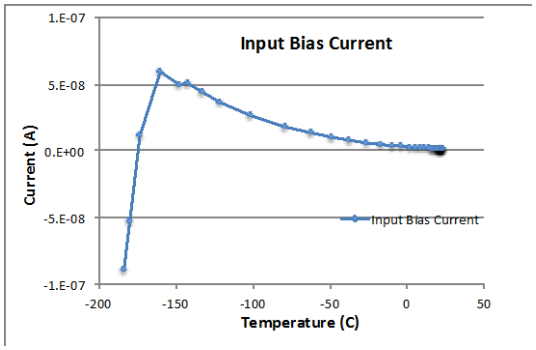

Fig. 4. Dependence of OP27 input bias current on temperature.

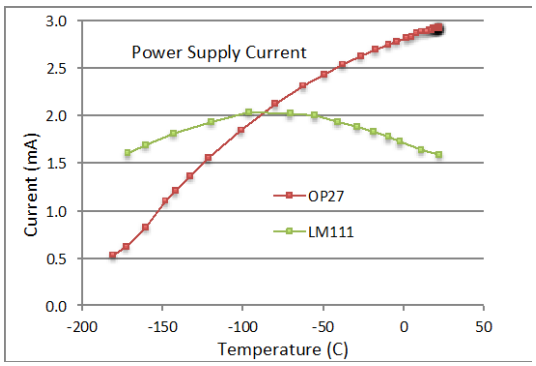

Fig. 5. Temperature dependence of the power supply current of the LM111 comparator and the OP27 op-amp.

LM117 Voltage Regulator. The most important parameter of the LM117 voltage regulator is the internal bandgap reference, because the output voltage scales with that parameter. Output current drive is also affected, but can be accommodated by de-rating the maximum allowable load current in circuit applications.

Although small changes occur in reference voltage as the temperature changes between -100 and -150 °C, the most prominent characteristic is a sharp decrease at about -160 °C, shown in Fig. 6. It is caused by the specific design of the internal bandgap reference circuit, which can no longer function properly when the npn transistor gain falls below a value of about 30.

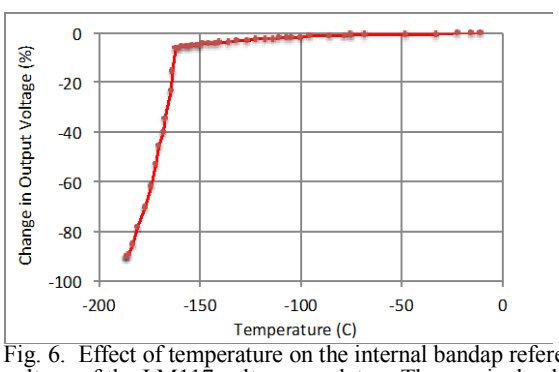

Fig. 6. Effect of temperature on the internal bandap reference voltage of the LM117 voltage regulator. The nominal value at room temperature is 1.25 V.

IV. Mechanisms for Temperature Dependence

A. *Temperature Dependence of Internal Transistors*

The effects of temperature and radiation damage on pnp and npn transistors in the basic linear IC process are distinctly different. Substrate and lateral pnp transistors are inherently more sensitive to radiation damage, while npn transistors are more sensitive to temperature. For applications near -150 °C, the large decrease in npn gain at low temperature can produce changes in key device parameters that are often more important than radiation damage. Thus, specific circuit designs have to be considered for applications in radiation environments at low temperature.

Bipolar transistors with advanced processes can operate satisfactorily at much lower temperature [5], providing an alternative but much more expensive approach for operation at low temperature (custom circuits or ASICs need to be developed). Circuits fabricated with mainstream linear processes are still important because of their low cost, as well as the availability of a wide range of circuit functions.

Although it was initially debated, the temperature sensitivity of conventional npn and pnp transistors has been attributed to bandgap narrowing, which is caused by band tailing and subsequent modification of the density of states in the material. [6]. It effectively increases the equilibrium carrier concentration. For an emitter doping concentration of 10^{20} cm^{-3}, the bandgap is reduced by about 100 mV (at room temperature). It depends logarithmically on carrier concentration. The lower emitter doping in lateral and substrate pnp transistors in mainstream linear circuit processes (Fig. 1) nearly eliminates that effect for those transistors.

V. Radiation Damage and Low Temperature

A. *Basic Considerations*

The effect of temperature on total dose damage has been examined in considerable detail for older oxides used in MOS transistors, particularly at high field [7]. Although these effects will be revisited in Section VI., it is useful to provide an overall picture of what is expected for thick oxides at low fields before examining experimental results. We will begin with effects in oxides, and extend those results to the bipolar devices that are the subject of this study.

Effects in Silicon Dioxide

For charge trapping in SiO_2, four processes are involved:

Initial recombination, which eliminates most of the electron-hole pairs under the low-field conditions that apply to these thick oxides.

Charge transport, which has been found to be well described by the continuous-time-random-walk (CTRW) model [8]. This process is highly dispersive, extending over more than ten orders of magnitude. The characteristic time depends on temperature; as a result it is one of the most important factors in temperature dependence.

Charge trapping, which can take place near the interface between the silicon and silicon dioxide interface region, but may also be present in the bulk region or in border traps [9]. The latter are located much further from the localized region near the interface than conventional hole traps.

Annealing, which occurs through a tunneling process for conventional traps near the interface region.

Effects in Bipolar Transistors

For the types of bipolar transistors addressed in this work, charge within the bulk region of the oxide has little effect (except for special gated transistors). Transistor gain is only affected when the charge generated in the oxide region produces traps near the surface [10]. This mechanism increases the surface recombination velocity, decreasing transistor gain.

Previous work using relatively short pulses of electrons has shown that damage in bipolar transistors depends on temperature, and that the damage actually builds up long after the initial pulse is over (the delay is about 1000 seconds for a 700 nm oxide, irradiated at -25 °C) [3]. These results are consistent with the CTRW charge transport model [11], along with the assertion that charge within the bulk region of the oxide does not affect transistor gain.

Expectations for Low Temperature Irradiation

The mechanisms described above suggest that initial recombination, which has been investigated to only a limited extent at low fields, and charge transport are the most important factors. The experiments done at low temperature were planned to help resolve those issues.

B. Lateral PNP Experiment at -140 °C

To investigate effects at much lower temperatures, we irradiated an isolated lateral pnp transistor from the LM111 process at -138 °C. The irradiation was done with all pins grounded, using cobalt-60 gamma rays at a dose rate of 10 rad(SiO_2)/s to a dose of 8.5 krad (SiO_2)/s. The top curve in Fig. 7 shows the initial temperature dependence before irradiation. Measurements done approximately 5 minutes after the irradiation showed that no change in gain occurred! This is consistent with the temperature dependence of thick oxides in the CTRW model [12] (which predicts that almost no hole will be transported to the interface at that temperature) as long as additional holes that are present in the bulk region of the oxide after irradiation do not affect the gain.

After the irradiation, the device was gradually warmed. Periodic gain measurements were made, shown in the middle curve. Only slight changes took place until approximately -30 °C. As the temperature increased further, additional damage was observed.

Following the warm-up cycle, the device was cooled again. As shown in the dashed line, significant damage occurred at all temperatures, even at the very low temperature where no damage was observed after irradiation. This is an important result. It shows that damage only occurs at higher temperatures, and supports our assumption in last year's paper that damage in these bipolar devices does not occur until holes have transported through most of the oxide.

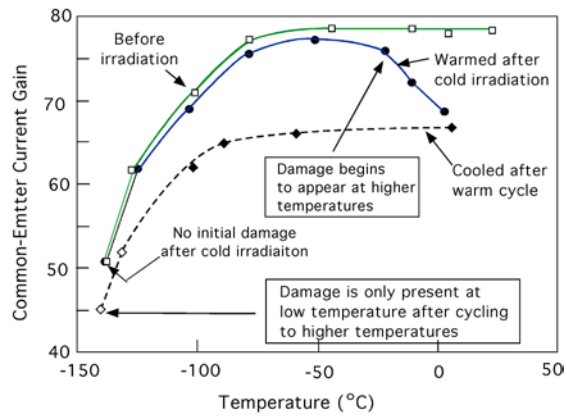

Fig. 7. Results of an experiment where the irradiation was done at low temperature, cycling the part to higher temperatures after irradiation, and then back to low temperature. The damage remains "locked in place" until the part reaches temperatures above -50 °C.

Further insight is provided when we compare the results of a room-temperature irradiation at the same dose rate and total dose with the irradiation at low temperature (Fig. 8). The gain comparisons are made at room temperature. It is apparent that far less damage occur for the low-temperature irradiation.

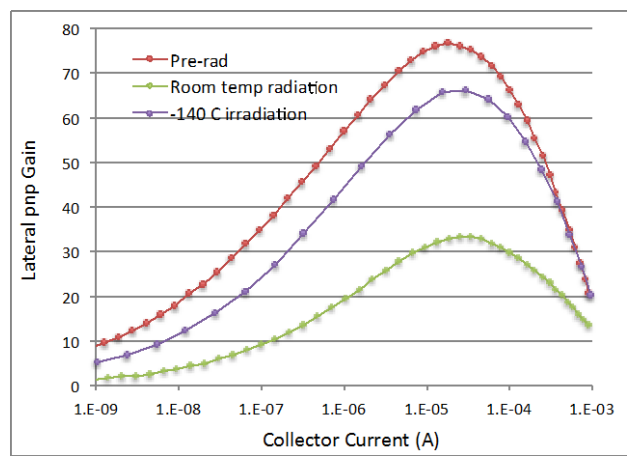

Fig. 8. Comparison of the gain reduction at 8.5 krad(SiO_2) of lateral pnp transistors irradiated at low temperature and at room temperature. The comparisons are made using gain at room temperature.

Integrated circuit comparisons are often made by comparing changes in input bias current [13], essentially the change in base current for a transistor that operates at constant current. The ratio of the change in base current of the lateral pnp transistor near the "beta peak" current in Fig. 8 is 8.2; this can be interpreted as a reduction in damage by that same factor when the irradiation is done at very low temperature.

C. Low Temperature Results for the LM111 Comparator

The LM111 was tested by irradiating the device with cobalt-60 gamma rays at -35 °C. The dose rate for those tests was 0.005 rad(SiO_2)/s, a condition where low dose-rate tests at room temperature no longer depend on dose rate.

The irradiation temperature was selected because it was within the rated temperature range for guaranteed performance by the manufacturer, and sufficiently below room temperature to determine whether the much longer charge transport times for holes would affect results at low dose rate.

Test results are shown in Fig. 9, comparing them with tests at the same dose rate at room temperature (the room temperature results were published previously [3]. The most obvious effect of the lower temperature was decrease in the slope of the damage (assuming linearity). The slope at low temperature is about 60% of the slope for room temperature irradiation. There are subtle differences at low total dose levels for room temperature irradiation, which are caused by the difference in dose-rate sensitivity of npn and pnp transistors.

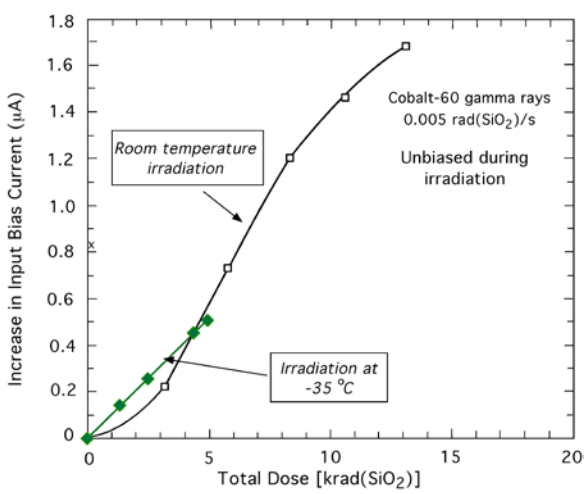

Fig. 9. Test results for the LM111 comparator at -35 °C and room temperature at low dose rate.

Although the effect of temperature on damage is less pronounced than for the lateral pnp irradiations, done at much lower temperature, the same trend towards less damage at reduced temperature is observed.

D. Low Temperature Results for the OP27 Op-Amp

Evaluation of the OP27 op-amp was done by cooling samples that had previously been irradiated to 40 krad (SiO_2) at room temperature. When the samples were initially irradiated to 40 krad(SiO_2) at room temperature, sufficient annealing took place over about 12 hours so that the net change in input bias current was five times less than the value immediately after irradiation [3]. It recovered almost completely after two days. For this device, the input current depends on the internal compensation circuit, which uses lateral pnp transistors that provide a bucking current that is vey nearly equal to that of the input npn transistor base current.

Even though the large initial changes in I_b recovered almost completely, the large changes observed just after irradiation show that the operating headroom of the input circuit was reduced by radiation damage. Tests of their performance at low temperature after the initial damage recovered evaluate how the stable component of the damage, which doesn't anneal, will affect performance at reduced temperature.

When those devices were cooled the compensation currents of the two inputs continued to track closely to temperatures of about -100 °C, but became severely mismatched at lower temperature. This is shown in Fig. 10, along with the power supply current, which drops to very low values at low temperature.

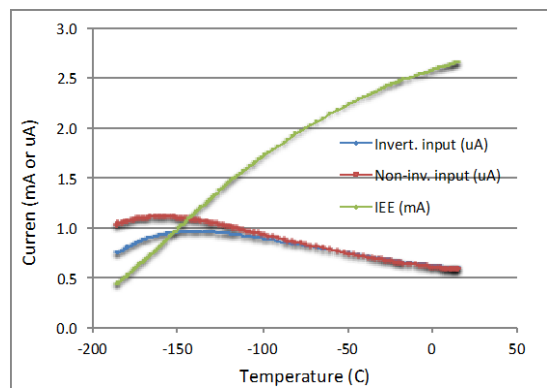

Fig. 10. Effect of temperature on input compensation current and power supply current of the OP27 op-amp after irradiation to 40 krad(SiO_2). Low-temperature properties were nearly identical to un-irradiated parts due to the strong falloff of npn transistor gain at low temperature.

These results show that radiation damage has a more pronounced effect on low-temperature performance of the OP27 compared to the LM111, which uses a more basic circuit design. Although the OP27 appears to work satisfactorily at temperatures within its normal rating, the complex design of the input compensation circuit limits its performance at the much lower temperatures we are considering in this paper.

E. Low Temperature Results for the LM117 Voltage Regulator

Low temperature performance of the LM117 voltage regulator was also done by evaluating devices that had been previously irradiated at room temperature at lower temperature. Radiation damage has a much larger effect on low temperature circuit characteristics of the LM117 reference voltage, as shown in Fig. 11. After exposure to 20 krad(SiO_2), the "knee" region decreases from about -162 °C before irradiation to about -120 °C at 10 krad(SiO_2). Smaller changes occur at lower total dose levels; consequently this device can be used for surface exploration missions with relatively small performance degradation where the total dose is below approximately 10 krad(SiO_2), but limits applications at higher levels.

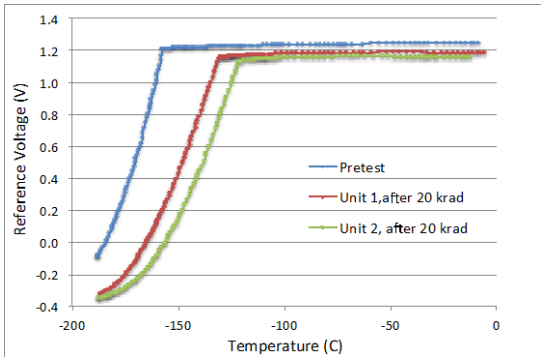

Fig. 11. Total dose damage effect on internal reference voltage of the LM117 voltage regulator. The device was irradiated at low dose rate with all pins grounded.

The classic bandgap reference circuit uses npn transistors [14]. Its performance depends on maintaining relatively high gain for npn transistor, which is effective over the standard -55 to 125 °C temperature range. More complex designs are used in the LM117, providing improved performance compared to the basic circuit, but the relatively poor performance of irradiated devices at lower temperatures is consistent with the strong falloff of npn transistor gain in that temperature range.

VI. Discussion

A. Initial Recombination

Although we anticipated that hole transport would be nearly negligible for irradiations at -140 °C, the observation that significantly less damage took place upon subsequent warming was not. One contributing factor is initial recombination, which may much higher at low temperature.

Most work in the literature on recombination has been done with thinner oxides; furthermore the results at low field are inconsistent. The net fraction of holes that survive initial recombination at low fields has ranged from about 14% in earlier work using cobalt-60 gamma rays [15] to about 4% for more recent studies with X-rays [16]. Microscopic differences in the electron-hole track structure can explain these results to some extent [17], but the effects of temperature at low fields has not been thoroughly examined.

Computer calculations show that the average spacing between electron-hole pairs produced by high-energy electrons is on the order of 100 nm [17]. This distance is large enough to reduce the importance of interactions with other electron-hole pairs. Consequently a geminate recombination model is usually used for electrons, as well as Compton electrons from cobalt-60 gamma rays, the two types of radiation sources used for experimental work in this paper.

Geminate recombination can be treated using the approach developed by Onsager [18], which yields a complex result known as the Smoluchowski equation. One of the key variables in that analysis is the recombination radius. An older theoretical study by Ausman provided numerical results for the Smoluchowski equation for various temperatures, using different values for the recombination radius [19]. Although one figure from that work is used in the book by Ma and Dressendorfer [20], another figure from the Ausman work is more directly applicable to our present study. This result, shown in Fig. 12, plots escape probability vs. electric field, including the low-field region that is applicable to the thick oxides in bipolar devices; the dashed lines are extrapolations from values at low field.

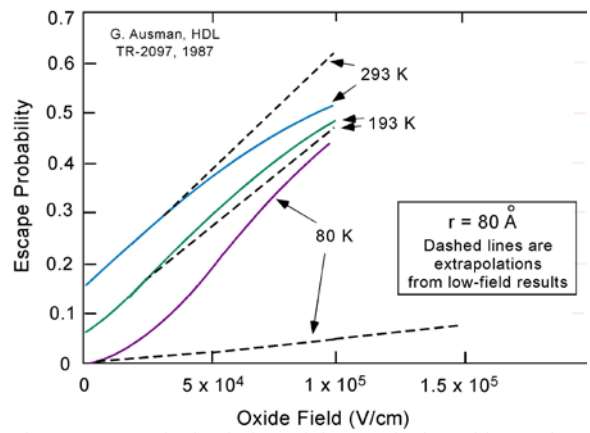

Fig. 12. Numerical solution of the Smoluchowski equation for the number of electron-hole pairs that escape initial recombination [19].

Our experiment at -138 °C (135 K) are approximately midway between the 193 and 80 K curves of Fig. 11. A reasonable estimate is an escape probability of 0.03 to 0.05, which would cause the number of holes to be reduced by a factor of 3 to 5, reasonably close to our experimental results (Fig. 7 and the following discussion). This suggests that increased recombination at low fields is the reason for reduced damage at low temperature.

Although the results in Fig. 12 are only given for three temperatures, the results can be used to predict results at other temperatures. For example, our low dose-rate irradiation of the LM111 at -35 °C (238 K) is approximately midway between the upper curves of Fig. 12. The interpolated low-field recombination for that temperature is about 12%, which would reduce the observed damage by about 25% compared to room temperature.

B. Charge Transport

Temperature plays an important role in hole transport. The temperature dependence is reduced at very low temperatures. This *transition temperature*, which is about ¼ of the Debye temperature, has been estimated to occur between 80 K and 160 K (note that our lateral pnp experiment, where hole transport was very low, was within that range).

For temperatures above the transition temperature, charge transport has been described by the equation [20]

$$t_s = t_s^o \left(\frac{d_{ox}}{a}\right)^{1/\alpha} \exp\left[\frac{\Delta_{Act}(E_{ox})}{kT}\right]$$

where t_s is scaled time in the CTRW model, t_s^o is a constant, a is the average hopping distance, and α is the disorder parameter. The latter is about 0.25 for gate oxides, and 0.33 for thick oxides.

The effect of temperature on the characteristic time in the CTRW model is incorporated through the last term, which is effectively an activation energy. Δ_{Act} depends on electric field:

$$\Delta_{Act}(E_{ox}) = \Delta_o - b\,E_{ox}$$

where Δ_o is the activation energy at low field, b is a constant (0.05 eV-cm/MV), and E_{ox} is the electric field.

For gate oxides, Δ_o is about 0.65, independent of E_{ox}. Experimental results for steam-grown field oxides indicate that Δ_o is about 0.77 eV [12].

Calculations of the temperature dependence of scaled time using older values for thin and thick gate oxides are shown in Fig. 13. The temperature dependence is very strong, corresponding to ~ T^{-20} near room temperature.

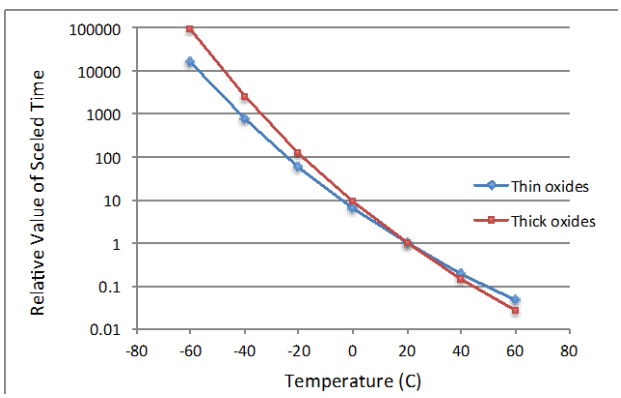

Fig. 13. Calculations of the effect of temperature on scaled time in the CTRW model.

Although npn transistors within bipolar integrated circuits are expected to have about the same temperature dependence, the oxides over their emitter-base junctions are thinner than the corresponding oxides in pnp transistors. Consequently the fourth power dependence of scaled time on gate oxide thickness predicts that t_s will be about two orders of magnitude smaller for npn transistors. In turn, there will be experimental conditions where damage builds up much more quickly in npn transistors.

C. *Circuit Design Factors*

Input Bias Current. As discussed earlier, input bias current, which in simple circuits is inversely proportional to the gain of the input transistor, is often used as a basic metric for radiation degradation [12]. Although this assumption holds for the LM111, the majority of new operational amplifier designs use more complex input stages, where the base current of a high-performance npn transistor is compensated by a current source that uses pnp transistors, reducing the input current by more than an order of magnitude. Such designs, which usually use pnp as well as npn transistors, do not perform as well at low temperature because of the large decrease in npn gain.

The OP27 is a good example of modern op-amps. Even though that particularly device continued to function at temperatures down to -150 °C for fresh devices, radiation damage imposes a further difficulty, as shown in Fig. 10. The performance degradation is consistent with the expected degradation of the compensation circuit, demonstrated with special measurements of input current matching.

Current Sources. Insight into the behavior of current sources can be provided by examining the basic current mirror. Most current mirrors use pnp current mirrors, which in elementary form are relatively insensitive to temperature. However, in the OP27, npn transistors are used to sample other currents within the circuit to current mirrors. Although this is satisfactory within normal temperature ranges, it affects current sources at the more extreme temperature conditions we are considering in this work because of the extremely low gain of npn transistors at low temperature. This is consistent with the difference in temperature sensitivity of power supply current for the LM111 comparator, which uses simple internal current sources, and the OP27. It suggests that internal current source design can potentially be used as a figure of merit to select devices with a wide temperature operating range.

VII. Conclusions

This paper has shown how the interplay between temperature sensitivity and radiation damage of internal transistors affects linear integrated circuits at temperatures below the normal low-temperature limit considered by the manufacturer. Several circuit types operate satisfactorily at temperatures that are more than 100 °C below the normal design range, providing a low-cost alternative to custom low-temperature circuits that is potentially useful for Mars surface and asteroid missions.

Low temperature performance depends on circuit design. Bandgap narrowing causes internal npn transistors to have a stronger dependence on temperature compared to pnp transistors, which (for typical linear IC processes) have much lower emitter doping levels.

Irradiations of pnp transistors at low temperature shows that little or no damage is observed until the device is warmed to high temperatures. Once the device

is warmed, damage is observed when the part is cycled to low temperature. This is consistent with the CTRW hole transport model. We also observed that less damage takes place when devices are irradiated at low temperature compared to irradiations at room temperature. This can be explained by the reduction in charge yield at low temperature, consistent with the early theoretical work of Ausman [19]. Consequently it may be possible to improve radiation performance of linear integrated circuits by operating them at reduced temperature. Our data shows that reductions in damage of a factor of two or more can be achieved when circuits are used near the lower limit of the MilSpec temperature range. Larger improvements are possible by operating them at lower temperature.

For low temperature cycling applications, such as Mars surface exploration, the results show that radiation damage is a second-order effect compared to temperature dependence for radiation levels below about 5 krad. Although specific devices are useful at higher radiation levels, far more effort is required to characterize and develop models because changes in performance due to radiation damage become comparable or greater than temperature effects above that threshold level.

REFERENCES

[1] R. D. Harris, *et al*., "Comparison of TID Effects in Space-Like Variable Dose Rates and Constant Dose Rates", IEEE Trans. Nucl. Sci., **55**(6), pp. 3088-3095 (2008).

[2] S. Feindt, J.-J. Hajjar, J. Lapham and D. Buss, "XFCB: A High-Speed Complementary Bipolar Process on Bonded SOI", Proc. 1992 Bipolar/BiCMOS Circuits and Technology Meeting, pp. 264-267.

[3] A. H. Johnston, *et al*., "Dose Rate Effects in Linear Bipolar Transistors," IEEE Trans. Nucl. Sci., **58**(6), pp. 2816-2823 (2011).

[4] G. Erdi, "Amplifier Techniques for Combining Low Noise, Precision, and High-Speed Performance", IEEE J. Solid State Ckts.", **SC-16** (6), pp. 653-661 (1981).

[5] J. D. Cressler, *et al*., "On the Low-Temperature Static and Dynamic Properties of High-Performance Silicon Bipolar Transistors", IEEE Trans. Elect. Dev., **36**(8), pp. 1489-1502 (1989).

[6] S. E. Swirhun, Y. –H. Kwark, and R. M. Swanson, "Measurements of Electron Lifetime, Electron Mobility and Band-Gap Narrowing in Heavily Doped p-Type Silicon", 1988 IEDM Proceedings, pp. 25-27.

[7] F. B. McLean, H. E. Boesch, Jr., and J. M. McGarrity, "Hole Transport and Recovery Characteristics of SiO2 Gate Insulators," IEEE Trans. Nucl. Sci., **23**(6), pp. 1506-1512 (1976).

[8] T. R. Oldham, *Ionizing Radiation Effects in MOS Oxides*, World Scientific: Singapore, 1999.

[9] D. M. Fleetwood, P. S. Winokur, R. A. Rehe, T. L. Meisenheimer, J. R. Schwank, M. R. Shaneyfelt and L. E. Riewe, "Effects of Oxide Traps, Interface Traps, and Border Traps on Metal-Oxide Semiconductor Devices", J. Appl. Phys., **73**(10), pp 5058-5074 (1993).

[10] E. H. Snow, A. S. Grove, and D. J. Fitzgerald, "Effects of Ionizing Radiation on Oxidized Silicon Surfaces and Planar Devices", Proc. IEEE, **55**(7), pp. 1168-1185 (1967).

[11] H. Sher and E. W. Montroll, "Anomalous Transit Time Dispersion in Amorphous Solids", Phys. Rev. B, **12**(6), pp. 2455-2477 (1975).

[12] H. E.Boesch, Jr., and F. B. McLean, "Hole Transport and Trapping in Field Oxides," IEEE Trans. Nucl. Sci., **32**(6), pp. 3940-3945 (1985).

[13] R. L. Pease, "Total Dose Effects in Bipolar Devices and Circuits," IEEE Trans. Nucl. Sci., **50**(3), pp. 539-551 (2003).

[14] G. C. M. Meijer. P. C. Sachmale, and K. van Zalinge, "A New Curvature-Corrected Bandgap Reference," IEEE J. Solid-State Circuits, **17**, pp. 1139-1147 (1982).

[15] J. E. Boesch, Jr., and J. M. McGarrity, "Charge Yield and Dose Effects in MOS Capacitors at 80K", IEEE Trans. Nucl. Sci., **23**(6), pp. 1520-1527 (1976).

[16] T. R. Oldham and J. M. McGarrity, "Comparison of ^{60}Co and 10 keV X-ray Response in MOS Capacitors", IEEE Trans. Nucl. Sci., **30**(6), pp. 4377-4381 (1983).

[17] M. Murat, A. Akkerman, and J. Barak, "Spatial Distribution of Electron-Hole Pairs Induced by Electrons and Protons in SiO_2", IEEE Trans. Nucl. Sci., **51**(6), pp. 3211-3218 (2004).

[18] L. Onsager, "Initial Recombination of Ions", Phys. Rev., **54**, pp. 554-557 (1938).

[19] G. A. Ausman, Jr., "Field Dependence of Geminant Recombination in a Dielectric Medium", Harry Diamond Laboratory Report HDL-TR-2097, January 1987.

[20] T. P. Ma and P. V. Dressendorfer, Eds., *Ionizing Radiation Effects in MOS Devices and Circuits*, John Wiley: New York, 1989.