National Aeronautics
and Space Administration

NAND Flash Qualification Guideline

Jason Heidecker

Jet Propulsion Laboratory, California Institute of Technology

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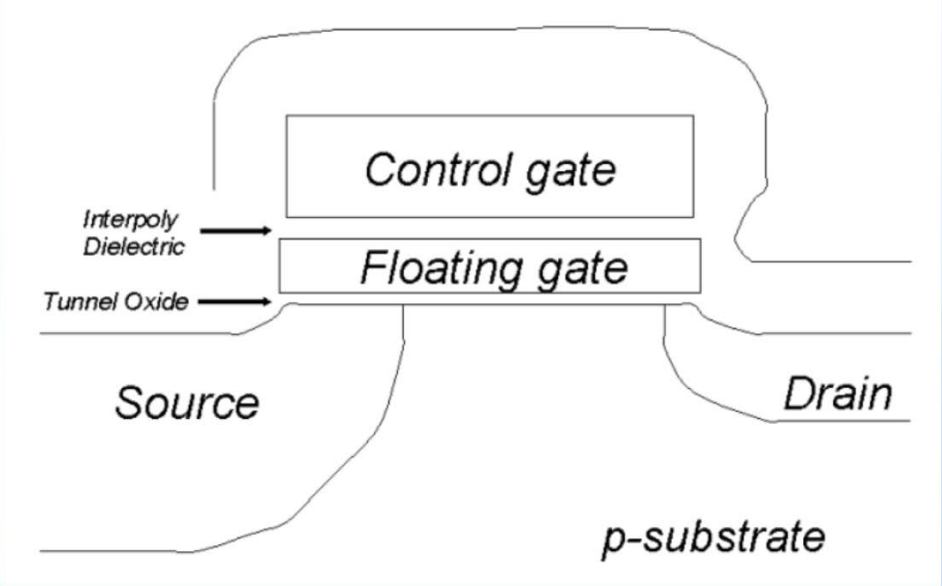
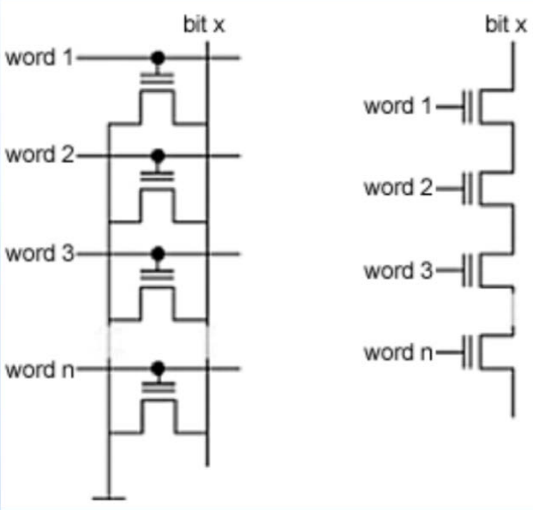
What is NAND Flash?

- Unique architecture.
- PROGRAM/READ by PAGE.
- ERASE by BLOCK.
- Built on CMOS. TSOP packages.
- Nonvolatile; low standby power.
- VERY high density.
- Mature technology, billions of chips produced over decades.

Only memory to offer both Gb density and nonvolatility.

Floating Gate Memory Cell



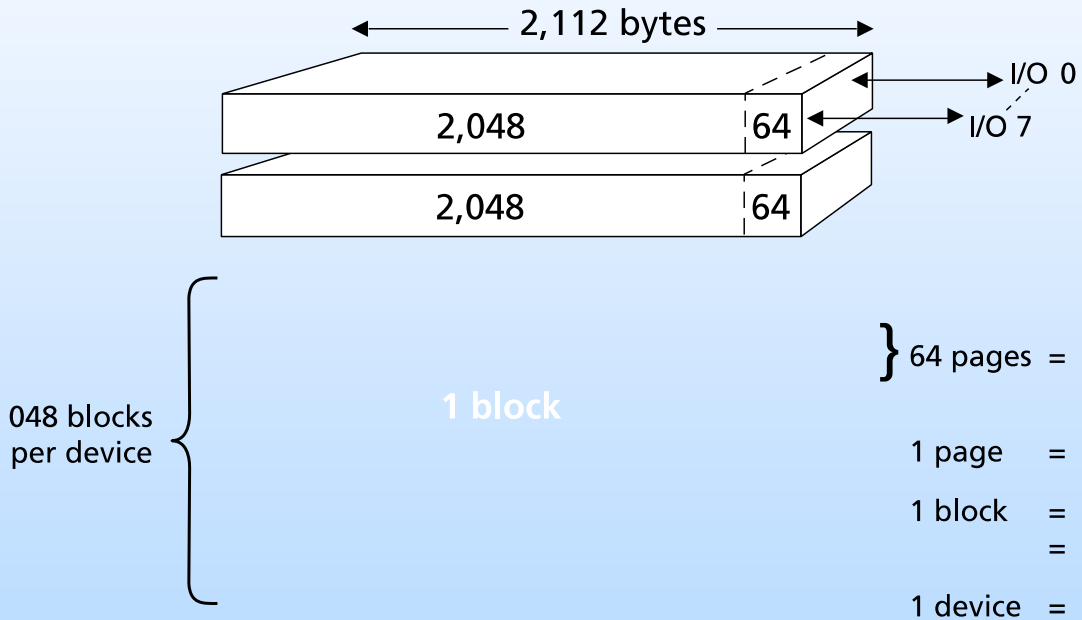


Comparison of NOR (left) and NAND (right) Flash cells.

Array Organization

Bits, Bytes, Pages, and Blocks

Array Organization for 4 Gb Micron Device



64 pages = 1 block
(128K + 4K) bytes

1 page = (2K + 64) bytes

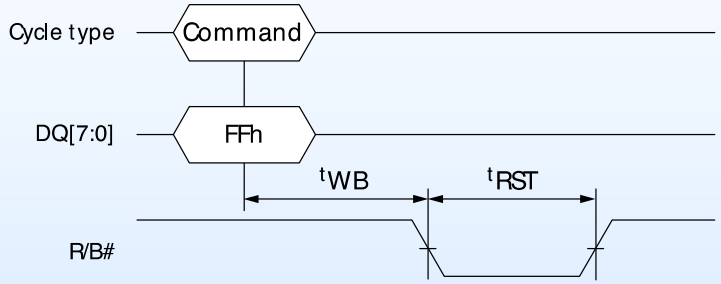
1 block = (2K + 64) bytes x 64 pages
= (128K + 4K) bytes

1 device = (2K + 64) bytes x 64 pages
x 2,048 blocks
= 2,112Mb

Operation

Commands, Addresses, and Data sent over same I/O

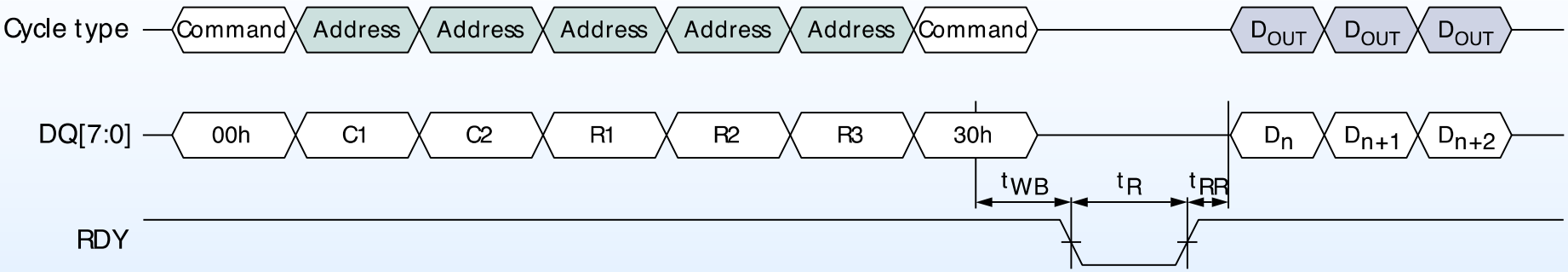
RESET (FFh) Operation



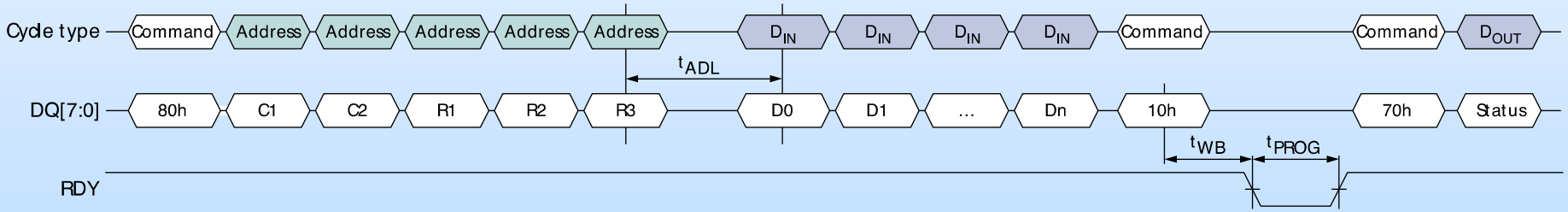
1 ●	48	
2	47	
3	46	
4	45	
5	44	
6	43	
7	42	
8	41	
9	40	
10	39	
11	38	DNU or Vss
12	37	Vcc
13	36	Vss
14	35	NC
15	34	NC
16	33	NC
17	32	I/O3
18	31	I/O2
19	30	I/O1
20	29	I/O0
21	28	NC
22	27	NC
23	26	NC
24	25	NC

Operation

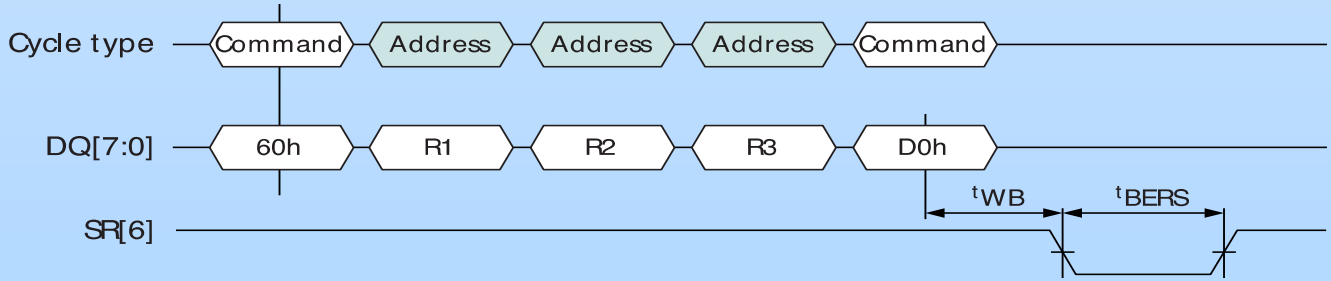
PAGE READ



PAGE PROGRAM



BLOCK ERASE



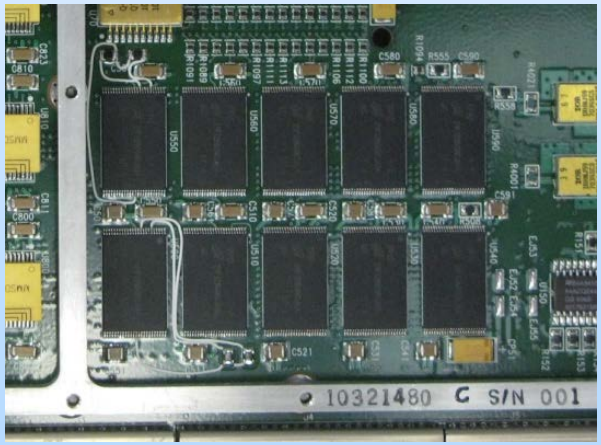
Applications

COMMERCIAL

- **Mobile Computing**
  - Cell Phones
  - MP3
  - "Thumb" Drives
- **Hard Drives**
  - "Instant On" discs

SPACE

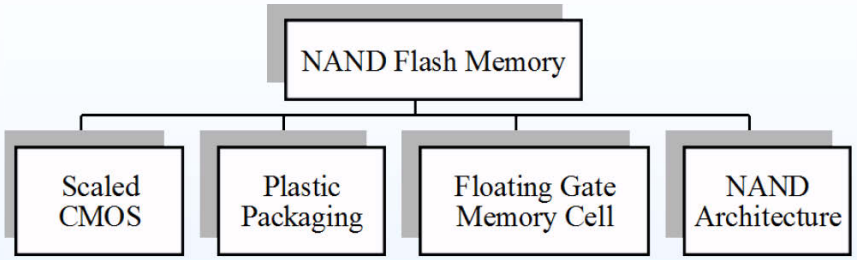
- **NVM Data Storage**
  - Engineering & Science Data



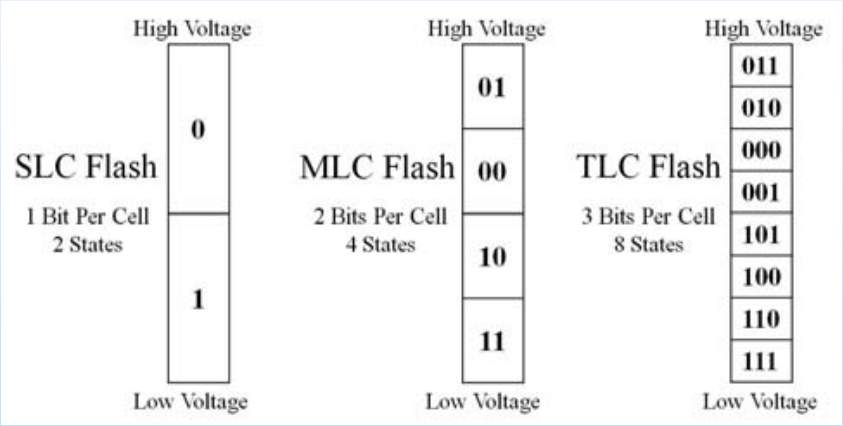
10 x 128 Gb MLC NAND Flash parts on space project (JPL)

Reliability Issues

- Reliability (bit errors) is getting worse with newer NAND technologies.
- Smaller Vth/level = More Errors
- Fowler-Nordheim Tunneling for Erase and Program uses destructive high voltages ~20 V



NAND Reliability



Smaller Margins Means Less Reliability (Susceptibility to disturb, SILC)

Four Areas of Focus:

1. Bad Blocks
2. Endurance
3. Retention
4. Disturb

Bad Blocks

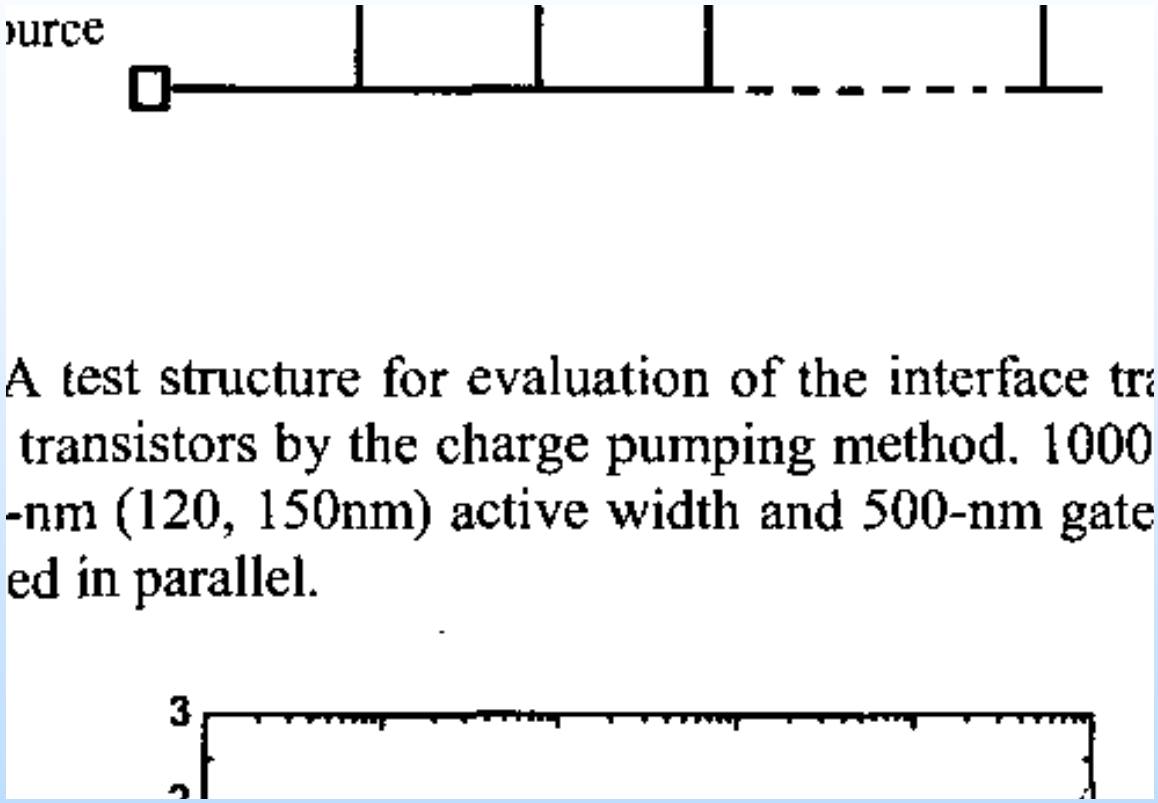
- Devices are expected to ship with a specified number of bad blocks.
- Specification can be as high as 5%.
  - Parts may be shipped with 1% bad blocks, but spec says device should not exceed 5% bad blocks (in this case) before endurance specification is met.
- Blocks will "go bad" with use.
- Bad block is defined as having a certain bit error rate (BER).

For example, a particular 64 Gb Micron TLC device has 2736 blocks:

- Spec says: it has an
  - endurance specification of 500 cycles
  - minimum number of valid block of 2626
  - 60-bit ECC required per 1146 bytes of data

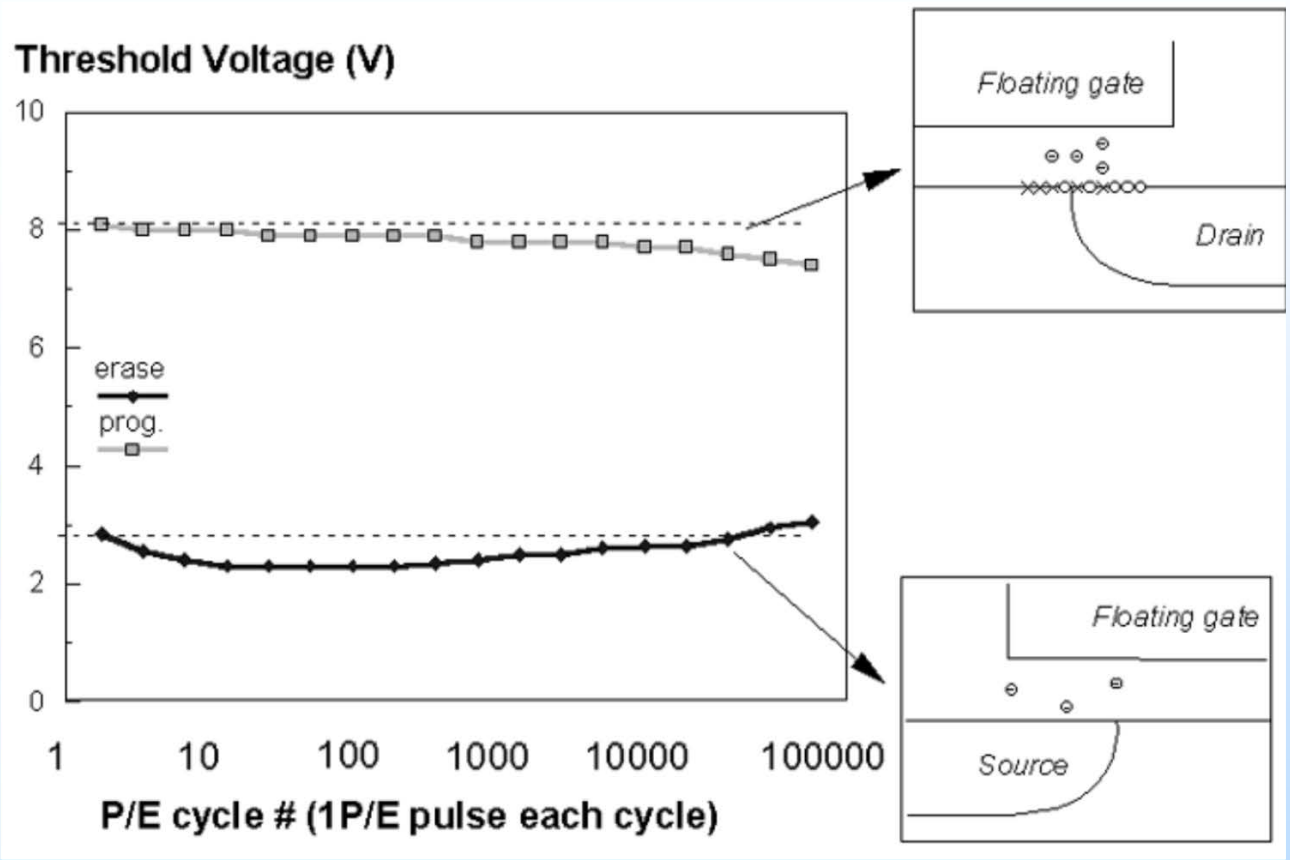
Therefore, the user should never see more than 60 bit errors per 1146 bytes of data in more than 110 blocks, up to 500 cycles.

Data Retention



DEGRADATIONF TUNNEL OXIDE BY FN CURRENT STRESS AND ITS EFFECTS ON DATA RETENTION CHARACTERISTICS OF 90-nm NAND FLASH MEMORY CELLS
Lee, J. IRPS, 2003.

Endurance

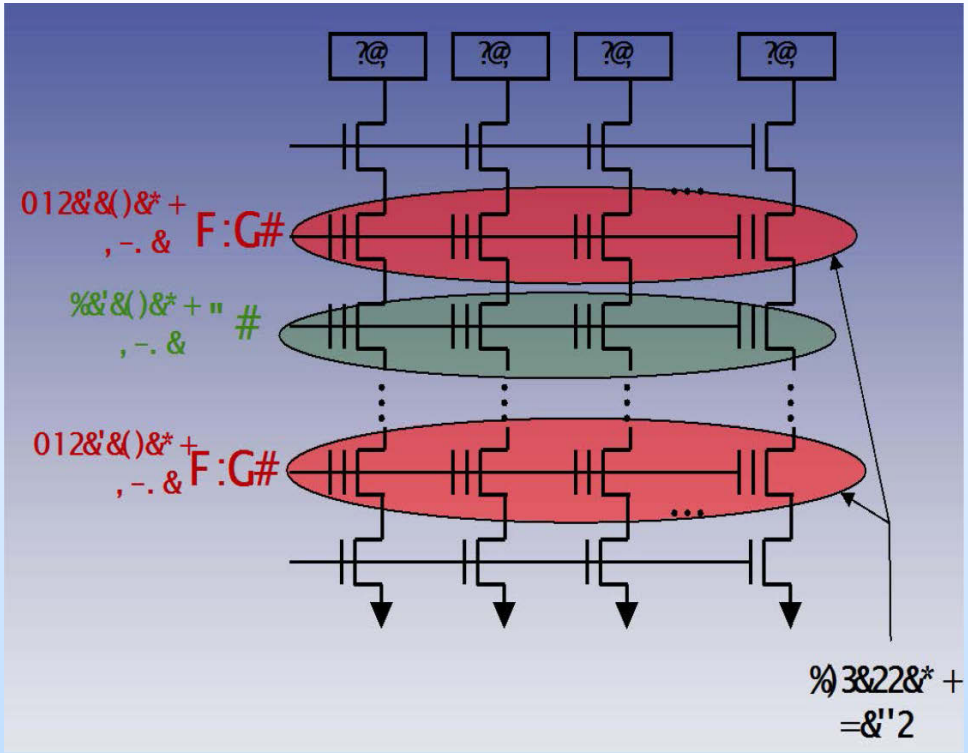


Introduction to Flash Memory

ROBERTO BEZ, EMILIO CAMERLENGHI, ALBERTO MODELLI, AND ANGELO VISCONTI
PROCEEDINGS OF THE IEEE, VOL. 91, NO. 4, APRIL 2003

Read Disturb

- Flash also susceptible to Program and Erase Disturb, but only Read disturb is prevalent in modern devices
- Read Disturb confined to block being operated on
- Stressed cells are in unselected pages
- Nondestructive
- Disturb occurs when charge collects on the floating gate, causing the cell to appear weakly programmed



NAND Flash Reliability and Performance The Software Effect
Wes Prouty, Micron Technology, Inc.
Flash Memory Summit, 2007.

Failure Modes

Failure Mode	Detection Method	Countermeasure
Erase Failure	Check status after erase	Block replacement
Program Failure	Check status after program	Block replacement
Bit Errors (within spec)	Verify ECC	ECC correction
Bit Errors (beyond spec)	Verify ECC	Block replacement

Screening & Qualification

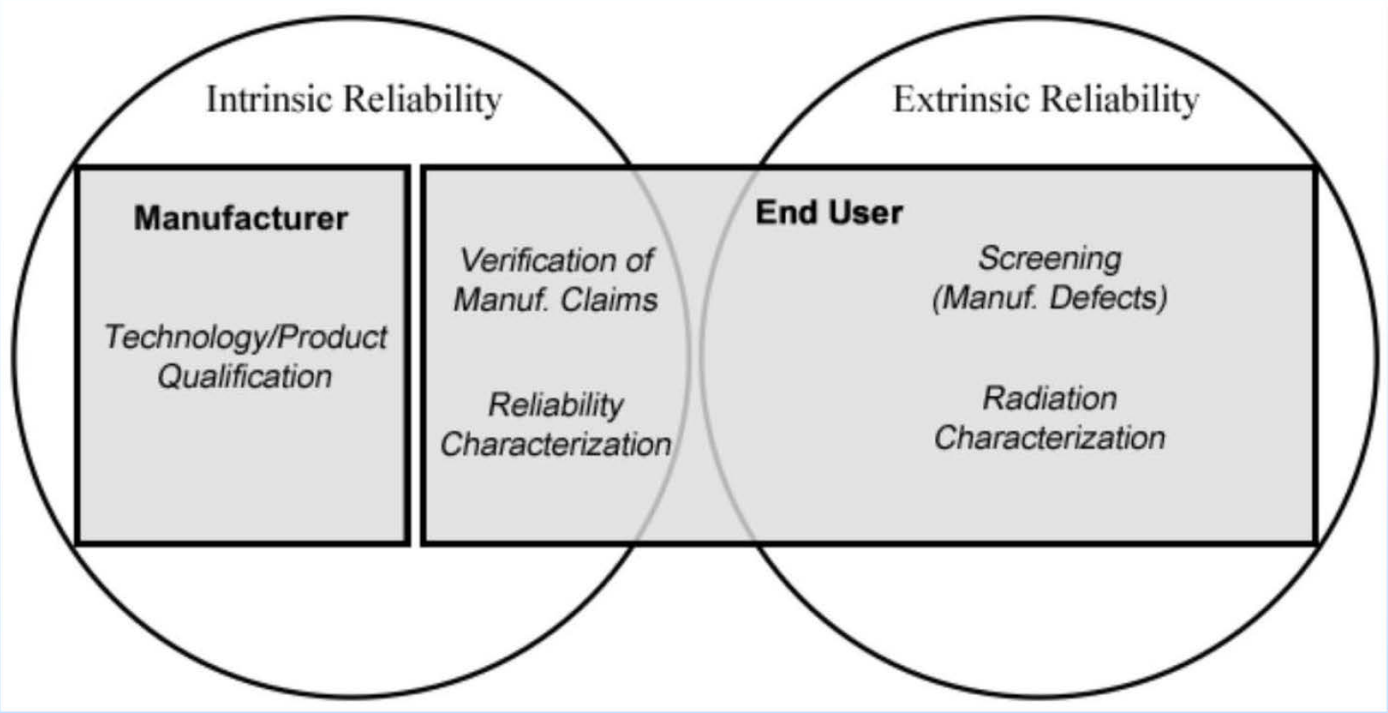


Diagram depicting the roles of the manufacturer and space project in screening and qualifying an EEE device for space application.

Screening

Step	Test	Requirements	Sample Size & Notes	
			Level 1 Mission	Level 2 Mission
1	Glass transition temperature, Tg	Thermal Mechanical Analysis (TMA)	3 pc	3 pc
2	Serialization		100%	100%
3	Electricals (AC, DC, Functional)	Test to datasheet. Read & record data. Tri-temp (-40°C, 25°C, 85°C).	100%	100%
4	Dynamic Burn-In	MIL-STD-883, Method 1015, 125°C	100% 240 hrs	100% 160 hrs
5	Electricals (AC, DC, Functional)	Test to datasheet. Read & record data. Tri-temp (-40°C, 25°C, 85°C).	100%	100%
6	Delta Calculations	25°C	100%	100%
7	Percent Defective Allowable (PDA) Calculation		5% PDA[1]	5% PDA
8	Stabilization Bake	125°C, 24 hours	100%	100%
9	Flight Part Storage	In accordance with [5].	100%	100%

[1] 3% PDA for functional parameters at 25°C.

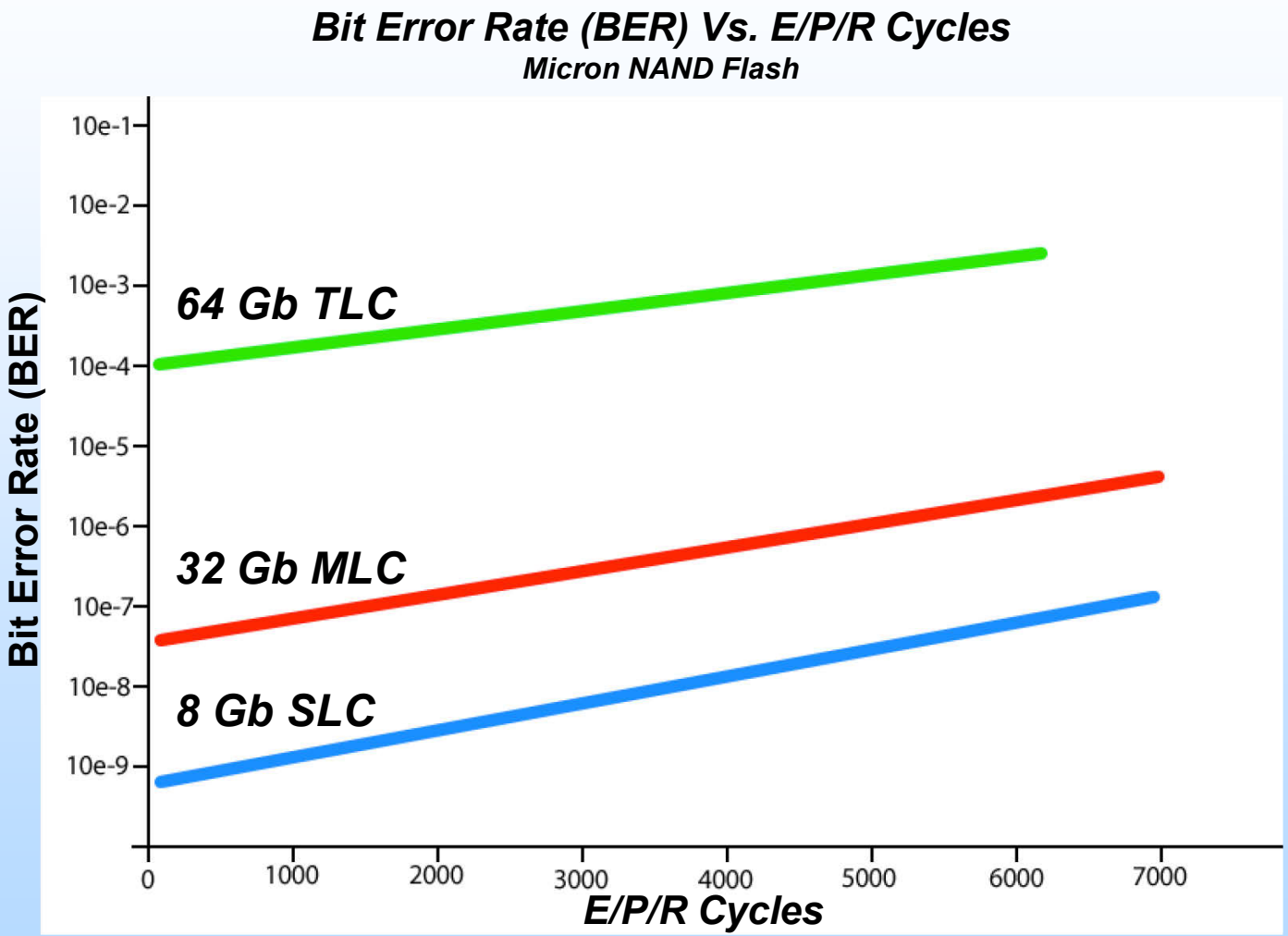
Qualification

Step	Test	Requirements	Sample Size & Notes	
			Level 1 Mission	Level 2 Mission
12	Temp Cycling	MIL-STD-883, Method 1010, Condition B	22 pc, 300 cycles	22 pc, 100 cycles
13	Electricals (AC, DC, Functional)	Test to datasheet. Read & record data. Tri-temp (-40°C, 25°C, 85°C).	45 pc	22 pc
14	High Temperature Operating Life (HTOL)	MIL-STD-883, Method 1005, 125°C		
15	Electricals (AC, DC, Functional)	Test to datasheet. Read & record data. Tri-temp (-40°C, 25°C, 85°C).		
16	Destructive Physical Analysis (DPA)	2 pc from temp cycled samples, rest from life tested samples	5 pc	3 pc
17	Reliability Characterization	See Table 4	10 pc	
18	Radiation Characterization	TID and SEE per radiation specialist recommendation	Per rad specialist	

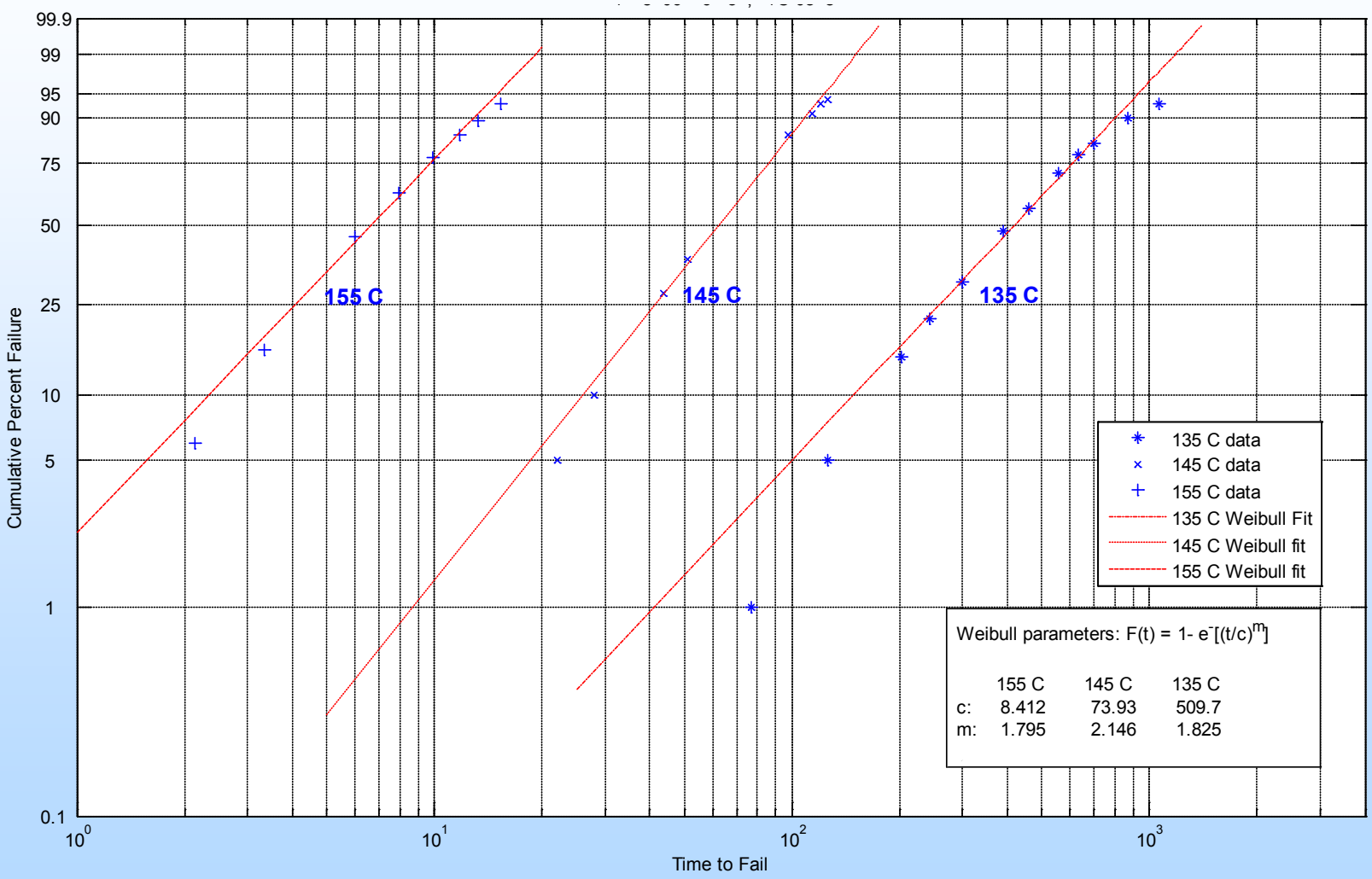
Reliability Characterization

Step	Test	Requirements
1	Endurance Cycling	Up to 1.5x application endurance requirement
2	Data Retention Bake	Three temperatures; at 1.5x application endurance requirement
3	Read Disturb	Multiple reads after 0, 0.5x, 1.0x, and 1.5x application endurance requirement
4	Worst Case UBER Calculation	At 1.5x application endurance requirement

Endurance Cycling



Data Retention Bake

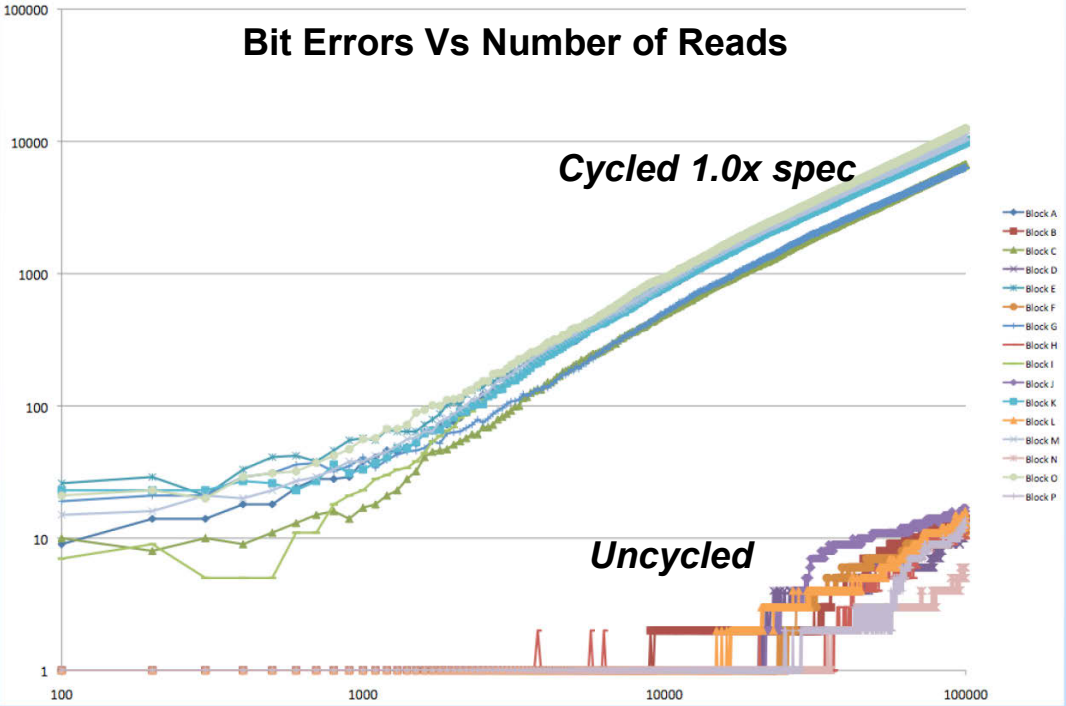


Read Disturb

- **PURPOSE**
  - Measure how BER worsens with multiple reads of block of data

- **DISTURB TEST**
  1. Erase
  2. Program
  3. Read many times

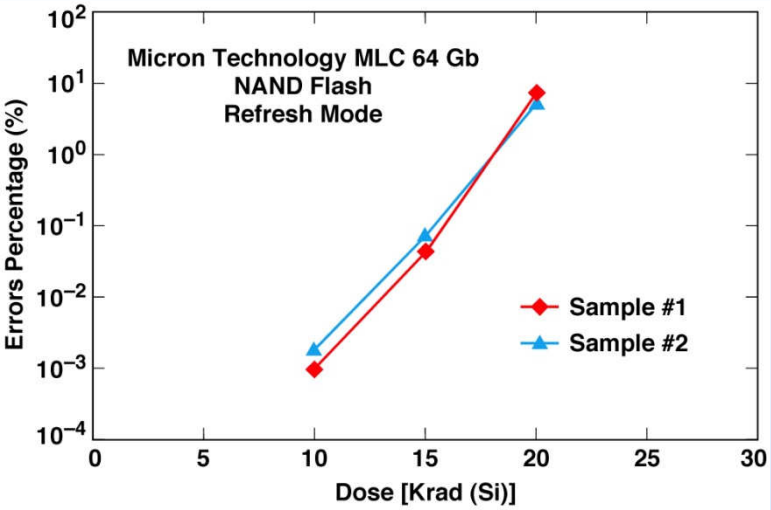
- **Repeat test after cycling device. Perform at:**
  - 0x
  - 0.5x
  - 1.0x
  - 1.5x

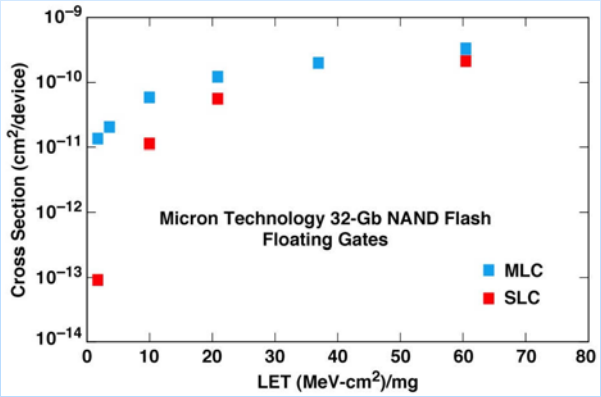


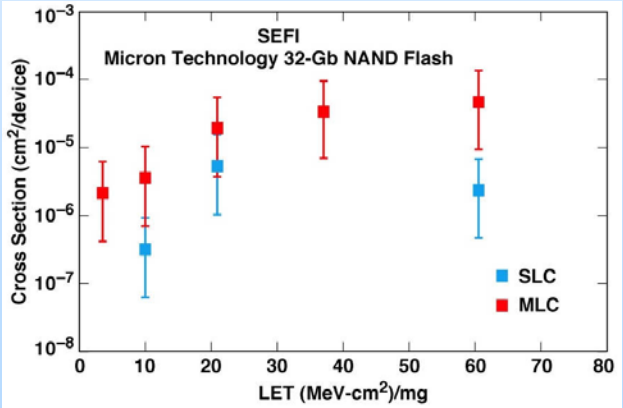
Read disturb error rate much worse in parts that have consumed erase/program/read cycles.

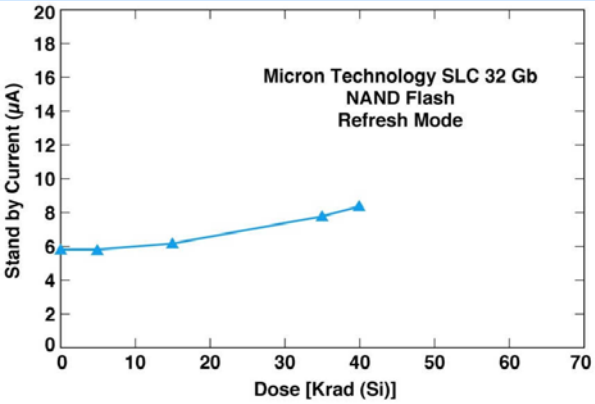
Radiation Effects

- Every lot should be tested
- Total Ionizing Dose (TID)
- Single Event Upset (SEU)
- Single Event Fault Interrupt (SEFI)
- Flash can be tested for different applications:
  - Refresh: Erase/Program Between Read
  - No Refresh: Read Only







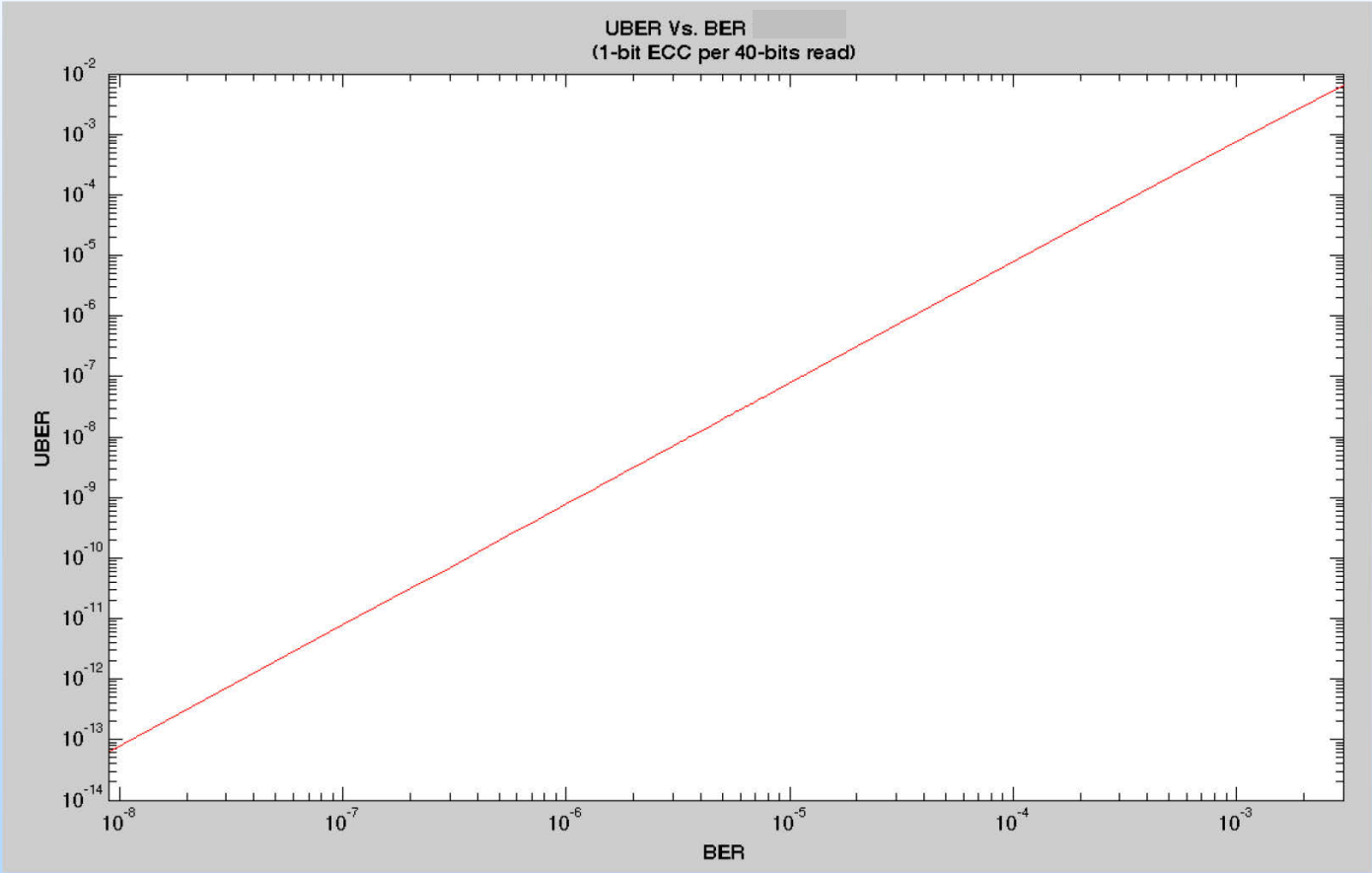


Data from Irom and Nguyen (JPL). NEPP 2011.

Worst Case UBER Calculation

When calculating uncorrectable bit error rate (UBER) from raw NAND bit error rate (BER), the worst case BER should be used. Here's a general example, but users should tailor to their specific application or use case:

$$BER_{worst\ case} = BER_{radiation} + BER_{cycling} + BER_{disturb}$$



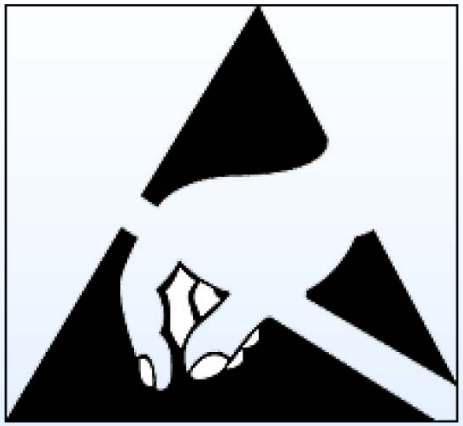
System Level Considerations

Error Correction Codes (ECC)

- Always required with NAND Flash.

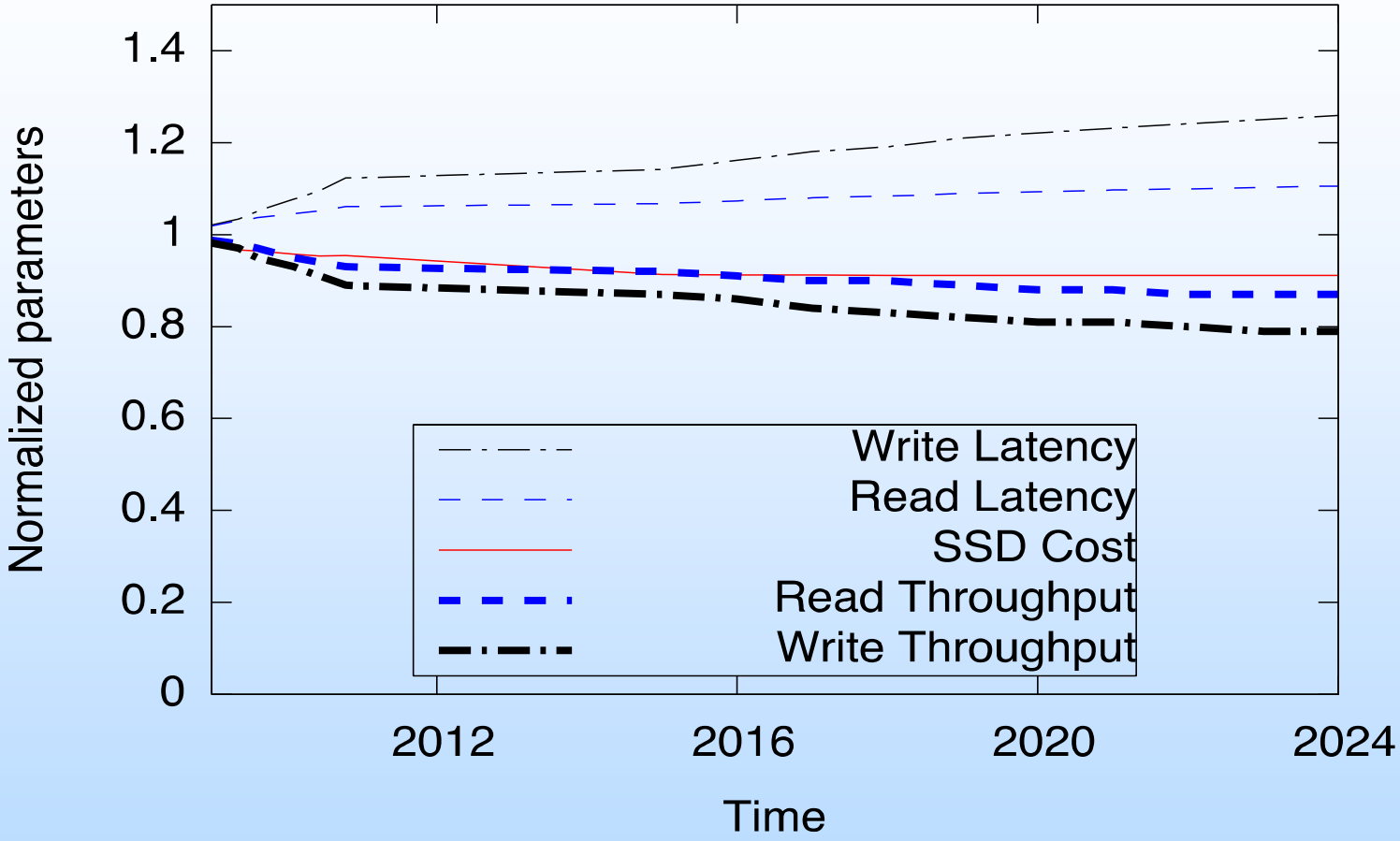
NAND Type	Datasheet ECC Requirement	Corresponding Bit Error Rate	Recommended ECC
SLC	1-bit ECC per 528 bytes of data	0.02%	SEC/DEC Hamming Code or Reed-Solomon Code
MLC	12-bit ECC per 539 bytes of data	0.28%	BCH Algorithms
TLC	60-bit ECC per 1146 bytes of data	0.65%	Low Density Parity Check (LDPC) Codes

Other Recommendations



- **Pure Tin Leads**
  - All NAND Flash are PEMS, which have pure tins leads. Leads must be retinned or solder-dipped before installation onto flight boards.
- **Disturb Error Mitigation**
  - Limit the number of reads between programming, sequentially program pages in a block, and minimize partial-page programming.
- **Moisture Sensitivity (PEMS Storage)**
  - Plastic packaging is hygroscopic
  - Need to be stored in humidity controlled environments
  - Should be “baked out” prior to assembly to prevent popcorning or other damage
- **Electrostatic Discharge (ESD) Sensitivity**
  - Most NAND Flash devices are classified has having ESD sensitivities of Class 1C (>1000 V HBM) or better.
  - Most standard ESD practices (static dissipative wrist straps, workbenches, and storage bags) will prevent damaging the device.

End of the Road for Flash?



The Bleak Future of NAND Flash Memory

Laura M. Grupp†, John D. Davis‡, Steven Swanson†
†Department of Computer Science and Engineering, University of California, San Diego
‡Microsoft Research, Mountain View

Sources/References

1. Heidecker, J. “NAND Flash Screening and Qualification Guideline for Space Application.” NASA Electronics and Packaging Program (NEPP), 2011.

2. Sheldon, D. “Disturb Testing in Flash Memories.” NASA Electronics and Packaging Program (NEPP), 2009.

3. Yaakobi, L. “Characterization and Error-Correcting Codes for TLC Flash Memories.” International Conference on Computing, Networking and Communications, Data Storage Technology and Applications Symposium, 2012.

4. Prouty, W. “NAND Flash Reliability and Performance, The Software Effect.” Flash Memory Summit, 2007.

5. Grupp, L. “The Bleak Future of NAND Flash Memory.” University of San Diego, 2011.

6. Bez, R. “Introduction to Flash Memory.” Proceedings of the IEEE, Vol. 91, No. 4, April 2003.

7. Iron, F. “Radiation Tests of Highly Scaled, High-Density, Commercial, Nonvolatile NAND Flash Memories—Update 2011.” NASA Electronics and Packaging Program (NEPP), 2011.

8. “NAND Flash 101,” Micron.com.