NAND Flash Qualification Guideline

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What is NAND Flash?

- Unique architecture.
- PROGRAM/READ by PAGE.
- ERASE by BLOCK.
- Built on CMOS. TSOP packages.
- Nonvolatile; low standby power.
- VERY high density.
- Mature technology, billions of chips produced over decades.

*Only memory to offer both Gb density and nonvolatility.*
Floating Gate Memory Cell

Comparison of NOR (left) and NAND (right) Flash cells
Array Organization

Bits, Bytes, Pages, and Blocks

Array Organization for 4 Gb Micron Device

- 2,112 bytes
- 2,048 bits
- 64 bytes
- 64 pages

048 blocks per device

1 block

64 pages = 1 block (128K + 4K) bytes
1 page = (2K + 64) bytes
1 block = (2K + 64) bytes x 64 pages = (128K + 4K) bytes
1 device = (2K + 64) bytes x 64 pages x 2,048 blocks
= 2,112Mb
Operation

Commands, Addresses, and Data sent over same I/O

RESET (FFh) Operation

<table>
<thead>
<tr>
<th>Cycle type</th>
<th>Command</th>
<th>DQ[7:0]</th>
<th>FFh</th>
<th>WB</th>
<th>RST</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>●</td>
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<tr>
<td>24</td>
<td></td>
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</tr>
</tbody>
</table>

1 - 48

38, 37, 36, 35, 34, 33, 32, 31, 30, 29, 28, 27, 26, 25, DNU or Vss, Vcc, Vss, NC, NC, NC, I/O3, I/O2, I/O1, I/O0, NC, NC, NC, NC
Operation

PAGE READ

Cycle type: Command | Address | Address | Address | Address | Address | Command | D_OUT | D_OUT | D_OUT

DQ[7:0]:
00h | C1 | C2 | R1 | R2 | R3 | 30h | D_n | D_n+1 | D_n+2

RDY

PAGE PROGRAM

Cycle type: Command | Address | Address | Address | Address | Address | D_IN | D_IN | D_IN | D_IN | Command | Command | D_OUT

DQ[7:0]:
80h | C1 | C2 | R1 | R2 | R3 | D0 | D1 | ... | Dn | 10h | 70h | Status

RDY

BLOCK ERASE

Cycle type: Command | Address | Address | Address | Address | Command

DQ[7:0]:
60h | R1 | R2 | R3 | D0h

SR[6]

tWB | tPROG | tADL | tWB | tBERS
Applications

COMMERCIAL

- Mobile Computing
  - Cell Phones
  - MP3
  - “Thumb” Drives

- Hard Drives
  - “Instant On” discs

SPACE

- NVM Data Storage
  - Engineering & Science Data

10 x 128 Gb MLC NAND Flash parts on space project (JPL)
Reliability Issues

- Reliability (bit errors) is getting worse with newer NAND technologies.
- Smaller Vth/level = More Errors
- Fowler-Nordheim Tunneling for Erase and Program uses destructive high voltages ~20 V

Four Areas of Focus:
1. Bad Blocks
2. Endurance
3. Retention
4. Disturb

Smaller Margins Means Less Reliability (Susceptibility to disturb, SILC)
Bad Blocks

• Devices are expected to ship with a specified number of bad blocks.

• Specification can be as high as 5%.
  – Parts may be shipped with 1% bad blocks, but spec says device should not exceed 5% bad blocks (in this case) before endurance specification is met.

• Blocks will “go bad” with use.

• Bad block is defined as having a certain bit error rate (BER).

For example, a particular 64 Gb Micron TLC device has 2736 blocks:

• Spec says: it has an
  – endurance specification of 500 cycles
  – minimum number of valid block of 2626
  – 60-bit ECC required per 1146 bytes of data

Therefore, the user should never see more than 60 bit errors per 1146 bytes of data in more than 110 blocks, up to 500 cycles.
A test structure for evaluation of the interface trap states in transistors by the charge pumping method. 10000 90-nm (120, 150nm) active width and 500-nm gate length in parallel.

Endurance

Introduction to Flash Memory
ROBERTO BEZ, EMILIO CAMERLENGHI, ALBERTO MODELLI, AND ANGELO VISCONTI
PROCEEDINGS OF THE IEEE, VOL. 91, NO. 4, APRIL 2003
Read Disturb

- Flash also susceptible to Program and Erase Disturb, but only Read disturb is prevalent in modern devices

- Read Disturb confined to block being operated on

- Stressed cells are in unselected pages

- Nondestructive

- Disturb occurs when charge collects on the floating gate, causing the cell to appear weakly programmed

*NAND Flash Reliability and Performance The Software Effect*  
Wes Prouty, Micron Technology, Inc.  
Flash Memory Summit, 2007.
## Failure Modes

<table>
<thead>
<tr>
<th>Failure Mode</th>
<th>Detection Method</th>
<th>Countermeasure</th>
</tr>
</thead>
<tbody>
<tr>
<td>Erase Failure</td>
<td>Check status after erase</td>
<td>Block replacement</td>
</tr>
<tr>
<td>Program Failure</td>
<td>Check status after program</td>
<td>Block replacement</td>
</tr>
<tr>
<td>Bit Errors (within spec)</td>
<td>Verify ECC</td>
<td>ECC correction</td>
</tr>
<tr>
<td>Bit Errors (beyond spec)</td>
<td>Verify ECC</td>
<td>Block replacement</td>
</tr>
</tbody>
</table>
Screening & Qualification

Diagram depicting the roles of the manufacturer and space project in screening and qualifying an EEE device for space application.
<table>
<thead>
<tr>
<th>Step</th>
<th>Test</th>
<th>Requirements</th>
<th>Sample Size &amp; Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>Level 1 Mission</td>
</tr>
<tr>
<td>1</td>
<td>Glass transition temperature, Tg</td>
<td>Thermal Mechanical Analysis (TMA)</td>
<td>3 pc</td>
</tr>
<tr>
<td>2</td>
<td>Serialization</td>
<td></td>
<td>100%</td>
</tr>
<tr>
<td>3</td>
<td>Electricals (AC, DC, Functional)</td>
<td>Test to datasheet. Read &amp; record data. Tri-temp (-40°C, 25°C, 85°C).</td>
<td>100%</td>
</tr>
<tr>
<td>4</td>
<td>Dynamic Burn-In</td>
<td>MIL-STD-883, Method 1015, 125°C</td>
<td>100% 240 hrs</td>
</tr>
<tr>
<td>5</td>
<td>Electricals (AC, DC, Functional)</td>
<td>Test to datasheet. Read &amp; record data. Tri-temp (-40°C, 25°C, 85°C).</td>
<td>100%</td>
</tr>
<tr>
<td>6</td>
<td>Delta Calculations</td>
<td>25°C</td>
<td>100%</td>
</tr>
<tr>
<td>7</td>
<td>Percent Defective Allowable (PDA) Calculation</td>
<td></td>
<td>5% PDA¹</td>
</tr>
<tr>
<td>8</td>
<td>Stabilization Bake</td>
<td>125°C, 24 hours</td>
<td>100%</td>
</tr>
<tr>
<td>9</td>
<td>Flight Part Storage</td>
<td>In accordance with [5].</td>
<td>100%</td>
</tr>
</tbody>
</table>

¹3% PDA for functional parameters at 25°C.
## Qualification

<table>
<thead>
<tr>
<th>Step</th>
<th>Test</th>
<th>Requirements</th>
<th>Sample Size &amp; Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>12</td>
<td>Temp Cycling</td>
<td>MIL-STD-883, Method 1010, Condition B</td>
<td>22 pc, 300 cycles</td>
</tr>
<tr>
<td>14</td>
<td>High Temperature Operating Life (HTOL)</td>
<td>MIL-STD-883, Method 1005, 125°C</td>
<td>45 pc</td>
</tr>
<tr>
<td>16</td>
<td>Destructive Physical Analysis (DPA)</td>
<td>2 pc from temp cycled samples, rest from life tested samples</td>
<td>5 pc</td>
</tr>
<tr>
<td>17</td>
<td>Reliability Characterization</td>
<td>See Table 4</td>
<td>10 pc</td>
</tr>
<tr>
<td>18</td>
<td>Radiation Characterization</td>
<td>TID and SEE per radiation specialist recommendation</td>
<td>Per rad specialist</td>
</tr>
</tbody>
</table>
## Reliability Characterization

<table>
<thead>
<tr>
<th>Step</th>
<th>Test</th>
<th>Requirements</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Endurance Cycling</td>
<td>Up to 1.5x application endurance requirement</td>
</tr>
<tr>
<td>2</td>
<td>Data Retention Bake</td>
<td>Three temperatures; at 1.5x application endurance requirement</td>
</tr>
<tr>
<td>3</td>
<td>Read Disturb</td>
<td>Multiple reads after 0, 0.5x, 1.0x, and 1.5x application endurance requirement</td>
</tr>
<tr>
<td>4</td>
<td>Worst Case UBER Calculation</td>
<td>At 1.5x application endurance requirement</td>
</tr>
</tbody>
</table>
Endurance Cycling

Bit Error Rate (BER) Vs. E/P/R Cycles
Micron NAND Flash

64 Gb TLC
32 Gb MLC
8 Gb SLC
Data Retention Bake

Weibull parameters: $F(t) = 1 - e^{-\left(\frac{t}{c}\right)^m}$

<table>
<thead>
<tr>
<th>Temperature</th>
<th>c</th>
<th>m</th>
</tr>
</thead>
<tbody>
<tr>
<td>135°C</td>
<td>8.412</td>
<td>1.795</td>
</tr>
<tr>
<td>145°C</td>
<td>73.93</td>
<td>2.146</td>
</tr>
<tr>
<td>155°C</td>
<td>509.7</td>
<td>1.825</td>
</tr>
</tbody>
</table>
Read Disturb

• PURPOSE
  – Measure how BER worsens with multiple reads of block of data

• DISTURB TEST
  1. Erase
  2. Program
  3. Read many times

• Repeat test after cycling device. Perform at:
  – 0x
  – 0.5x
  – 1.0x
  – 1.5x

Read disturb error rate much worse in parts that have consumed erase/program/read cycles.
Radiation Effects

- Every lot should be tested
- Total Ionizing Dose (TID)
- Single Event Upset (SEU)
- Single Event Fault Interrupt (SEFI)

Flash can be tested for different applications:
- Refresh: Erase/Program Between Read
- No Refresh: Read Only

Data from Irom and Nguyen (JPL).
NEPP 2011.
Worst Case UBER Calculation

When calculating uncorrectable bit error rate (UBER) from raw NAND bit error rate (BER), the worst case BER should be used. Here’s a general example, but users should tailor to their specific application or use case:

\[ \text{BER}_{\text{worst case}} = \text{BER}_{\text{radiation}} + \text{BER}_{\text{cycling}} + \text{BER}_{\text{disturb}} \]
## System Level Considerations

### Error Correction Codes (ECC)
- Always required with NAND Flash.

<table>
<thead>
<tr>
<th>NAND Type</th>
<th>Datasheet ECC Requirement</th>
<th>Corresponding Bit Error Rate</th>
<th>Recommended ECC</th>
</tr>
</thead>
<tbody>
<tr>
<td>SLC</td>
<td>1-bit ECC per 528 bytes of data</td>
<td>0.02%</td>
<td>SEC/DEC Hamming Code or Reed-Solomon Code</td>
</tr>
<tr>
<td>MLC</td>
<td>12-bit ECC per 539 bytes of data</td>
<td>0.28%</td>
<td>BCH Algorithms</td>
</tr>
<tr>
<td>TLC</td>
<td>60-bit ECC per 1146 bytes of data</td>
<td>0.65%</td>
<td>Low Density Parity Check (LDPC) Codes</td>
</tr>
</tbody>
</table>
Other Recommendations

- **Pure Tin Leads**
  - All NAND Flash are PEMS, which have pure tins leads. Leads must be retinned or solder-dipped before installation onto flight boards.

- **Disturb Error Mitigation**
  - Limit the number of reads between programming, sequentially program pages in a block, and minimize partial-page programming.

- **Moisture Sensitivity (PEMS Storage)**
  - Plastic packaging is hygroscopic
  - Need to be stored in humidity controlled environments
  - Should be “baked out” prior to assembly to prevent popcorning or other damage

- **Electrostatic Discharge (ESD) Sensitivity**
  - Most NAND Flash devices are classified has having ESD sensitivities of Class 1C (>1000 V HBM) or better.
  - Most standard ESD practices (static dissipative wrist straps, workbenches, and storage bags) will prevent damaging the device.
End of the Road for Flash?

The Bleak Future of NAND Flash Memory

Laura M. Grupp†, John D. Davis‡, Steven Swanson†
†Department of Computer Science and Engineering, University of California, San Diego
‡Microsoft Research, Mountain View
Sources/References


