MRAM Technology and Status

Jason Heidecker
Jet Propulsion Laboratory, California Institute of Technology

Table of Contents

1. Introduction
2. Magnetoresistance
3. State-of-the-Art: MTJ
4. Future: TAS, STT
5. SRAM-like Operation
6. Reliability
7. Radiation Effects
8. Comparison with Other NVM
9. Applications
10. Manufacturers & R&D
11. MRAM Market
12. Product History & Roadmap
13. Flight Heritage
14. Sources/References
What is an MRAM?

**MRAM = Magnetoresistive RAM**

- WRITE using magnetic hysteresis.
- READ using magnetoresistance.
- Built on CMOS. TSOP packages (or ceramic flat-pack for space)
- Architecture similar to SRAM.
- First memory to use magnetic structures exploiting electron SPIN as well as CHARGE.
- Future technologies have potential for very HIGH DENSITIES.
- MEMORY CELLS are nonvolatile (unlimited retention) and immune to radiation-induced upset. Also unlimited endurance.
MRAM: The Ideal Memory?

- DRAM Density
- SRAM Speed
- NAND Nonvolatility
- Rad-Hard Memory Cells

Potential to be first nonvolatile Gb memory with unlimited endurance and 20+ year retention (and SEU immunity bonus)
Spintronics

MRAM, The Spintronic Memory

Traditional Memory

- Bulk Movement/Storage of Electrons

Spintronics

- Exploitation of Electron Spin and Resulting Magnetic Moment

Information is carried by electron spin in addition to, or in place of its charge.
Read: Magnetoresistance (MR)

**Types of magnetoresistance (MR):**

<table>
<thead>
<tr>
<th>Name</th>
<th>Increase in Resistance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ordinary (OMR)</td>
<td>2%</td>
</tr>
<tr>
<td>Giant (GMR)</td>
<td>50%</td>
</tr>
<tr>
<td>Colossal (CMR)</td>
<td>99.9%</td>
</tr>
<tr>
<td>Tunnel (TMR)</td>
<td>200%</td>
</tr>
</tbody>
</table>

*Modern “MTJ” MRAMs*
“Ordinary” Magnetoresistance Effect

Resistance of material changes with applied magnetic field.

Corbino Disc

Magnetic field adds circular current component $I_\theta$ and creates resistance to radial component $I_\rho$.

Also known as “anisotropic magnetoresistance” (AMR) because effect is 0 when current and B are parallel and maximum when perpendicular.

Effect discovered by Lord Kelvin in 1856.

Increased resistance is due to Lorentz Force:

$$F = q(E + \mathbf{v} \times \mathbf{B})$$

Change in resistance is proportional to $B^2$ (Kohler’s Rule):

$$\frac{\partial \rho}{\rho} \propto a \left( \frac{H}{\rho} \right)^2$$
"Giant" Magnetoresistance

**Birth of “spintronics”**

- A much larger magnetoresistance effect (up to 50%) observed in thin-film structures composed of alternating ferromagnetic and non-magnetic layers (e.g. Fe/Cr/Fe). Thicknesses in nm.

- Current passes parallel to layers: current in plane (CIP).

- Resistance of material is affected by alignment of magnetic moments of magnetic materials which creates changes in scattering of spin up or spin down electrons.

- **In practical application as memory cell**, change in resistance is too small (4-8%). Not good enough for high density memory.

**Using pinning layer also known as “spin valve” structure**

**Disc Head Readers**

*Discovered by IBM and published in 1991. Modern MRAM is derivative of this structure.*

The 2007 Nobel Prize in physics was awarded to Albert Fert and Peter Grünberg for the discovery of GMR, which they did (independently) in the 1980s.
“Colossal” Magnetoresistance

- Very large change in resistance under magnetic field observed mostly in certain manganese oxide compounds

- First seen in 1950s by Jonker and Stanten (Philips)

- Effect not well understood

- Materials not to be seen in MRAM (or any other electronics) any time soon

Resistance has recently been discovered in La$_{1-x}$CoO$_x$. The largest effects have been observed for $x=0$, where effects are observed, on the order of $\Delta R/R(H) = 125$. The resistance changes by 99.9%. Figure 14 shows a resistivity of the material undergoes a low temperature. The colossal magnetoresistance effect has been shown that the insulating to metal transition temperature. HP has produced high-quality CMR film with a resistance of about 95%. This resistance reduction is relatively stable over degrees (Figure 16). These results were reported by National Laboratories in February, 1995 [Ref. 8]. The insulating materials is the field dependence of the resistance. These issues will be the focus...
“Tunnel” Magnetoresistance and the MTJ

Magnetic Tunnel Junction (MTJ) Cell Structures

• Two layers of magnetic metal (such as cobalt-iron) separated by a layer of insulator (typically aluminum oxide, ~1 nm)

• Tunneling Magnetoresistance
  – Consequence of spin-dependent tunneling
MTJ Operation

MTJ STORAGE ELEMENT

- S → N (Low Resistance)
- Magnetic layer 1 (free layer)
- Tunnel barrier
- Magnetic layer 2 (fixed layer)
- S → N (High Resistance)

N → S
MTJ Drawbacks

- **Scaling Issues**
  - Smaller bits are more susceptible to thermal fluctuations

- **Complicated Lithography**

1st Gen: MTJ Cell

2nd Gen: STT Cell
MRAM Future: Thermally Assisted Switching (TAS)

• Idea is to heat the cell, which lowers the strength of the required magnetic fields for switching

• Advantages:
  – Eliminates write selectivity problems: write select is temperature driven
  – Lower power: only one magnetic field required for write
  – It is thermally stable due to the exchange bias of the storage layer.

• Main Advocate: Crocus (Spintec spin-off): Just received $300M to build factory in Russia.
MRAM Future: Spin Torque Transfer (STT)

- Advantages:
  - Lower Power Consumption
  - Better Scalability
  - Simpler Cells
SRAM-like Operation

MRAM Read

MRAM Write

SRAM Read

SRAM Write
Device Reliability: 1 Mb Everspin (JPL)

- Unlimited Endurance
- 20+ year Retention
- Low susceptibility to external magnetic fields
- -55 to 125°C operation (E2V upscreen)
  - Sold by Everspin as -45 to 130°C

B field measurements at JPL

Bit Errors Vs B Field

~25 mT
Radiation Effects - JPL

A 1 Mbit MRAM die packaged in a 40-pin dual-in-package (DIP) for SEL testing (top) and thin-small-outline-package (TSOP) for TID testing (bottom).

<table>
<thead>
<tr>
<th>Run #</th>
<th>Device</th>
<th>Energy (MeV/AMU)</th>
<th>Energy (MeV)</th>
<th>Ion</th>
<th>Eff. LET</th>
<th>Run Time (s)</th>
<th>Fluence</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>25</td>
<td>1766</td>
<td>Kr</td>
<td>21.2</td>
<td>177</td>
<td>2.0E+05</td>
</tr>
<tr>
<td>2</td>
<td>1</td>
<td>25</td>
<td>1766</td>
<td>Kr</td>
<td>21.2</td>
<td>242</td>
<td>3.0E+06</td>
</tr>
<tr>
<td>3</td>
<td>1</td>
<td>25</td>
<td>1766</td>
<td>Kr</td>
<td>21.2</td>
<td>45</td>
<td>5.0E+06</td>
</tr>
<tr>
<td>4</td>
<td>1</td>
<td>25</td>
<td>313</td>
<td>Kr</td>
<td>39</td>
<td>54</td>
<td>5.0E+06</td>
</tr>
<tr>
<td>5</td>
<td>1</td>
<td>25</td>
<td>1077</td>
<td>Xe</td>
<td>56</td>
<td>51</td>
<td>5.0E+06</td>
</tr>
<tr>
<td>6</td>
<td>2</td>
<td>25</td>
<td>1077</td>
<td>Xe</td>
<td>56</td>
<td>61</td>
<td>5.0E+06</td>
</tr>
<tr>
<td>7</td>
<td>2</td>
<td>25</td>
<td>1077</td>
<td>Xe</td>
<td>56</td>
<td>62</td>
<td>5.0E+06</td>
</tr>
<tr>
<td>8</td>
<td>2</td>
<td>15</td>
<td>2429</td>
<td>Au</td>
<td>84.1</td>
<td>89</td>
<td>1.0E+07</td>
</tr>
<tr>
<td>9</td>
<td>3</td>
<td>15</td>
<td>2429</td>
<td>Au</td>
<td>84.1</td>
<td>79</td>
<td>1.0E+07</td>
</tr>
<tr>
<td>10</td>
<td>4</td>
<td>15</td>
<td>2429</td>
<td>Au</td>
<td>84.1</td>
<td>54</td>
<td>1.0E+07</td>
</tr>
</tbody>
</table>

Ion beams used for SEL testing. No latchup observed during any testing.
# Memory Comparison

<table>
<thead>
<tr>
<th></th>
<th>SRAM</th>
<th>DRAM</th>
<th>NOR Flash</th>
<th>NAND Flash</th>
<th>FRAM</th>
<th>PRAM</th>
<th>MTJ MRAM</th>
<th>STT MRAM</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Density</strong></td>
<td>144 Mb</td>
<td>1 Gb</td>
<td>1 Gb</td>
<td>64 Gb</td>
<td>4 Mb</td>
<td>512 Mb</td>
<td>16 Mb</td>
<td>Gb?</td>
</tr>
<tr>
<td><strong>Access Time</strong></td>
<td>&lt;1 ns</td>
<td>260 ps</td>
<td>25 ns</td>
<td>20 ns</td>
<td>110 ns</td>
<td>&lt;16 ns</td>
<td>35 ns</td>
<td>&lt;10?</td>
</tr>
<tr>
<td><strong>Standby I (mA)</strong></td>
<td>2</td>
<td>150</td>
<td>&lt;1</td>
<td>&lt;1</td>
<td>&lt;1</td>
<td>&lt;1</td>
<td>&lt;1</td>
<td>&lt;1</td>
</tr>
<tr>
<td><strong>Read I (mA)</strong></td>
<td>100</td>
<td>1000</td>
<td>20</td>
<td>25</td>
<td>&lt;10</td>
<td>16</td>
<td>30</td>
<td>15?</td>
</tr>
<tr>
<td><strong>Write I (mA)</strong></td>
<td>100</td>
<td>1000</td>
<td>50</td>
<td>25</td>
<td>&lt;10</td>
<td>20</td>
<td>30</td>
<td>15?</td>
</tr>
<tr>
<td><strong>Endurance</strong></td>
<td>Infinite</td>
<td>Infinite</td>
<td>100k</td>
<td>0.5-100k</td>
<td>$10^{14}$</td>
<td>$10^6$</td>
<td>Infinite</td>
<td>Infinite</td>
</tr>
<tr>
<td><strong>Retention</strong></td>
<td>~0</td>
<td>~0</td>
<td>~0</td>
<td>&gt;10 yrs</td>
<td>&gt;10 yrs</td>
<td>&gt;10 yrs</td>
<td>&gt;20 yrs</td>
<td>&gt;20 yrs</td>
</tr>
<tr>
<td><strong>Cell Size (F^2)</strong></td>
<td>100</td>
<td>8</td>
<td>6</td>
<td>5</td>
<td>10</td>
<td>6</td>
<td>10</td>
<td>&lt;4?</td>
</tr>
<tr>
<td><strong>Rad-Hard Cell</strong></td>
<td>✗</td>
<td>✗</td>
<td>✗</td>
<td>✗</td>
<td>✔</td>
<td>✗</td>
<td>✔</td>
<td>✔</td>
</tr>
</tbody>
</table>
Applications

Wherever nonvolatility, quick booting, high endurance, and/or radiation-hardness are important.

- **Home Computing**
  - Quick boot discs, similar to Flash

- **Mobile Computing**
  - Nonvolatility

- **Military/Space**
  - Nonvolatile, Rad-Hard

- **RFID**
  - Embedded MRAM
MRAM Players (Past and Present)
# MRAM Areas of Focus

## Commercial MTJ Vendors
- Everspin
- E2V (Everspin Upscreen)

## Commercial Rad-Hard MTJ
- Honeywell
- Aeroflex

## MTJ IP
- NVE
- Spintec

## Thermally Assisted Technology (TAS) R&D
- Crocus, IBM
- Spintec

## Inactive
- Motorola (2005, spun off Freescale)
- Freescale (2008, spun off Everspin)
- Infineon (~2006)
- Cypress (2005)

## Spin Transfer Torque (STT) R&D
- IBM
- Samsung
- Hynix-Grandis
- Everspin
- Avalanche Technology (CA start-up)
- Spin Transfer Technologies (NYU start-up)
- Intel
- NEC
- Renesas
- Fujitsu
- Toshiba
- Micron, A*Star (Singapore)
though there might be other concurrent players in the non-volatile segment, MRAM will still have the maximum share of the memory market.

**MRAM Market**

![Pie Chart](image)

**MRAM Compared to Other Nanotechnologies**

![Graph](image)

**3.2 Funding resources:** Throughout the past decade, many companies as well as research centers have been receiving constant funding from government agencies as well as other sources like...
## MRAM Product Roadmap

<table>
<thead>
<tr>
<th>Year</th>
<th>Device</th>
<th>Manufacturer</th>
</tr>
</thead>
<tbody>
<tr>
<td>2004</td>
<td>4 Mb MTJ</td>
<td>Freescale</td>
</tr>
<tr>
<td>2005</td>
<td>1 Mb MTJ Rad-hard</td>
<td>Honeywell</td>
</tr>
<tr>
<td>2005</td>
<td>STT MRAM Prototype</td>
<td>Sony</td>
</tr>
<tr>
<td>2009</td>
<td>32 Mb STT MRAM Prototype</td>
<td>Hitachi</td>
</tr>
<tr>
<td>2010</td>
<td>4/16 Mb MTJ Rad-hard</td>
<td>Aeroflex</td>
</tr>
<tr>
<td>2012?</td>
<td>16/64 Mb Rad-hard QML Class V</td>
<td>Aeroflex/Honeywell</td>
</tr>
<tr>
<td>2015?</td>
<td>Gb STT</td>
<td>Toshiba</td>
</tr>
</tbody>
</table>
Flight Heritage - SpriteSat

- SpriteSat – Tohoku University, Japan
- Various Payloads/Launches Since 2008
- 4 Mb Freescale devices
- Replacing Flash and SRAM with MRAM

Flight Heritage – CubeSat - COVE (JPL)

- Launch October 2011
- CubeSat On-board Processing Validation Experiment, “COVE”
- Secondary Payload on University of Michigan M-Cubed CubeSat
- Included:
  - Xilinx Virtex-5QV FPGA
  - Everspin MR4A16B MRAM (4 Mb)
  - Numonyx P5QPCM PRAM (128 Mb)
- First attempt: NPOESS Preparyory Project (NPP)
- M-Cubed did not separate from another CubeSat, Explorer 1-Prime
  - Although beacons have been heard, University of Michigan team has been unable to send commands to satellite.
Sources/References

7. NVE/Daughton, J. “Magnetoresistive Random Access Memory (MRAM).”