

Initial SEE Testing of Maestro

Steven M. Guertin

Jet Propulsion Laboratory / California
Institute of Technology
Pasadena, CA

This work was performed at the Jet Propulsion Laboratory, California Institute of Technology,
Under contract with the National Aeronautics and Space Administration (NASA)
This work was funded by the NASA Enabling Technology Development and Demonstration program (ETDD)

Overview

- + Present initial single-event effects (SEE) test results for the Opera program's Maestro 49-core processor
 - Testing at TAMU in 6/2011 and 9/2011
 - Testing at NSRL in 3/2012 and 5/2012
- + Discuss how this fits into the larger picture of full SEE evaluation of Maestro
- + Provide details about test methods and results to enable understanding of what was tested and what the sensitivities are

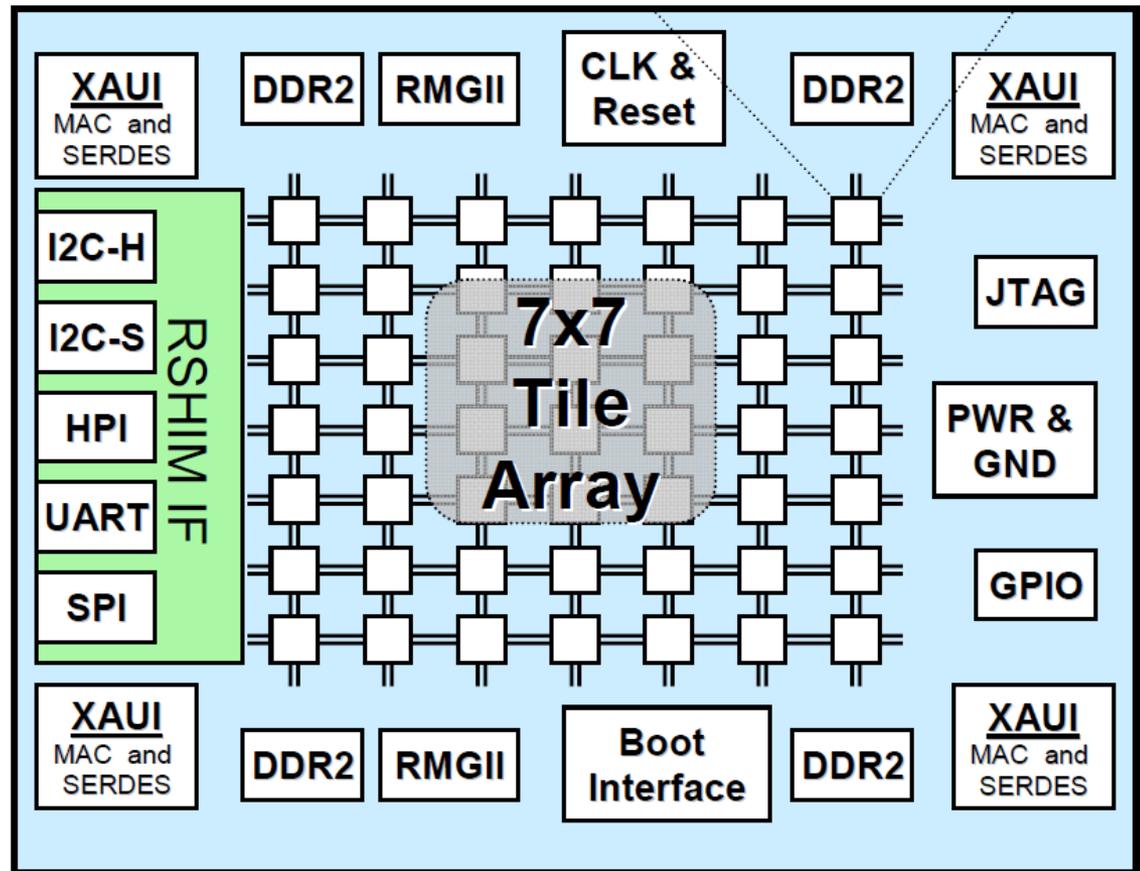
Maestro

✦ Opera's 49-core manycore microprocessor built by Boeing

- 49 processor tiles
- 5 on-chip networks
- 4 MMUs
- 4 XAUI ports
- Other slower interfaces

✦ RHBD to support certain applications

- IBM 90nm



Overview of SEE Testing

- + SEE testing concerns the sensitivity of electronic circuits to the passage of individual ions.
 - Caused directly by heavy ions
 - Or indirectly by scattering of lattice ions
- + Traversing ions liberate electrons and holes which result in a collected charge, Q

$$Q = \int \frac{L\rho}{W} dx$$

Effects include:

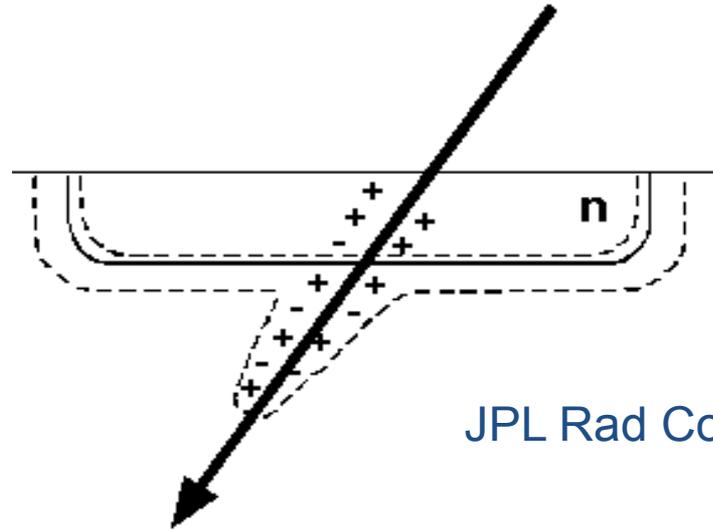
Single Event Latchup (SEL)

- short from power to ground

Single Bit Upset (SBU)

- flip of a bi-stable element

Single Event Transient (SET); Gate Rupture, Burnout, etc...



JPL Rad Course 2004

Test Approach

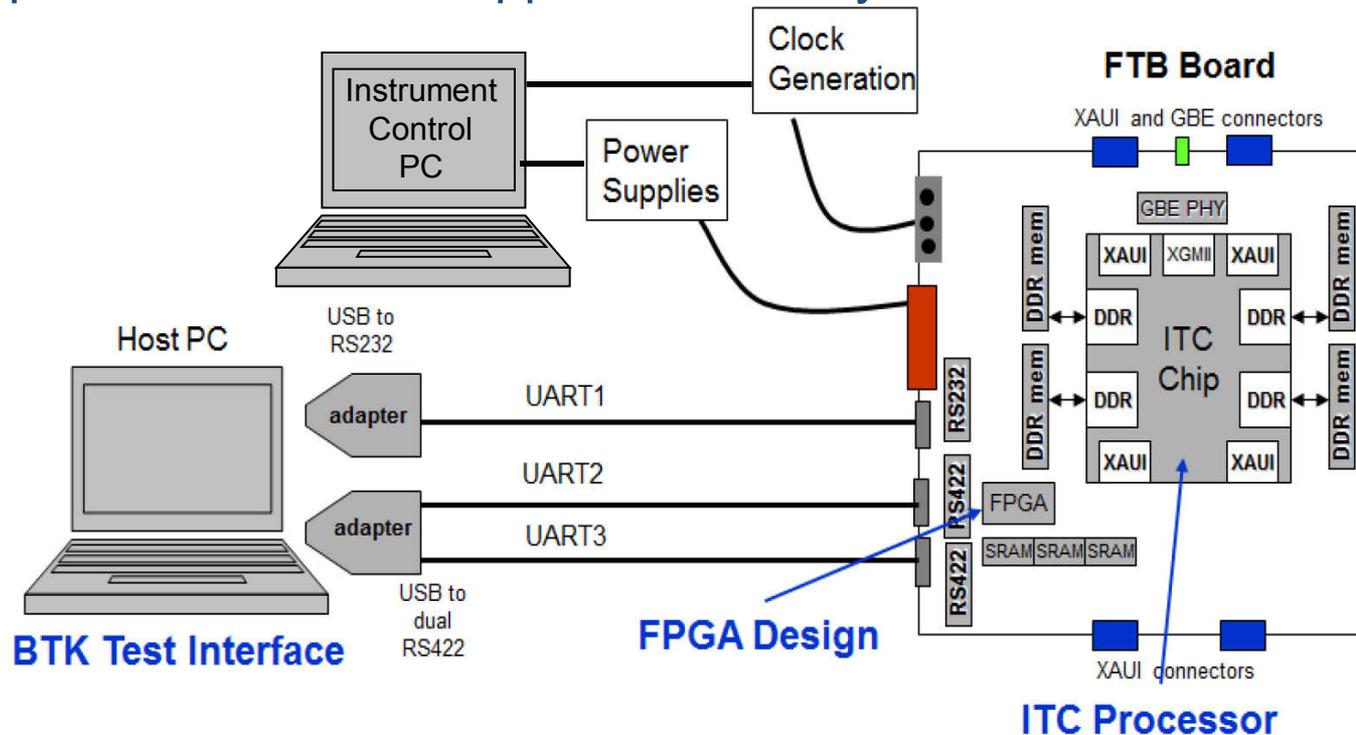
- + Testing so far targeted the first phase of a 3-phase approach
 - + Phase 1 – basic structures
 - Memory cells, latches, basic processor operations
 - Global operational issues (if observable)
 - + Phase 2 – peripherals and interconnects
 - On-chip networks, MMU, XAUI, etc
 - + Phase 3 – hypervisor/operating system – response of flight-like systems
 - Ensure system response is consistent with findings from Phases 1 & 2 (no surprises)
-  ← where we are

Phase 1 Test Approach

- + Identify tile-level sensitivity to SEE
 - Register static upset risk
 - + i.e. not using the register > 99% of the time
 - Register dynamic upset risk
 - + while using the register to perform calculations through the ALU
 - L1 static cache sensitivity
 - L2 static cache sensitivity
 - + Observe system-level SEE sensitivity (qualitatively)
 - Notice if system level upset behavior consistent with tile upsets, or located in a particular element
 - + (Sensitivity includes PLL, MDN, TDN, and UDN)
- 

Test Hardware/Setup

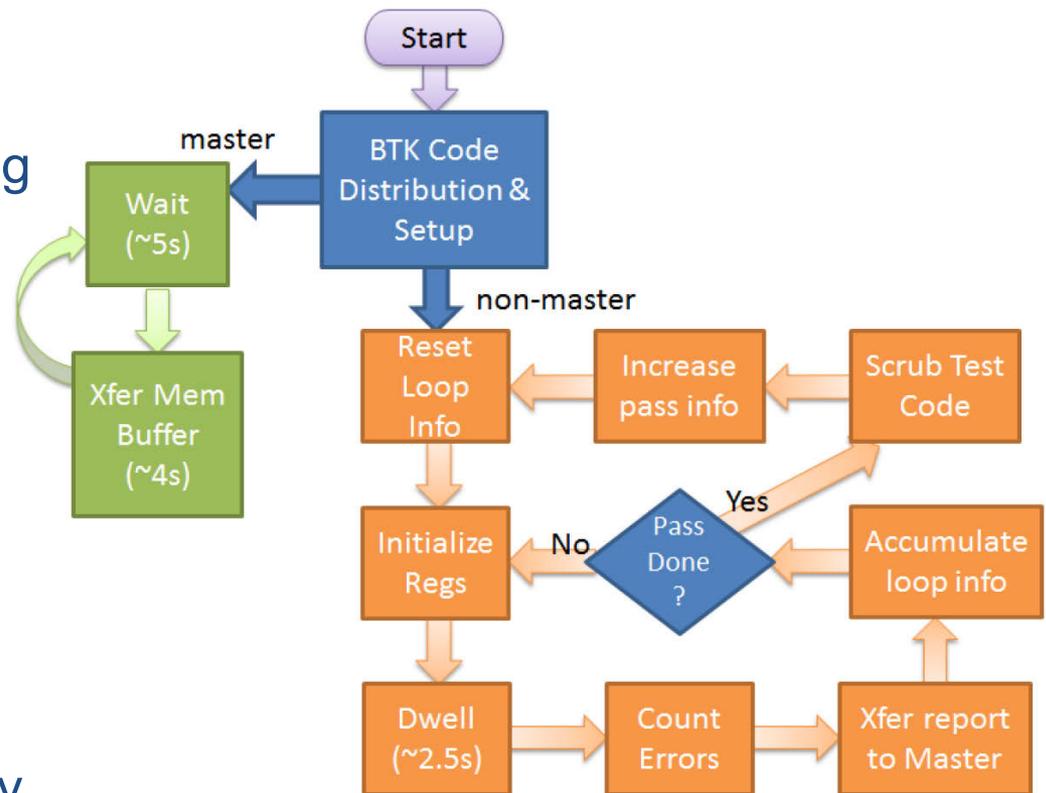
- ✦ Testing was performed using Boeing's Functional Test Board (FTB)
 - FTB used had no external hardware for Maestro (i.e. no memory)
 - Maestro device mounted with ZIF socket
- ✦ All power and clocks supplied externally and monitored



General Test Software Structure

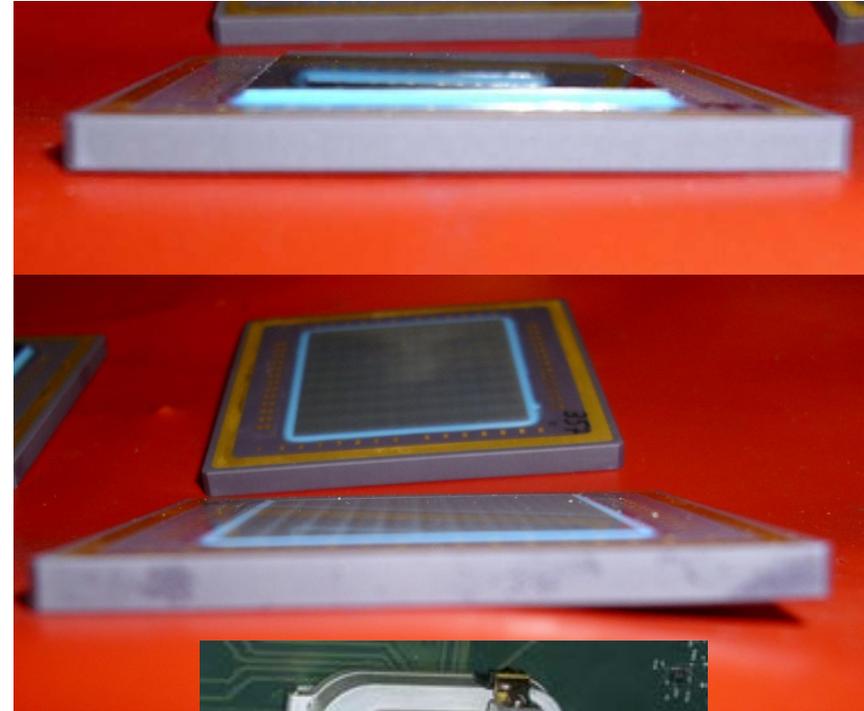
- ✦ Software was based on the Tileria Board Test Kit's basic multicore test modified as follows
 - Master tile no longer performs the test itself
 - Test tiles perform testing in infinite loop
- ✦ Due to lack of off-chip memory, all test code and report data is stored on the master tile (accessed by memory accesses)
- ✦ All code written in assembly

Primary test software structure



Test Setup Challenges

- + Lack of on-board memory
 - Requires use of L2 cache on master for code storage
- + Test fluxes need to be high to get counts
 - RHBD devices are designed to have low sensitivity, and we need to test for it
- + Master tile must be shielded
- + Test devices must be thinned for testing at Texas A&M

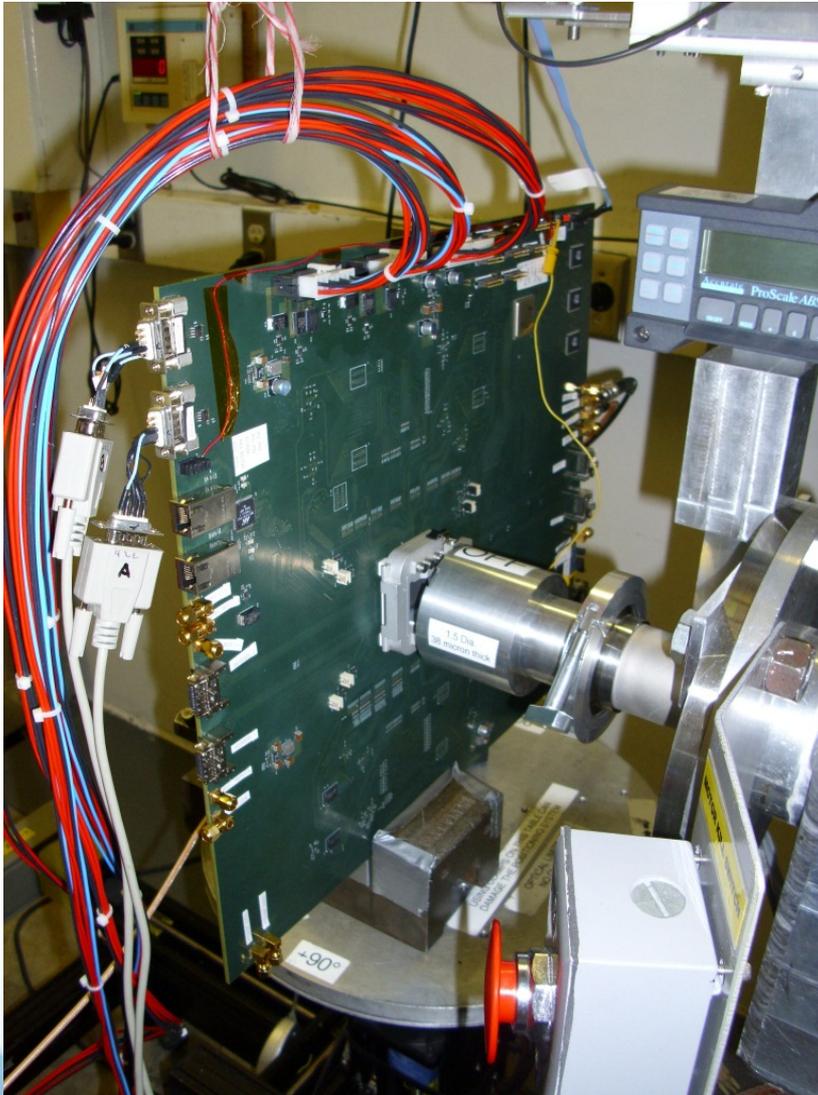


Limitations on Testing

- + Lack of on-board memory
 - Local double-bit error on L2 tag results in unhandled cache miss
 - **Tile Crash**
- + High test fluxes
 - Double-bit errors in L1 cache are undetected and may result in changes to running test code - **False Counts and/or Tile Crash**
- + Shielding
 - Results in overlap, meaning only 35 tiles are being tested
- + DUT is in a large socket
 - Limits testing to only normal-incident ions
- + All of these combine to form a limit on the sensitivity of the testing...

Tile Crashes indicated here are due to ground test conditions and are not indicative of error modes expected in space use

Testing Performed at TAMU

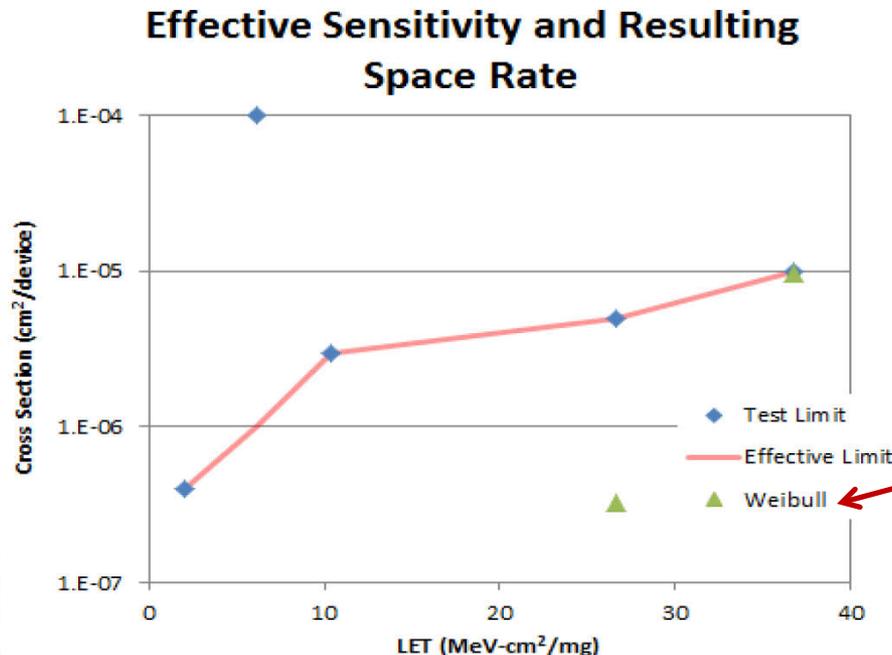


- ✦ Testing performed in air at TAMU
 - DUT not hot enough to require cooling (I/O interfaces not active)
- ✦ Tested with beams from LET = 2 MeV-cm²/mg to LET = 80

Ion & Energy (MeV/amu)	LET (MeV-cm ² /mg)	DUT 357 Exposure (#/cm ²)	DUT 327 Exposure (#/cm ²)
Ne-15	2	6.9x10 ⁵	7.4x10 ⁶
Ar-25	6.2	2.8x10 ⁶	1.2x10 ⁶
Ar-15	10.4	n/a	1.7x10 ⁵
Cu-15	26.6	n/a	8.9x10 ⁵
Kr-15	36.7	n/a	2.9x10 ⁵
Xe-25	46	2.2x10 ⁵	n/a
Au-15	80	1.8x10 ⁷ (2.8x10 ⁴ for non-SEL)	n/a

Testing Sensitivity

- ✦ A semi-quantitative limit on test sensitivity was established for the testing performed.
- ✦ Limit set at approximately $2.5 \times \sigma_{\text{Tile-Crash}}$
 - This is approximately the point where 20% of tiles crash – which is similar to the false count
 - This number is established quantitatively, but is also reviewed qualitatively and might be a little subjective



“reasonable” estimate of sensitivity of undetected event type – approximately 2×10^{-6} /device-day if no events seen (Adams 90% Worst Case GEO environment)

Single-Event Latchup Results

- + We collected data on SEL in a limited way
 - Nominal operating conditions used (usually you would want high bias and high temperature)
 - We were unable to keep the processor running while irradiating with very high flux (i.e. the tiles all crashed very early during SEL runs)

 - + No SEL observed
 - Exposed to Au ions with LET = 80 MeV-cm²/mg
 - Total fluence exposure was 1.8x10⁷/cm²
- 

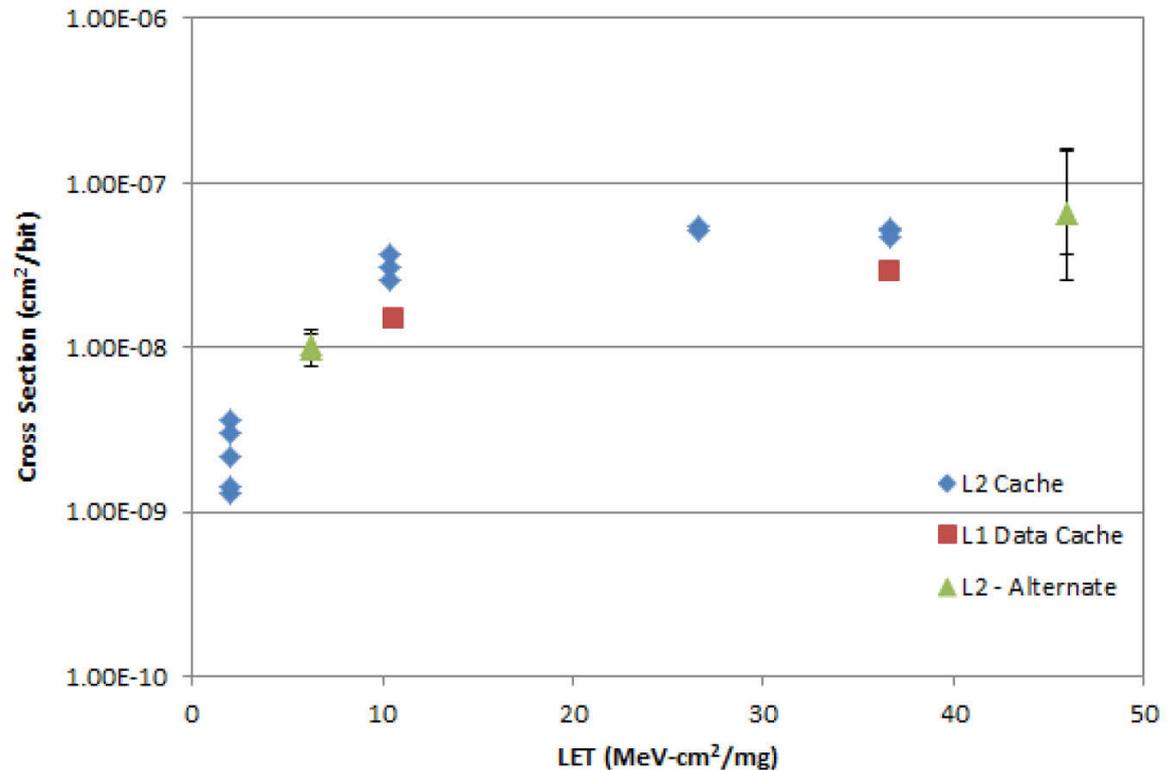
Testing Cache Bits

- + General cache test algorithm (for test tiles)
 - 1. Load cache with known pattern
 - 2. Dwell for ~2.5 seconds
 - 3. Check pattern and report errors by MDN (<100ms)
 - 4. Go To 1
- + L1 cache testing – data cache only
 - Known pattern was all '0's or all '1's
 - Ignored cache parity interrupts (disabled)
- + L2 cache testing
 - Test code used as data pattern
 - Scrub routine counted errors
 - (Also used a method similar to L1 in early testing)
 - Data analysis requires de-convoluting EDAC scheme – i.e. we only see double-bit upsets

Cache Test Results

- + Results from all test algorithms fairly consistent
- + Smaller cross section in L1 cache may be due to error in normalization (# of bits tested * exposure time)
- + Results very similar to reported sensitivity of Artisan™ SRAM

SEE Sensitivity of the L1 and L2 Cache Bits



Static Register Test Results

- + Algorithm is very similar to the caches
 - As many of the 64 registers as possible are loaded with all '0's or '1's.
- + Two types of errors could occur:
 - SBU – bit upsets where a single bit changes
 - + Only 1 candidate event seen – inconclusive
 - Clobber – the value of the register changes and is no longer similar to the load pattern
 - + All candidate events occurred during a time when algorithm is more susceptible to L1 double bit errors - inconclusive
- + Register upsets concluded to be at lower sensitivity than reached by this testing.

Inconclusive results indicate the event has been shown to be below the test sensitivity

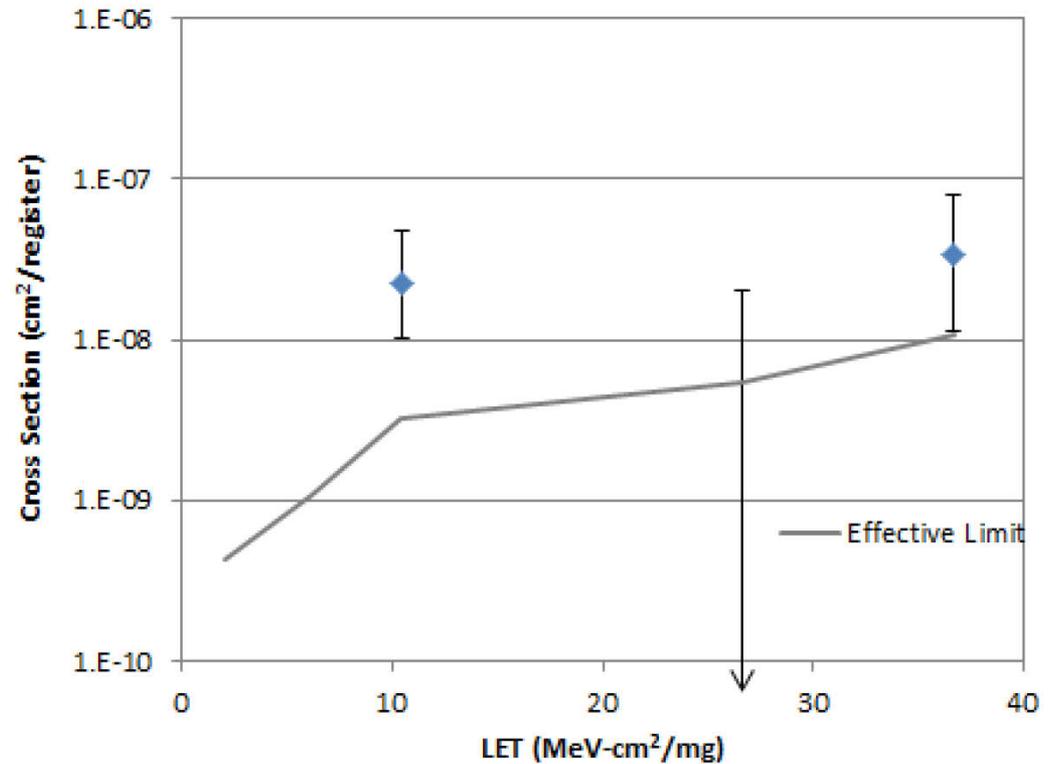
Testing Registers Dynamically

- + Dynamic register testing is really an attempt to characterize ALU operations for sensitivity
 - Desire is to have ALU(s) operating near full capacity (pipelines full, multiple instructions executing)
- + Algorithm
 - 19 registers were loaded with known values
 - Bundled operations were performed to increase usage (i.e. {
move r0, r1; move r1, r0 } //swap r0,r1)
 - Operations were performed many times (for ~2 seconds)
 - After repeated operations complete, the 19 registers were compared to expected values

Dynamic Register Test Results

- + SBU – only 1 candidate event seen (inconclusive)
- + Clobber – 5 events seen, distribution in time suggests they were not false positives
 - But result is still very close to the detection threshold

Effective Sensitivity vs. Dynamic Clobber



Comparison to Predictions

- + Boeing has predicted event rates for various parts of the Maestro chip.
- + For the components of the Maestro design tested, we have the following comparisons

Event Type	Approximate Rate (#/day in GEO)**	Approximate Predicted Rate
Reg static SBU	Below 6×10^{-11} /bit-day	Consistent
Reg static clobber*	Below 2×10^{-6} /day for 912 registers	Consistent
Reg dynamic SBU	Below 6×10^{-11} /bit-day	Consistent
Reg dynamic clobber	Between 7.8×10^{-5} and 2×10^{-6} /device-day	Predicted Rate ~10x Too High
L2 SBU	1.6×10^{-6} errors/bit-day (25/device-day)	Same
L1 SBU	1.6×10^{-6} errors/bit-day (15/device-day)	Same

- + The observed radiation sensitivities are consistent with predictions
 - (the register dynamic clobber rate predicted is a little conservative – but the sensitivity may increase with clock)

Future Work

- ✦ The level of sensitivity achieved in the TAMU testing is insufficient for some of the predicted sensitivities.
 - Test code could be improved to reduce crash rates by performing scrubbing more often.
 - Testing with a board with DDR2 memory would also enable improved sensitivity (thus it may be best to test with updated hardware that can also support peripheral testing).
- ✦ The testing performed here should also be repeated at a frequency more appropriate to Maestro (we used only 100MHz)
- ✦ The present testing only covers Phase 1 of the larger plan. It is recommended to proceed to Phase 2 (networks and peripherals)
 - Testing of on chip networks is recommended (during this testing some corruption was seen, but code was not adequate to measure sensitivity) – this is a key area of interest
 - Peripheral interfaces including the memory controllers and XAUI
- ✦ Angular results are much more important on RHBD devices due to multi-node strike sensitivity. This should be tested.

Conclusion

- + We have reported on initial SEE sensitivity of the full 49-core Maestro device
 - Supporting the low-level structures and qualitative system observation goals of phase 1 of testing
- + Observed sensitivities found to be consistent with Boeing predictions
 - Highlighted by the L1 data cache sensitivity which drives the rates on the current Maestro device
- + Presented details to the hardware and software setups that show where the limitations – highlighting future work
 - Key future work includes testing with memory and IO ports