



DDR2 Device Reliability Update

Steven M. Guertin

Jet Propulsion Laboratory / California Institute of Technology
Pasadena, CA

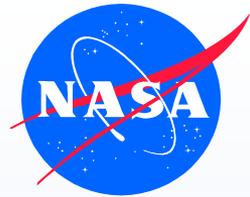
This work was performed at the Jet Propulsion Laboratory, California Institute of Technology,
Under contract with the National Aeronautics and Space Administration (NASA)
This work was funded by the NASA Electronic Parts and Packaging Program (NEPP)

Copyright 2012 California Institute of Technology. Government Sponsorship is acknowledged.



Outline

- Background
- Reliability Qualification Approach
- Test Equipment
- Recap of Last Year's Results
- Initial DIMM Results

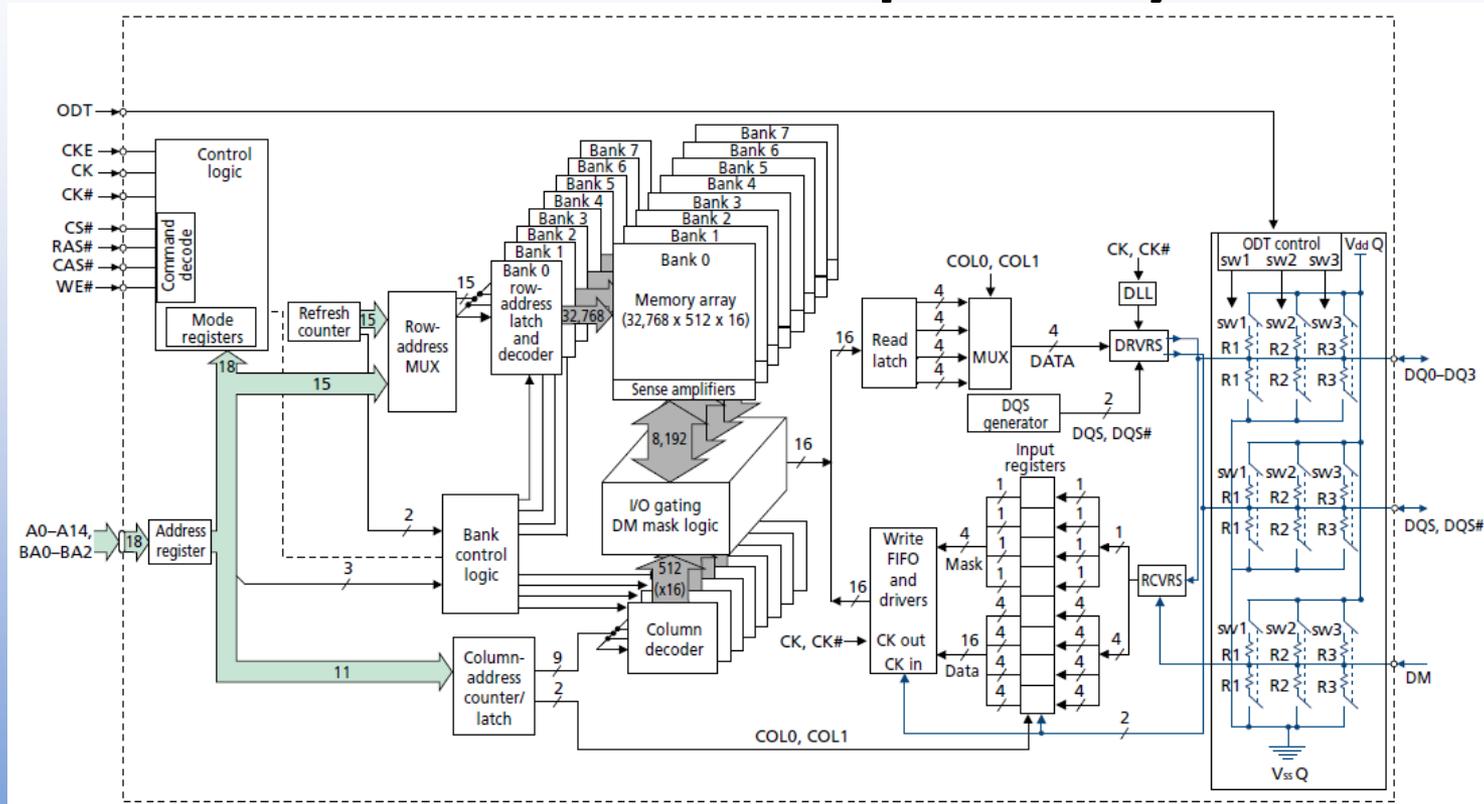


General Reliability

- General reliability is interested in the failure modes that will manifest as a result of any environment, age, or usage parameters
- But manufacturers devote significant resources to testing these devices – why do we need to test, and how are we different?
 - On a device-by-device basis, we have much more time to screen all parts.
 - Ability to identify outlying devices is a useful screening method that can be applied to devices used in space
 - Certain parameters of NASA use may be outside of standard usage – long life, extreme environments, off-spec sheet use
 - We need to be knowledgeable about running these devices to support program questions



Device Complexity



- Many different types of structures:
 - DRAM Cells, Registers, Buffers, Drivers, Voltage Regulators, Charge Pumps, Functional blocks: CRC, Pipelines, State Machines
 - Each has its own failure risk and parameter dependencies



Approach

- Use acceptance testing to establish outliers
 - 100's of test hours per device possible
 - Compared to minutes or less by manufacturer
- Perform accelerated life testing
 - Establish failure mechanisms of a given lot
 - Determine if the lot meets requirements



Test Matrix

$$X(p, M, F(t), Pat(t), V, T, f, D, S(t)) = \begin{cases} Pass / Fail \\ Range \\ Limit \\ \# Counts \end{cases}$$

- General reliability testing covers a vast set of target parametrics and operating parameters
 - p – parameter (e.g. data access time)
 - M – device mode
 - F(t) – device function during test
 - Pat(t) – data pattern during test
 - V – operating bias
 - T – environment temperature
 - f – clock rate
 - D – duty cycle
 - S(t) – stress history of device
- In addition:
 - # of test devices in sample
 - # of desired manufacturers
 - # of test lots

General reliability test matrix is intractable - it requires targeted selection of tested elements.



Things to Measure

- Presently we do the following
 - Monitor current under different operating modes
 - Extract the cell retention time
 - Examine changes over 1000 hour stress test
- We are working towards (up-screen/life test)
 - Examine leakage current on I/Os
 - Determine output voltages
 - Determine the operating frequency range
 - Run pattern-based screening tests



Pattern Dependency

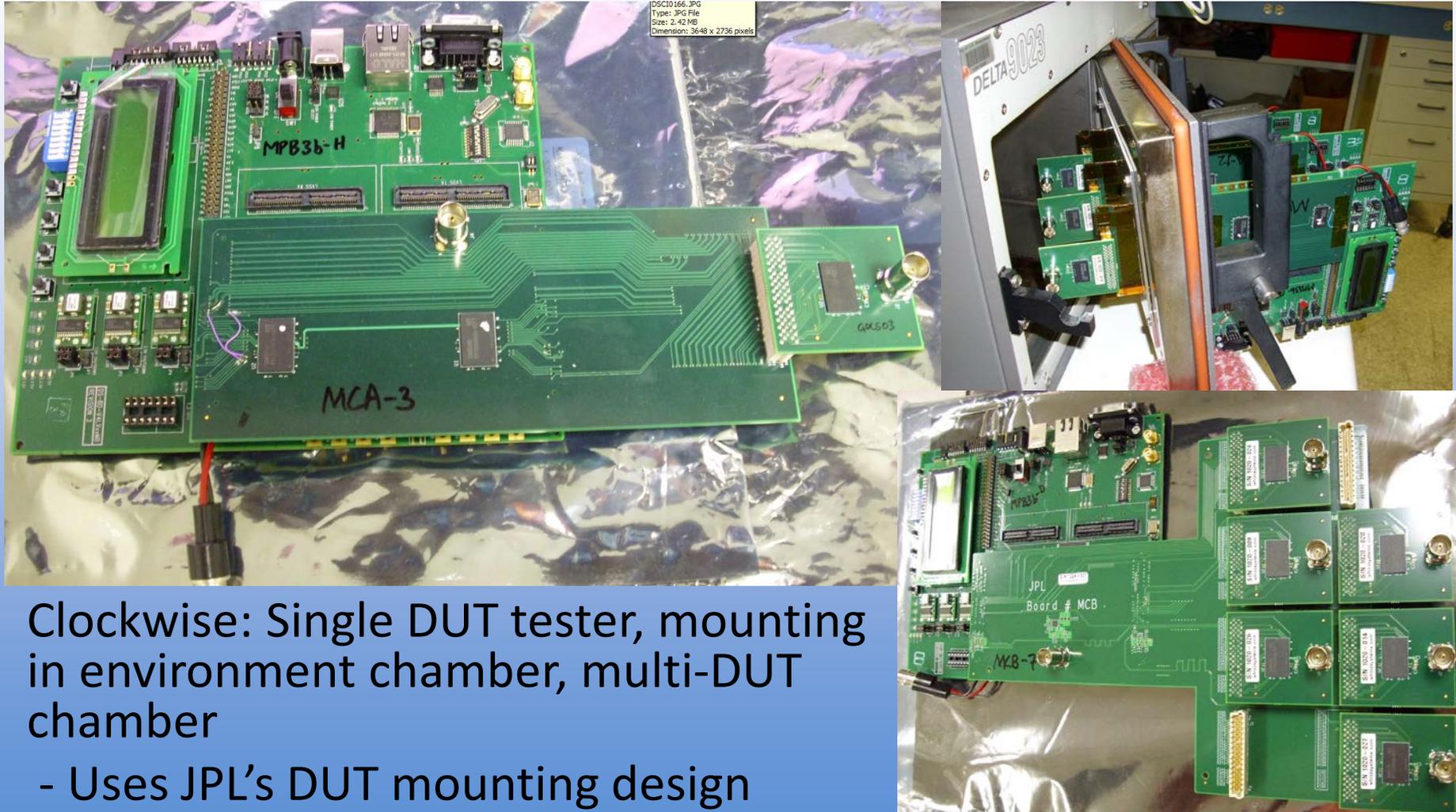
- DRAM storage arrays may have complex pattern dependency
 - Time intensive
 - Huge space of potential patterns
 - Cell retention can be related to pattern used
- Will be invaluable for handling flight anomalies
 - Any observed pattern dependencies during testing can be applied to flight
 - Ability to rule out reliability at a source of flight anomalies is useful



Moving to DIMMs

- Pros
 - Very low cost per device (~10\$ vs. ~200\$)
 - Interchangeable between testers (standard)
 - Enables many types of testing to establish device details
- Cons
 - Impossible to measure individual power
 - All devices on same DIMM in same exposure group
 - Difficult to get desired device parameters
- Bottom Line
 - Will provide a good way to sample many different types of issues
 - May provide good data but are not a vehicle for buying flight parts
 - Test equipment may be viable for flight acceptance...

Test Resources @ JPL



Clockwise: Single DUT tester, mounting
in environment chamber, multi-DUT
chamber

- Uses JPL's DUT mounting design

Test Resources @ JPL

- Credence D10 is a high-capability tester (up to 400MHz, but not well suited to run DUTs at high speed due to expense of interface board)
- Good for testing detailed timing parameters, leakage currents, and I/O voltage levels.
- Life testing, high speed operation, and pattern-dependent characterization of devices will still require other resources



Plan to have this online for individual parts in August 2012

Eureka Tester

- Added an industrial DDR2 DIMM tester
 - Performs standard acceptance tests on DIMMs
 - Frequency range, standard pattern sensitivity



- Also built adapter between loose test parts
 - Interchangeable with functional & parameter testers

DIMM Adapter

- Built adapter to connect to custom test system
- Will be used to perform:
 - Cell retention time studies with several patterns
 - Enable testing in thermal chambers up to 9 DIMMs at a time



Interoperability

- Loose parts:
 - Can work on all systems with use of DIMM adapter –



- DIMMs:
 - Can only be used on industrial tester (Eureka) and JPL memory functional tester



Last Year's Testing

- Test Matrix: 78nm 2Gb DDR2 devices

		Samsung	
		25C	125C
1.8V	X	3 DUTs - (complete) (Set 4)	
2.7V	3 DUTs - (complete) (Set 2)	3 DUTs - (complete) (Set 1)	

		Micron	
		25C	125C
1.8V	X	3 DUTs - (complete) (Set M5)	
2.7V	4 DUTs - (complete) (Set M3)	5 DUTs - (complete) (Set M4)	

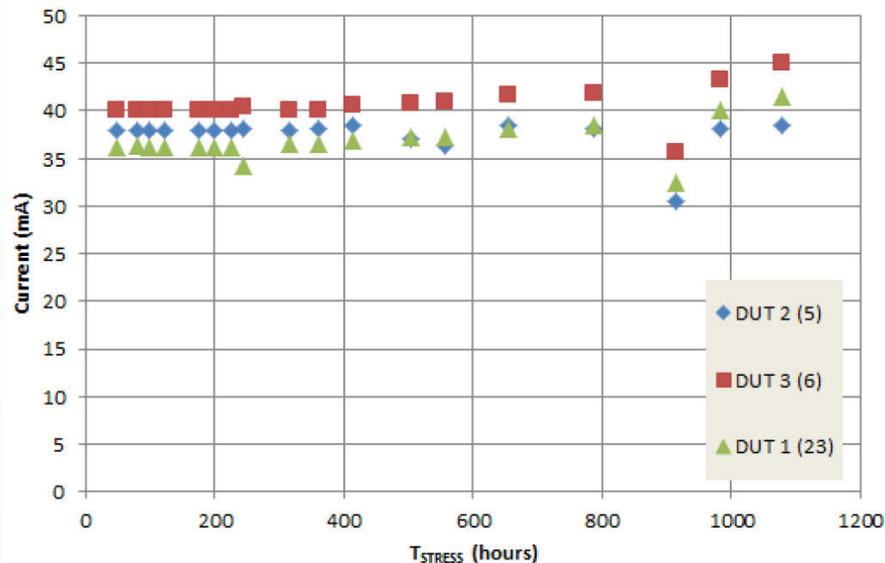
- Testing at 2.7V hindered by internal regulation
- Micron devices at 2.7V had 3 failures, but the statistics are low



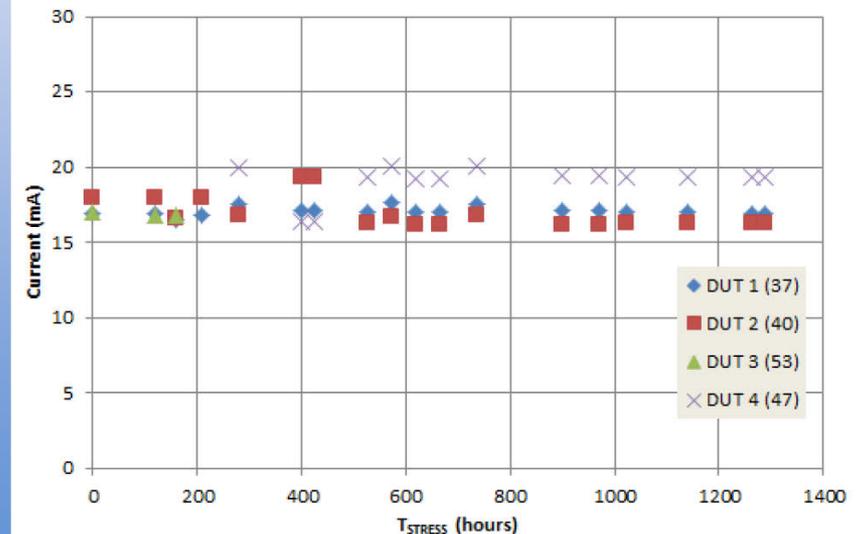
Minor Device Degradation

- Observed operational currents did not degrade significantly over 1000 hours at 2.7V and/or 125°C
- Abrupt jumps due to difficulty with 2.7V Operation

Samsung-1: 2.7V/125C I_{DD3N}

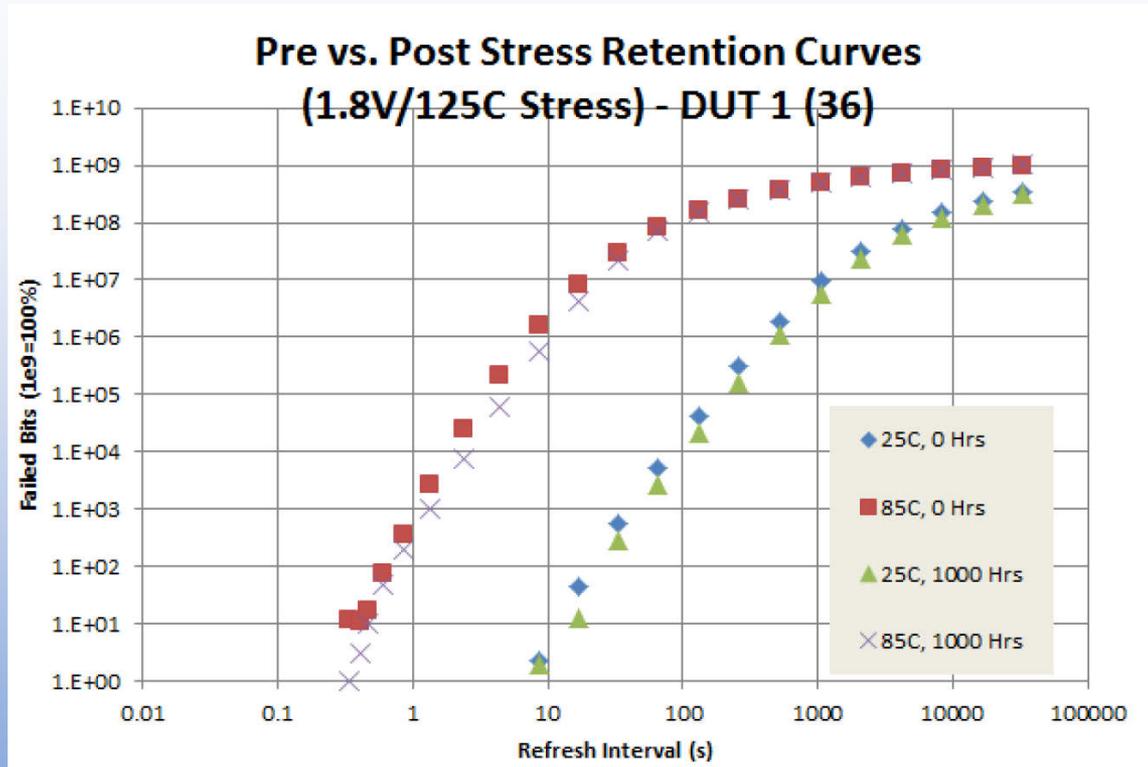


Micron-3: 2.7V/25C I_{DD3N}





Test Efforts



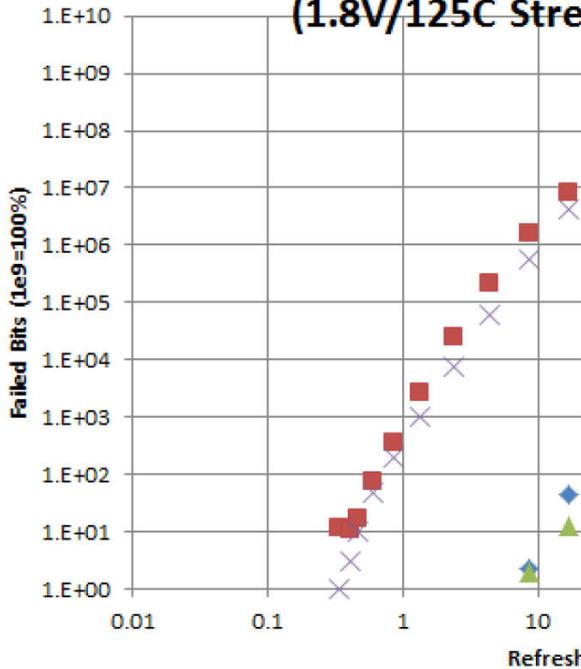
- Micron – Typical 125°C behavior
- Limited imprinting was apparent in Micron devices

25°C Measurement has thermal uncertainty (Explains change at 25°C)

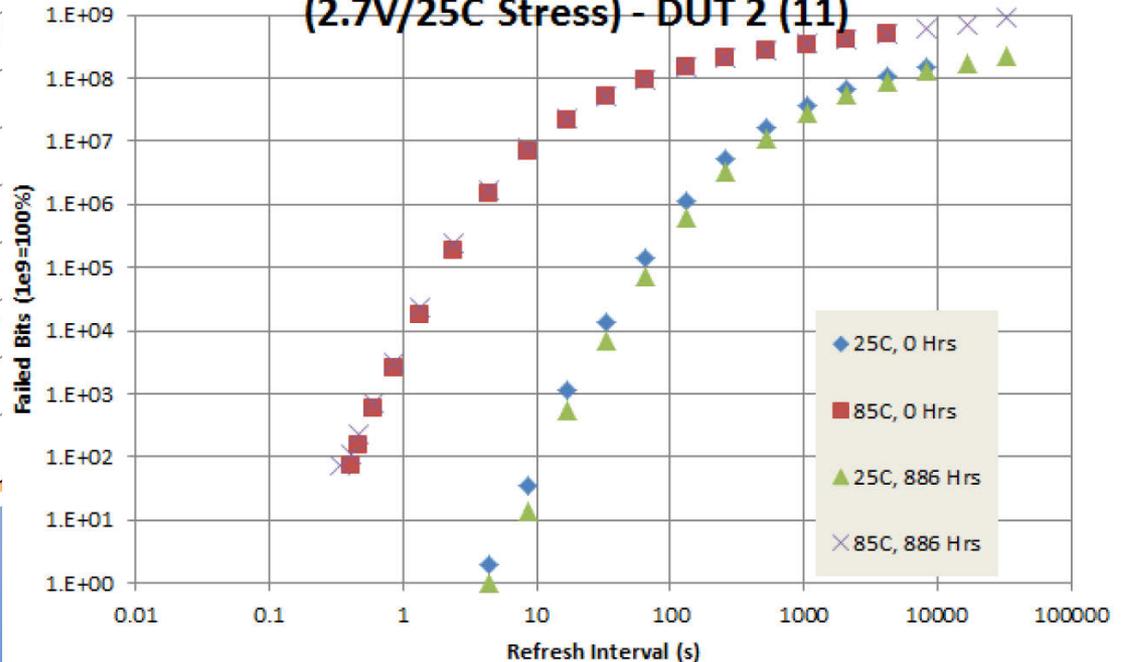


Test Efforts

Pre vs. Post Stress Retention Curves
(1.8V/125C Stress) - DUT 1 (36)



Pre vs. Post Stress Retention Curves
(2.7V/25C Stress) - DUT 2 (11)



- Micron – Typical 125°C behavior
- Limited imprinting was apparent in Micron devices
- Samsung – Typical
- Pre/Post Stress – No apparent change



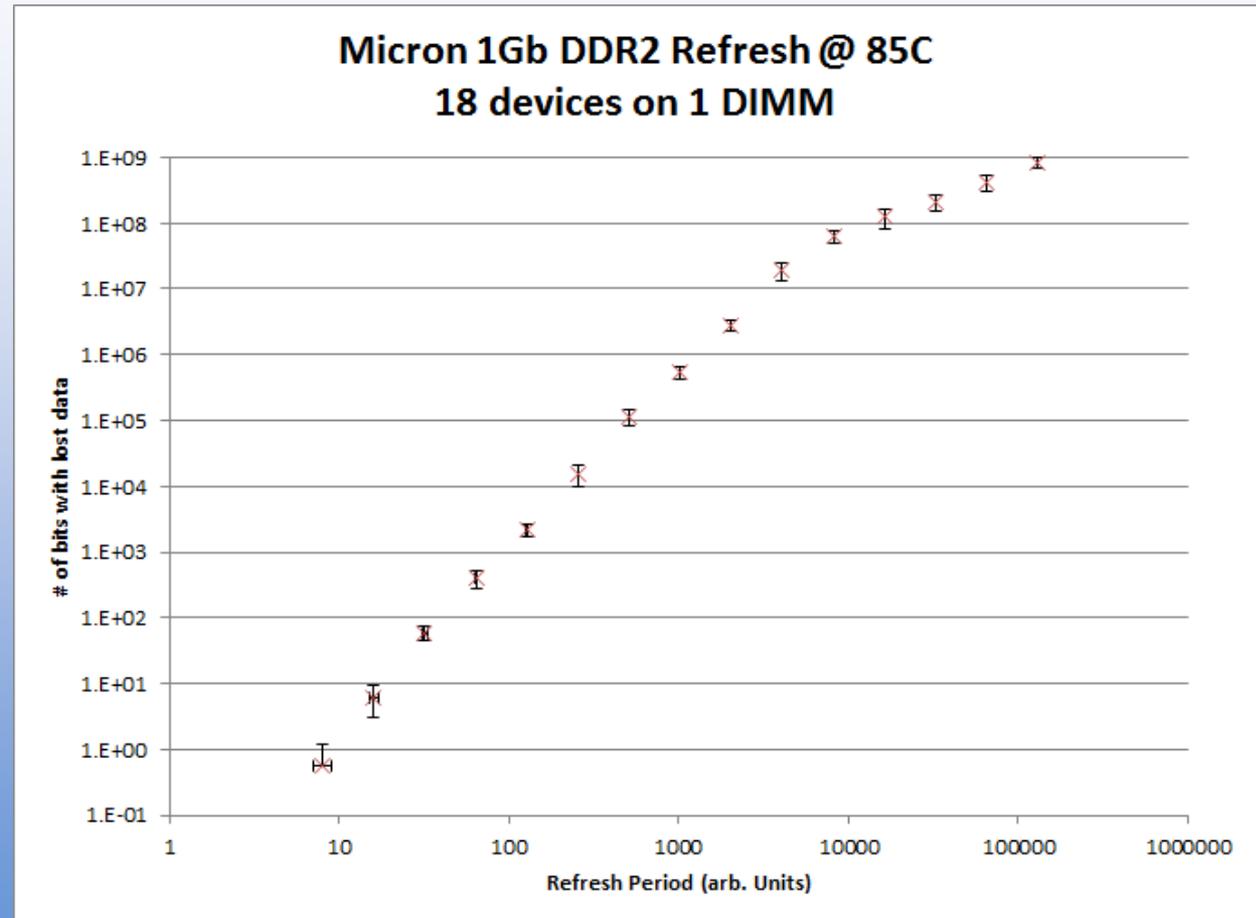
Summary of Results

- Performed 1000 hour testing at 1.8 and 2.7 V as well as 25 and 125°C
- Acceleration showed no significant changes until device failure
 - Failures are a significant result, but they are not hinted at by precursor degradation
- Failure likely due to out-of-spec operation
- Device characterization somewhat limited
 - Made us reexamine the test approach
- Examination for mechanisms limited
 - Device expected degradation modes unknown
 - Intractable matrix for examining mechanisms
- **Limited ability to factor out test conditions**



Initial DIMM Results

- With 16 test devices on each DIMM, statistical significance is quickly reached.
- Outliers are identified quickly
 - & differences in pattern dependency
- Thermal control is very important





Future Directions

- Widen scope of target devices
 - Continue efforts to identify potential DDR2 devices
 - Migrate to DDR3 soon
- Increase test capabilities
 - Development of operating codes and protocols for equipment
 - Credence
 - Eureka
 - Functional tester
- Increase cross-NEPP support
 - New DIMM-based and loose-die based form factors will be more flexible to synergize with GSFC efforts



Conclusion - I

- Qualification approach seeks to provide useful data for NASA programs
 - NASA-Specific and Program-Specific acceptance testing
 - Develop understanding of device family to identify outliers
 - Perform limited life testing
- Reliability test matrix is too big
 - DDR devices are essentially complex ICs with many subcomponents
 - Building additional capabilities to support more testing
 - Test plans must be based on sampling and key measurements
- DUT options and interchangeability
 - Building fully interchangeable system for testing loose devices
 - Making test systems support DIMMs as well



Conclusion - II

- Test hardware development
 - Functional test system to support many DIMMs at once
 - Parametric testing of loose devices with Credence coming online
 - Incorporating industrial acceptance test hardware for DIMMs
- Test efforts
 - Last year's 78nm parts highlighted need for more characterization
 - Testing targeted static pattern at 125C/2.7V
 - Device failures are indicative of useful test, but difficult interpretation
- Future efforts will continue to improve testing capability
 - Perform characterization testing on recently acquired DIMMs
 - Parametrics, data pattern impact on cell retention, etc.



END



Life Testing Concerns

- Interested in mechanisms that pass initial inspection
 - Manufacturer tests, burn in testing, additional upsampling
- TDDDB - time dependent dielectric breakdown
 - parameters: T, E field
- HCI – hot carrier injection
 - parameters: Current, # of bias switches
- Electromigration –
 - parameters: Current, Temperature, Activation Energy
- NBTI – negative bias temperature instability
 - parameters: E field, # of switches
- Key is to try to focus on early signs to identify outliers
- While also determining if a device family is acceptable



Test Matrix and Approach

- General Reliability Test Matrix is intractable
 - Large number of parameters
 - Large number of internal structures
 - Limited knowledge of internal voltage
 - Limited ability to apply accelerated wear out conditions
- General approach to provide highest benefit
 - Initial characterization used to identify population deviants
 - Perform characterization appropriate to missions
 - Perform characterization on every device using time-intensive algorithms such as
 - Cell retention at 25°C and 85°C/max T
 - Pattern dependency convolved with device refresh
 - Additional parametrics (timing, max frequency, etc)



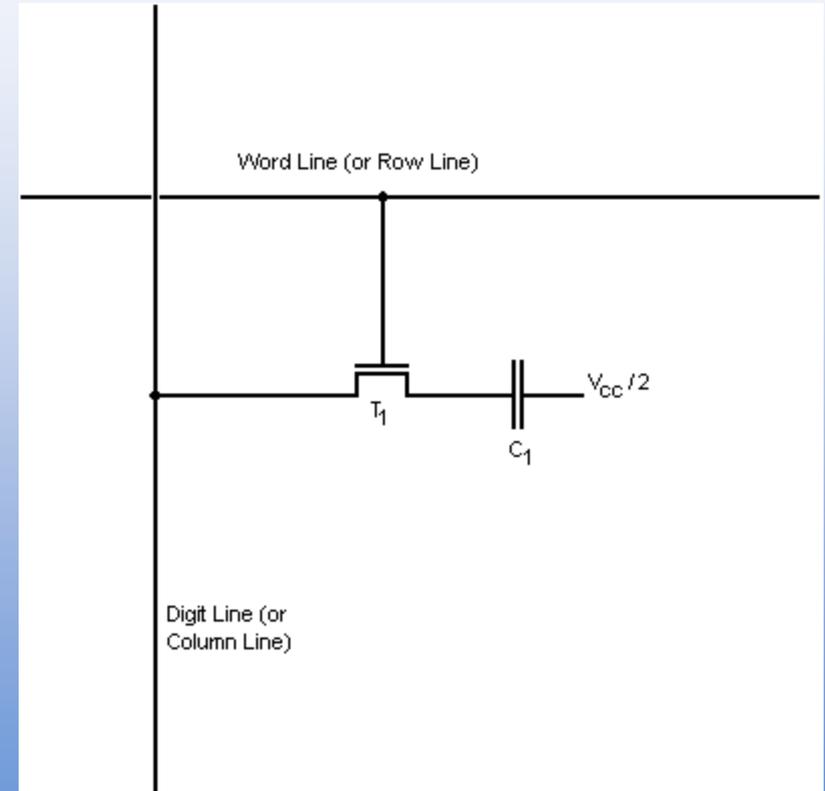
Test Hardware

- Supporting the following goals
 - General reliability testing
 - General project support
 - Flexible test capability to support off-spec-sheet testing
 - Interoperability to support NEPP-wide compatibility (including DIMM testing)
- Testing needs:
 - Individual part testing in small quantities
 - Targeting many data-sheet parameteric values
 - Test capabilities for many parts under life stress
 - Provide adequate operating conditions to achieve worst-case stress levels
 - Requires a couple complementary test setups
- Hardware directions:
 - Inexpensive expandable system for long life tests
 - Flexible and fast systems for full testing of key parameterics
 - Expanded compatibility of test hardware



Example: DRAM Cell Biasing

- The worst case bias across the gate to storage cell requires frequent refresh and/or inverting data
- Once charged to V_{CC} or 0, C_1 begins to discharge through T_1
- Refresh restores(inverts) the bias on C_1
- Frequent refreshing provides the worst case for high-bias failure mechanisms
- Some mechanisms (like HCI) will be worse if the bias switches.





Leading Failures

- Due to primarily targeting packaged devices, failure modes will be limited
 - Data errors
 - Decay in data storage capability (retention time or lost bits)
 - Modified operating bias
 - Changes in parameter ranges for operation
- Degraded performance may be difficult to link to a device structure
- Random Errors (degradation leading to reduced margin)
- Degraded Nodes (degradation leading to function loss)
- Reduced parameter-area of reliable operation
- Increased/altered device current draw



Qualification Challenges

- Establishing application usage requirements in concert with known device-type risks
- Using devices outside of the datasheet
 - Need to develop recommendations for both standard testing and derating needs
 - Failure mechanisms can be observed before they make a device fail a datasheet parameter
- Complex devices have many failure sources and modes - large test matrixes
- DDR devices are constantly changing



Qualification Approach I of II

- Device Selection
 - Generally plan on packaged devices unless a program is looking for a specific die/device
 - Target devices should include those of program interest as well as new RHBD/space grade devices such as Aeroflex, Boeing, SpaceMicro or others
 - Form factor may support loose devices and/or DIMMs



Qualification Approach II of II

- Establish test plan and take data
 - Depending on application and engineering goals, may need to develop parametric test capabilities specific for device
 - Set of environmental, bias conditions, and target test duration shall be set.
 - Utilize test setup to identify
 - First failures, leading parameter degradation, operational issues
- Reporting/Recommendations
 - Issue derating and usage guidelines
 - Prepare information for support of future program need and potential failure analysis



Testing Approach

- Testing many devices
 - Even after paring down, test matrix will be large
 - Will want 3 to 5 devices under each operating condition
- Testing different types of parameters
 - Data sheet timing parameters, bias levels, current draw under key operations
 - Non-data sheet parameters such as potential derating frequencies and refresh rates
- Life testing devices vs. Characterizing parameterics
 - Need constant functional operation during life testing
 - Will likely need to support 10+ simultaneous life test setups
 - Characterization will require more detailed operation than required during life-testing.



References

- Micron 2Gb DDR2 data sheet
- Mosis tech_cmos_rel FAQ “Reliability in CMOS IC Design: Physical Failure Mechanisms and their Modeling”
- Wikipedia DDR4 entry
- Jin Et. Al. “Prediction of Data Retention Time Distribution of DRAM by Physics-Based Statistical Simulation” – shows potential mechanism for our response is traps under the gate.



Additional Resources

- <http://www.sciencedirect.com/science/article/pii/S0026271402000306>
- <http://trs-new.jpl.nasa.gov/dspace/handle/2014/20169>
- <http://ieeexplore.ieee.org/Xplore/login.jsp?url=http%3A%2F%2Fieeexplore.ieee.org%2Fiel5%2F8520%2F26927%2F01197774.pdf%3Farnumber%3D1197774&authDecision=-203>
- <http://www.quickstartmicro.com/Sample%20Slides%20Quick%20Start%20IC%20Reliability.pdf>

Device Operation during Life Testing



- Key parameters for a given circuit element:
 - Temperature, Voltage(Electric Field), Activation Energy, Current Density, Times Switched,
 - At any given node, $V=V(t)$
- Desired operations
 - Switching of all transistors
 - Switching/operating a key subset of transistors
 - Operating at degraded frequency (for derating)
 - Operating worst case voltage and temperature, possibly off the datasheet.
 - Keep all “static” items biased the same as in operation
 - For DRAM data, this is achieved by simply refreshing, but can also be achieved by writing and reading the array repeatedly
 - Similar to industry standard Dynamic Operation Stress (DOS)