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Analysis of SDRAM SEFIs

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Outline

- A SEFI in space – the call to action
- Quick SEFI review
- SEFI Testing – special needs for data collection
- SEFI Reporting – capturing structural info
- Application Impact
- Conclusion

Special Note: A SEFI (Single Event Functionality Interrupt) here refers to an event that disrupts data stored in the SDRAM. The disrupted data is lost, but device operation may or may not have been affected

Call to Action

- After launch, the Juno spacecraft experienced a “Multi Bit Error (MBE)” event
- Analysis suggested this event was due to a SEFI on a 512 Mb Elpida SDRAM (EDS5104ABTA)
- Examinations of test data and usage cases were performed for Juno and other JPL missions
  - JPL has several missions using this SDRAM
  - Usage implied need for some additional, application specific, test data and event impact

- Special SEFI test data in flight-like application were taken in order to establish SEFI risk for a few JPL programs
  - Use case and SEFI structure were the relevant parameters

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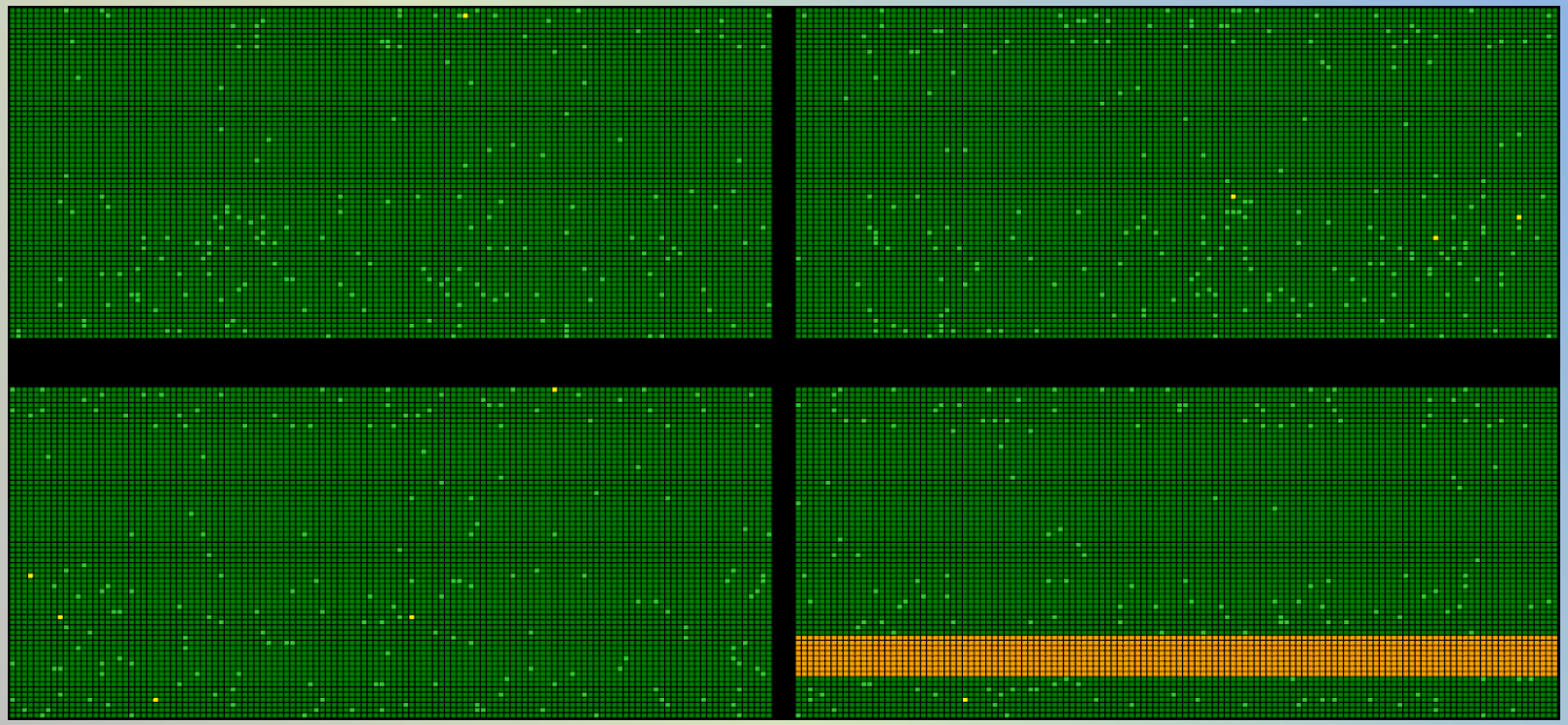
What is a SEFI

- Visual display can aid observation/description



Dark Green = no errors

Light Green = 1 SBU

Yellow = 2 SBU in row

Orange = 1 or more bytes with DBU

Red = 1 or more bytes with TBU

White = 3+ SBU in row

Testing for SEFI Structure

- Identify SEFIs:
  - Use a pattern where SEFIs cannot hide – recommend pseudo-random
  - Visual interface recommended, especially one that can easily identify, catalog, and then remove specific SEFIs
  - Use low enough fluence to clearly identify a few samples, or record passes with only a few new samples per pass
  - Test the entire device storage area
- Catalog SEFIs:
  - Record the operating mode of the DUT
  - Record the test pattern stored in the DUT
  - Understand distribution of bit errors/word expected
  - Identify address bits impacted by SEFI
- Determine Relative Importance
  - Reload data and all is well?
  - Requires power cycle?
  - Requires mode reload (reset)?
  - Other?

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Example:
Structure of a SEFI

- The manifestation of a SEFI is just a list of error addresses and bit patterns

- Address Analysis:
  - Example at right is from spacecraft event
  - Addresses were broken into bit values and each bit location binned by # of times it is 0 or 1
  - Gray bits are unchanging and specify the generic location of the SEFI
  - Yellow bits have approximately 50/50 0's and 1's

	Frequency		
Addr Bit#	1's	0's	ratio
31	0	2680	0.00
30	2680	0	1.00
29	0	2680	0.00
28	2680	0	1.00
27	2680	0	1.00
26	2680	0	1.00
25	0	2680	0.00
24	0	2680	0.00
23	1188	1492	0.44
22	1059	1621	0.40
21	1321	1359	0.49
20	1287	1393	0.48
19	1321	1359	0.49
18	1330	1350	0.50
17	1321	1359	0.49
16	1344	1336	0.50
15	1316	1364	0.49
14	1374	1306	0.51
13	0	2680	0.00
12	2680	0	1.00
11	1334	1346	0.50
10	1353	1327	0.50
9	1347	1333	0.50
8	0	2680	0.00
7	1295	1385	0.48
6	0	2680	0.00
5	2680	0	1.00
4	0	2680	0.00

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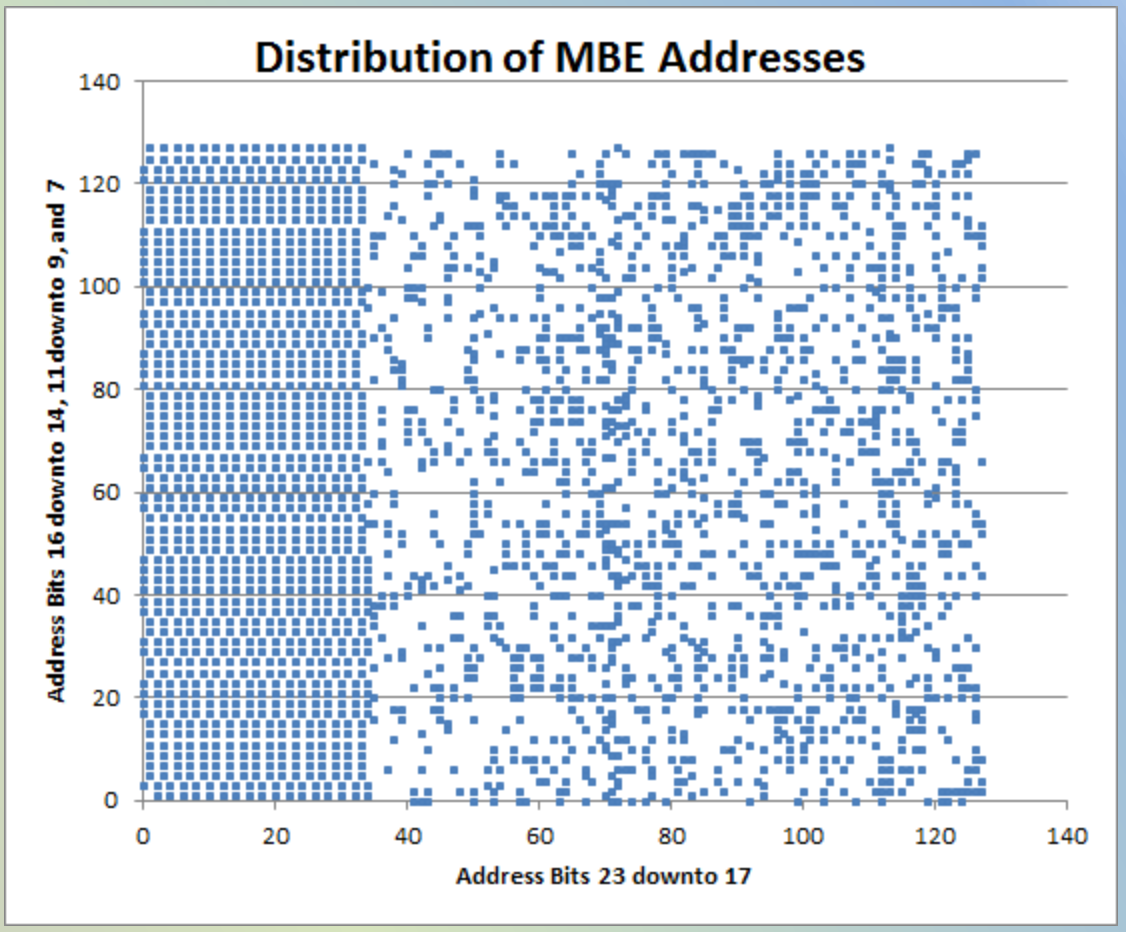
Example: Analysis Display of a SEFI

- Actual flight SEFI
- Only the SEFI rectangle is shown
- Left and right side show regions with two different underlying patterns
- Only addresses with 2-bit errors are shown



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Example:
Structure of a SEFI

- Error bits for most SEFIs on x4 Elpida 512 Mb
  - _,X,X,_
  - Or X,_,_,X ← Juno Event
- Error bits for most SEFIs on x8
  - _,_,X,X,X,X,_,_
  - Or X,X,_,_,_,_,X,X
- Error bits on x16 not analyzed

Test data from x4 device does not guarantee understanding of x8/x16, etc.

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JPL's New SEFI Test System

- Migrated a FPGA-based reliability test system to perform full device data transfer to a host PC using USB
- Operates DUT in application-like mode
- Sends all data to computer for storage and analysis
- Data taken at BNL with Elpida EDS5108ABTA

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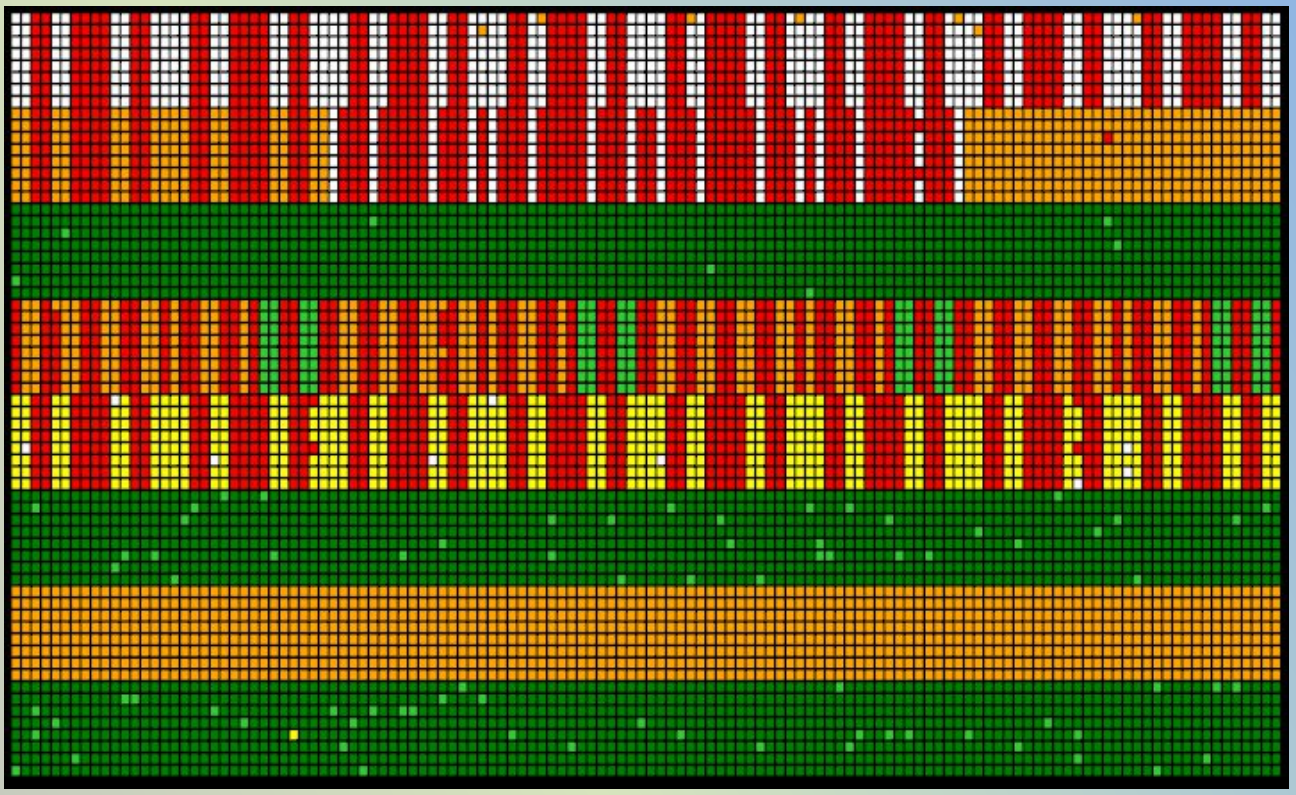
SEFI Testing

- JPL recently developed an in-house tester capable of visualization and computer-assisted-analysis of SEFIs

- Initial Visualization of Bank 3
- 5 Bands of errors



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SEFI Testing

- Tester can gather data an present visually
- But also provides interface to directly see error report

- List of errors quickly shows that only a few addresses in each row has errors (Band SEFI)

```
11744 R:00D4 C:724 B:3 Ex:01F950DF Rd:01F950FF Er:00000020
11745 R:00D5 C:724 B:3 Ex:FE06AF20 Rd:FE06AF00 Er:00000020
11746 R:00D6 C:724 B:3 Ex:01F940DF Rd:01F940C3 Er:0000001C
11747 R:00D7 C:724 B:3 Ex:FE06BF20 Rd:FE06BF3C Er:0000001C
11748 R:00D8 C:724 B:3 Ex:01F930DF Rd:01F930CB Er:00000014
11749 R:00D9 C:724 B:3 Ex:FE06CF20 Rd:FE06CF3C Er:0000001C
11750 R:00DA C:724 B:3 Ex:01F920DF Rd:01F920FF Er:00000020
11751 R:00DB C:724 B:3 Ex:FE06DF20 Rd:FE06DF00 Er:00000020
11752 R:00DC C:724 B:3 Ex:01F910DF Rd:01F910C3 Er:0000001C
11753 R:00DD C:724 B:3 Ex:FE06EF20 Rd:FE06EF3C Er:0000001C
11754 R:00DE C:724 B:3 Ex:01F900DF Rd:01F900FF Er:00000020
11755 R:00DF C:724 B:3 Ex:FE06FF20 Rd:FE06FF00 Er:00000020
11756 R:00E0 C:724 B:3 Ex:01F8F0DF Rd:01F8F0FF Er:00000020
11757 R:00E1 C:724 B:3 Ex:FE070F20 Rd:FE070F10 Er:00000030
11758 R:00E2 C:724 B:3 Ex:01F8E0DF Rd:01F8E0C3 Er:0000001C
11759 R:00E3 C:724 B:3 Ex:FE071F20 Rd:FE071F3C Er:0000001C
11760 R:00E4 C:724 B:3 Ex:01F8D0DF Rd:01F8D0FF Er:00000020
11761 R:00E5 C:724 B:3 Ex:FE072F20 Rd:FE072F00 Er:00000020
11762 R:00E6 C:724 B:3 Ex:01F8C0DF Rd:01F8C0C3 Er:0000001C
11763 R:00E7 C:724 B:3 Ex:FE073F20 Rd:FE073F3C Er:0000001C
11764 R:00E8 C:724 B:3 Ex:01F8B0DF Rd:01F8B0C3 Er:0000001C
11765 R:00E9 C:724 B:3 Ex:FE074F20 Rd:FE074F3C Er:0000001C
11766 R:00EA C:724 B:3 Ex:01F8A0DF Rd:01F8A0FF Er:00000020
11767 R:00EB C:724 B:3 Ex:FE075F20 Rd:FE075F00 Er:00000020
11768 R:00EC C:724 B:3 Ex:01F890DF Rd:01F890C3 Er:0000001C
11769 R:00ED C:724 B:3 Ex:FE076F20 Rd:FE076F3C Er:0000001C
```

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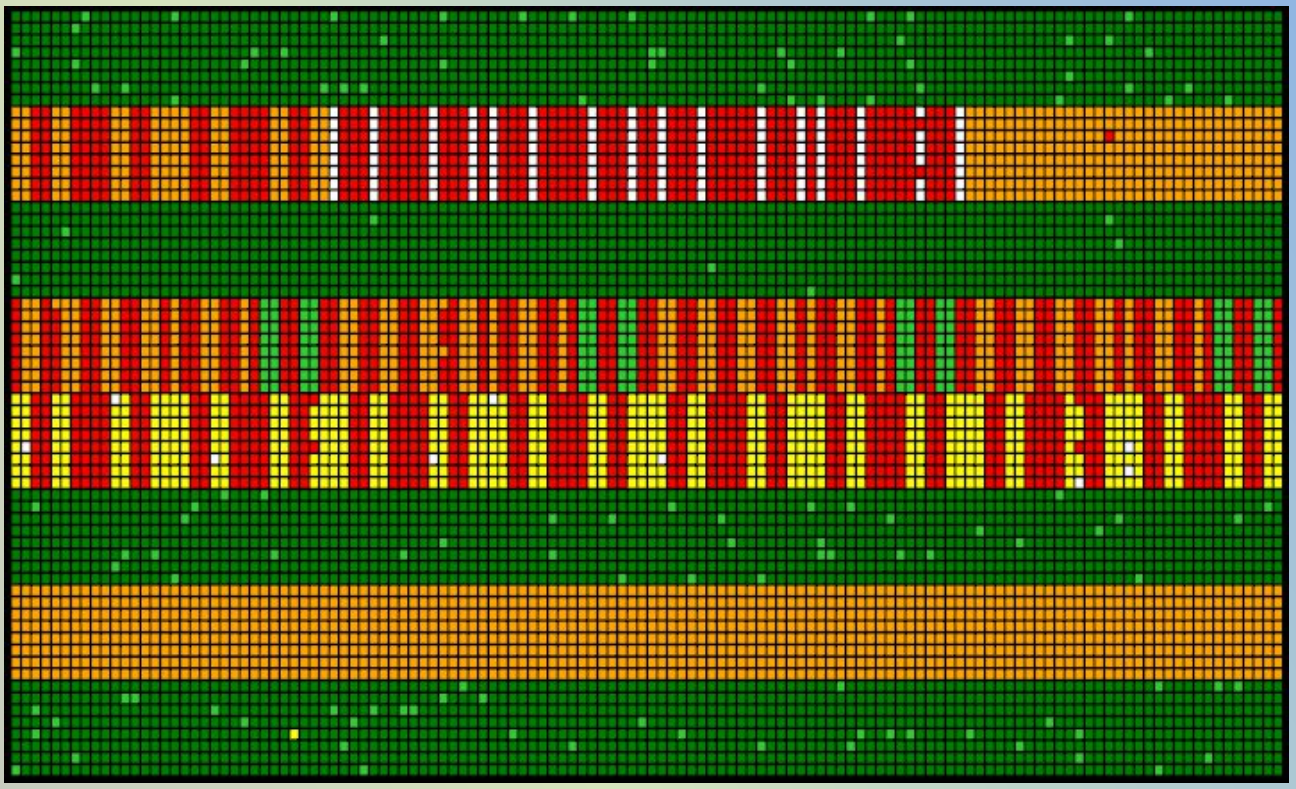
SEFI Testing

- Built-in analysis tools allow isolation and removal of explicit SEFI structures

- SEFIs can be removed from viewing while retaining all other errors in the array



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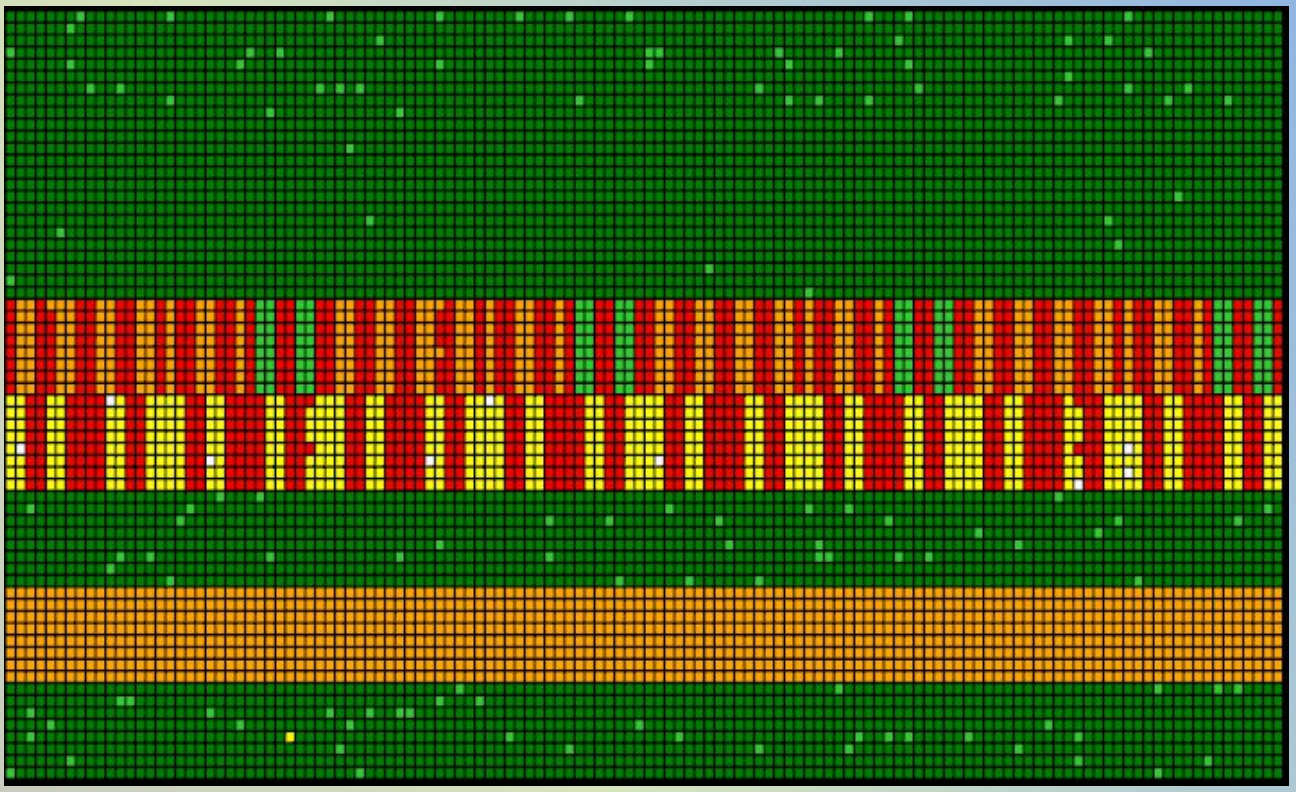
SEFI Testing

- Built-in analysis tools allow isolation and removal of explicit SEFI structures
- When extracting SEFIs, the exact structure can be collected



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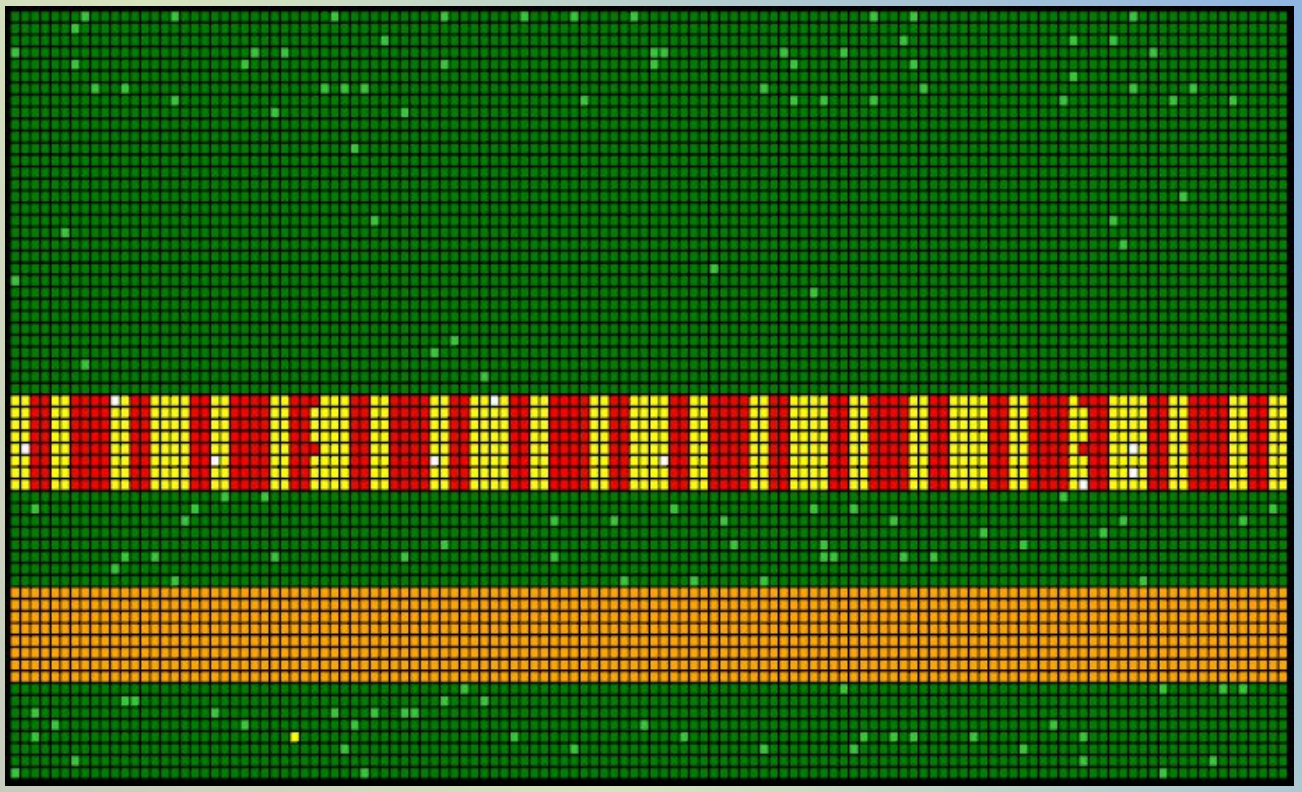
SEFI Testing

- Built-in analysis tools allow isolation and removal of explicit SEFI structures

- Multiple SEFIs in the same visible region can be easily distinguished in error listing



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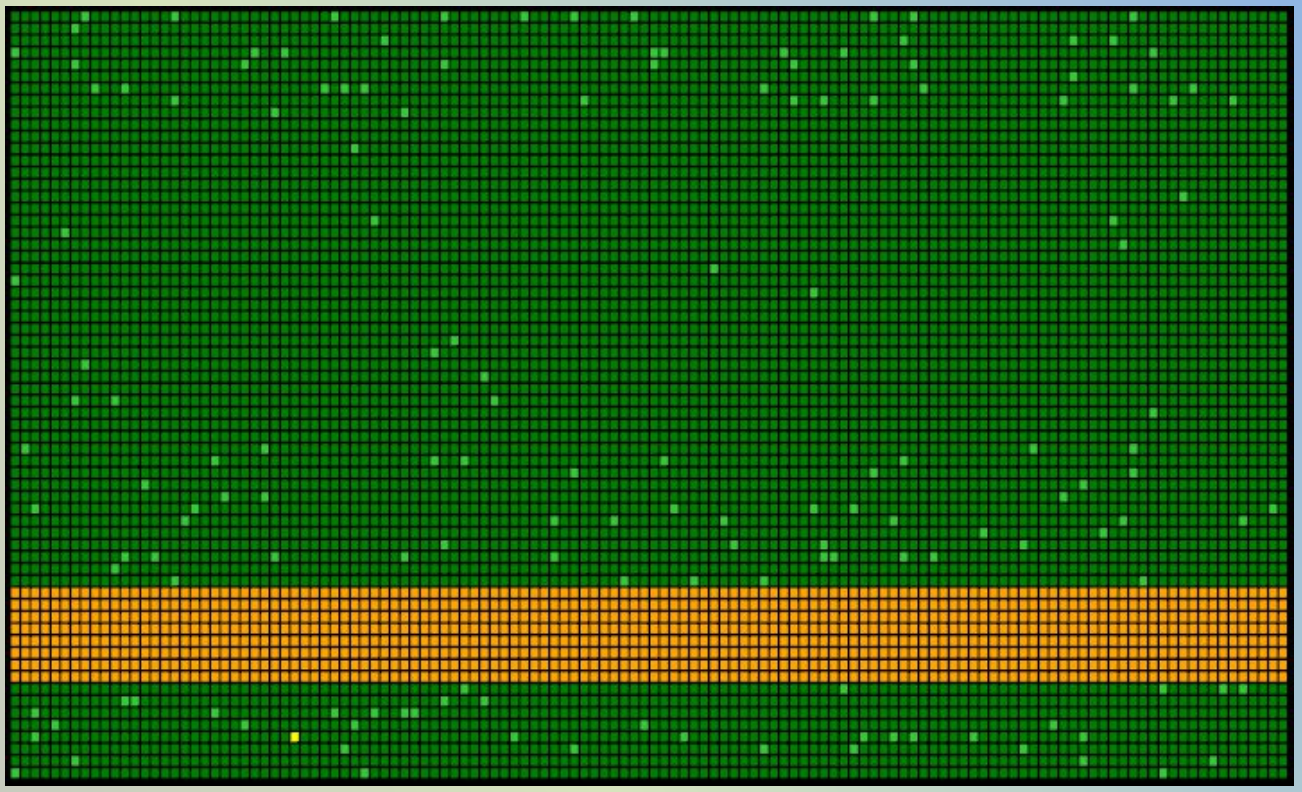
SEFI Testing

- Built-in analysis tools allow isolation and removal of explicit SEFI structures



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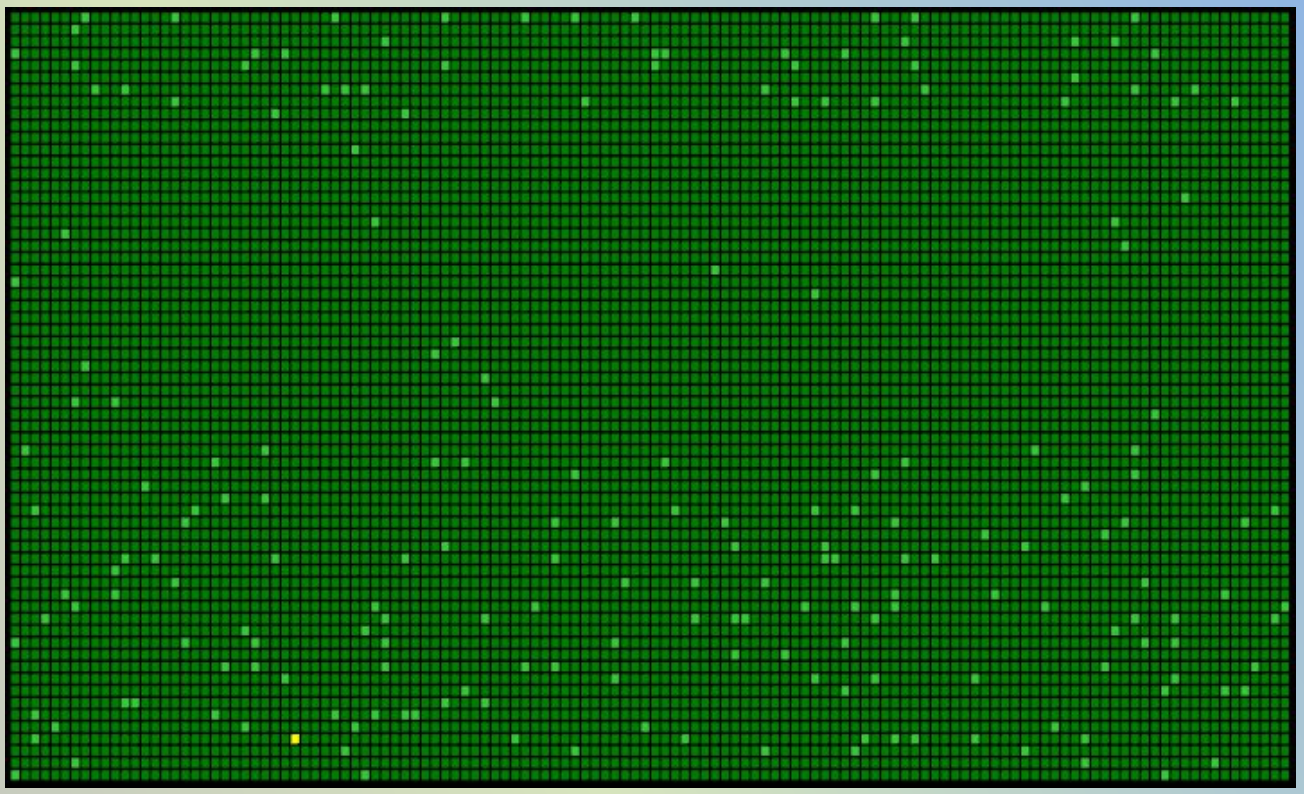
SEFI Testing

- Built-in analysis tools allow isolation and removal of explicit SEFI structures

- When all SEFIs removed, the remaining bit upsets can be easily scanned for MBUs and clusters



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SEFI Report

- Based on the computer-aided SEFI exclusion, a report on SEFIs in the device is generated:

```
Band R0000-03FF/B3/C124M1F7 Excluded:8192 bad quad bytes: ZBUs:12291
SBUs:3066 DBUs:15 TBUs:1016 QBUs:0 >4BUs:0 bits in error: 0000003E
Band R1000-13FF/B0/C14CM1FF Excluded:4096 bad quad bytes: ZBUs:9216 SBUs:0
DBUs:3072 TBUs:0 QBUs:0 >4BUs:0 bits in error: 3C000000
Band R0400-07FF/B3/C07CM1FF Excluded:4096 bad quad bytes: ZBUs:8448
SBUs:766 DBUs:1023 TBUs:771 QBUs:256 >4BUs:0 bits in error: 00C30000
Band R0400-07FF/B1/C038M1FF Excluded:4096 bad quad bytes: ZBUs:9216
SBUs:1536 DBUs:0 TBUs:1536 QBUs:0 >4BUs:0 bits in error: 3C000000
Band R1000-13FF/B3/C018M1FF Excluded:4096 bad quad bytes: ZBUs:6144
SBUs:1016 DBUs:0 TBUs:1032 QBUs:0 >4BUs:0 bits in error: C3000000
Band R0C00-0FFF/B3/C12CM1FF Excluded:4096 bad quad bytes: ZBUs:5760
SBUs:514 DBUs:769 TBUs:509 QBUs:128 >4BUs:0 bits in error: 0000C300
Band R1C00-1FFF/B1/C044M1FF Excluded:4096 bad quad bytes: ZBUs:6144
SBUs:1024 DBUs:0 TBUs:1024 QBUs:0 >4BUs:0 bits in error: 000000C3
Band R1800-1BFF/B3/C00CM1FF Excluded:4096 bad quad bytes: ZBUs:6144 SBUs:0
DBUs:2048 TBUs:0 QBUs:0 >4BUs:0 bits in error: 3C000000
```

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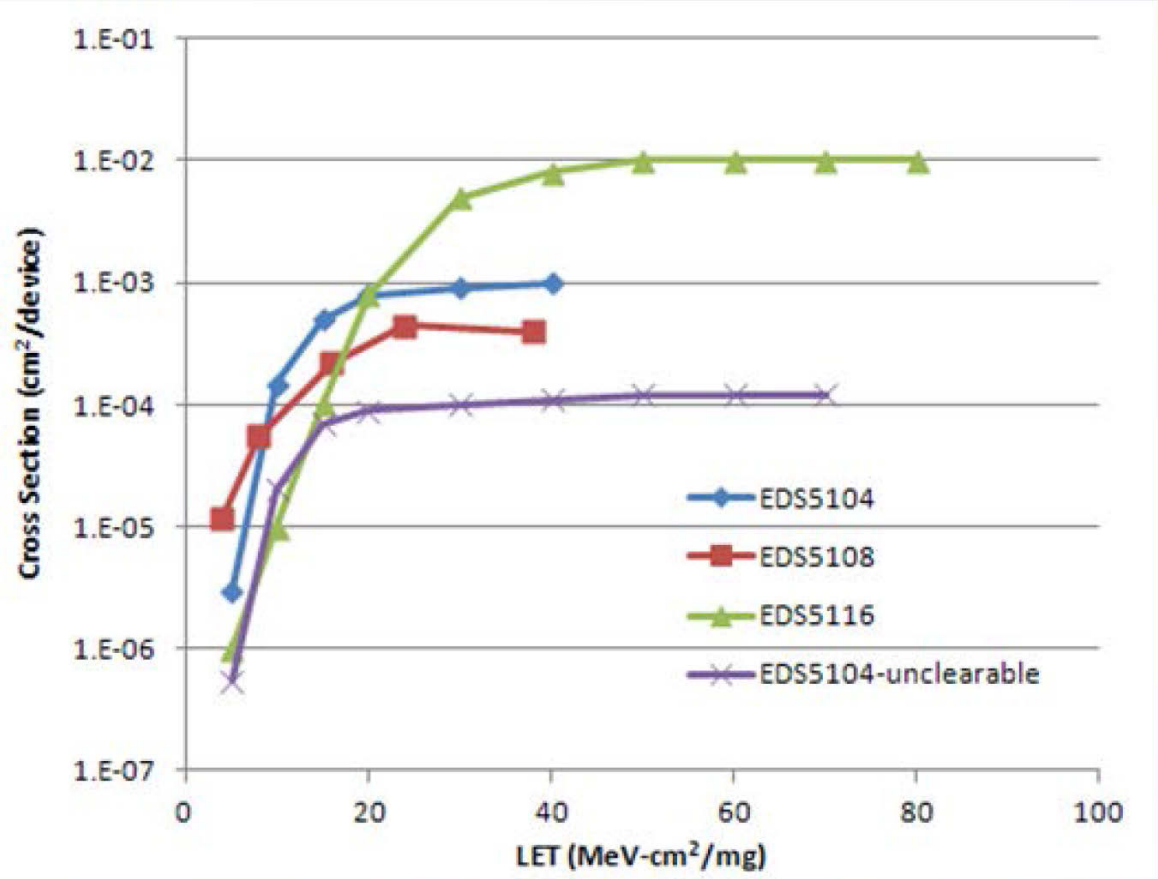
SEFI Test Results for EDS5108ABTA

- 3 Observed SEFI Types: Band SEFI, Row SEFI, “mini SEFI”
- Some SEFIs can be recovered by performing some DUT operation
- Test Results:



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Assessing SEFI Impact

- Use cases and SEFI structure must be taken together
  - Systems may be immune to some types of SEFIs:
    - If a system can fix DBEs on EDS5104, most SEFIs have no impact
  - Many applications only require temporary storage:
    - As long as device can store new data, an old SEFI is irrelevant
  - Many SEFIs are recoverable:
    - Mode register reload (reset) can recover data, provided the system can utilize this appropriately
    - Reloading data or reinitializing memory ← Juno case
    - Systems will still have some exposure to these SEFIs
  - Interplay of SEFI address extent and system use:
    - Key system data may have reduced SEFI risk
  - Applications as computer main memory are most critical:
    - Unless protected against full SEFI extent, a SEFI can cause a crash of a kernel task, taking down the computer.

Conclusion

- Usage recommendations
  - Use all SEFI mitigation available and reasonable for the application
    - Mode register reload; 2, 4, or more bit ECC; rewrite data; etc.
- Testing for SEFI structure can be difficult, but there are many aids to help improve test methods and results
  - Full device size must be tested with “good” pattern
  - Visual display and SEFI-specific analysis tools are very helpful
- SEFI structure is very important in establishing mission impact
  - Designers could design around them
  - SEFI impact on critical operations can be calculated separately
  - If structure is known, then it is much easier to identify SEFIs in space and help programs establish how to handle them
- SDRAM use case is also very important
  - Some types of applications are inherently resilient to SEFIs while others (e.g. computer main memory) are likely to have significant problems.

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Test Pattern & Errors

- SEFI Scenarios:
  - SEFI "resets" data
    - SEFI will set data to a pathological case – all 0's, all 1's, or some checkerboard structure
  - SEFI "swaps" data
    - SEFI exchanges data from two good regions with data
  - SEFI "maps in/out redundancy" data
    - SEFI exchanges data from a good region with a redundant region (spare bits for increasing yield)
- Pattern Impact
  - Under all three scenarios, simple/pathological test patterns have limited coverage
  - Address-based patterns will have pathological structure in a lot of cases and are weak, but better than simple patterns
  - Pseudo-random patterns are the best but lead to data analysis difficulty

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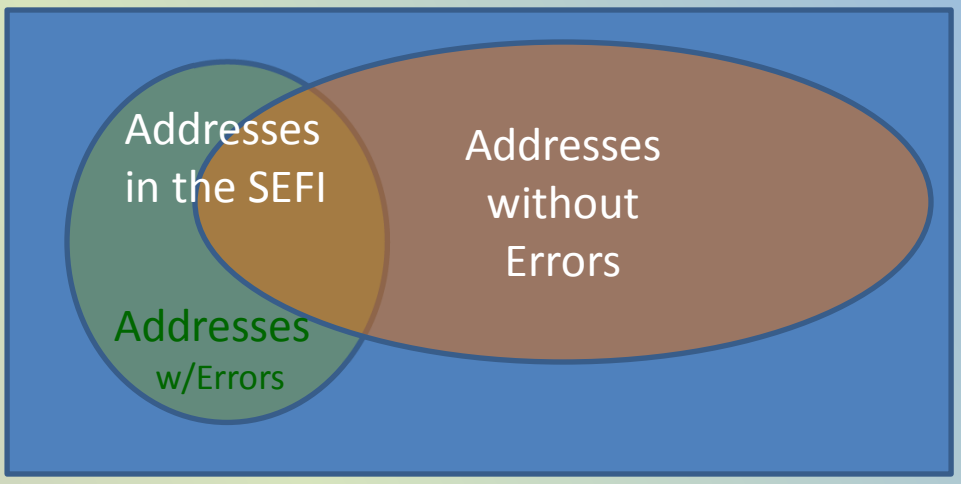
What Address Approach Means

- The most abstract description is a Venn-Diagram



- Goal is to obtain accurate SEFI info from errors
- Error address information can enable us to paint a more specific picture

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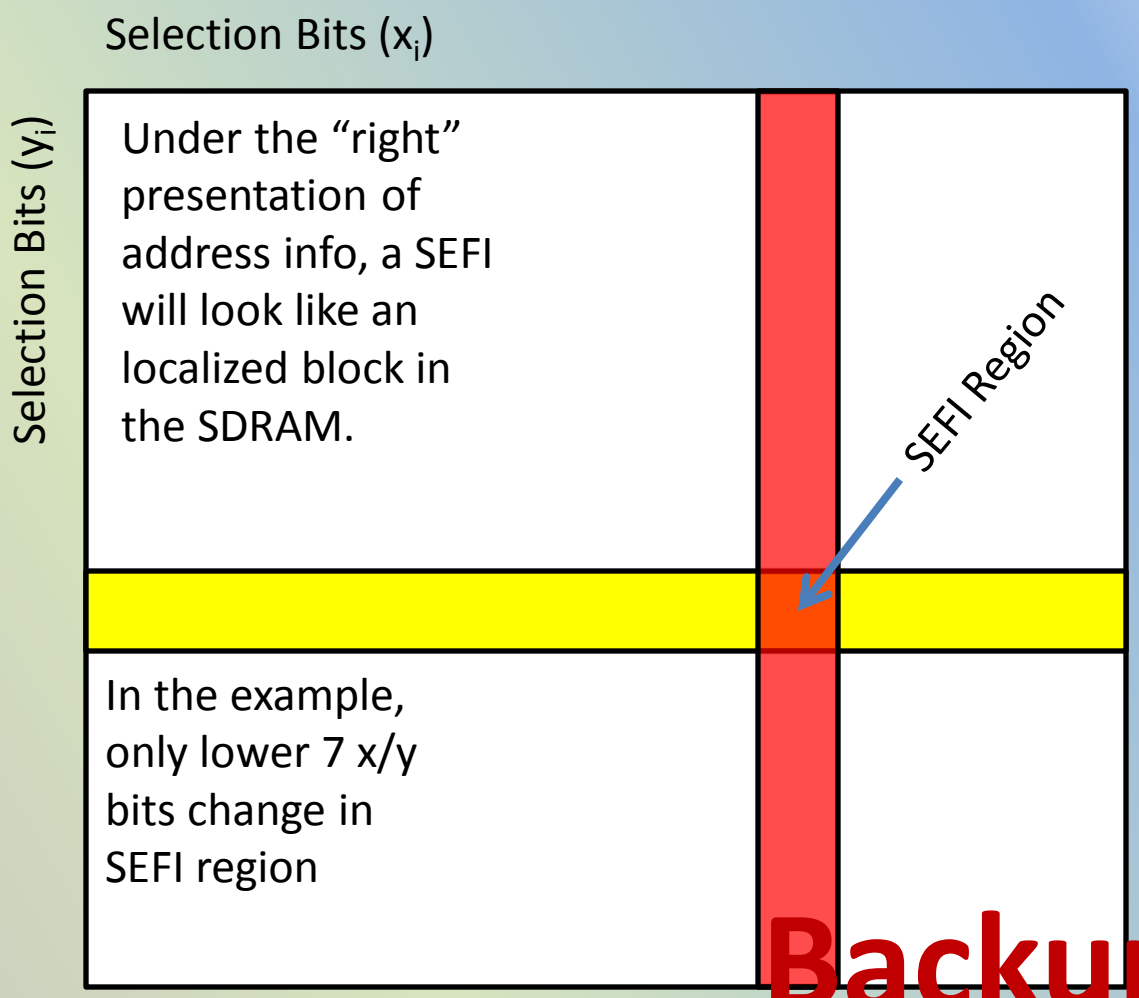
SEFI Address Abstraction

- Address details in SEFI can correspond to decoding and local corruption…
- First we take the "SEFI" address bits and arrange them into two groups $\{x_i\}$ and $\{y_i\}$
- Then we arbitrarily grab the remaining bits and concatenate them to make two vectors $X = (x_1, x_2, \ldots x_n)$ and $Y = (y_1, y_2, \ldots y_n)$
- If we then draw a 2-d plot of the errors, the full device will be a rectangle, and the SEFI region is a sub-rectangle



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Testing for SEFIs

- Full characterization is not possible - (~years)
- The present case, however, suggests full characterization is not necessary
  - Many different test groups have assessed block errors or SEFIs on these parts and results are all similar for the most common modes (Benedetto, Adell/McPeak, Lawrence)
  - Application specific verification may be necessary
    - At speed
    - Application algorithm

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Defining a SEFI

- Address Extent:
  - Which bits can change and/or which must stay the same (remain fixed)
  - What the value of the fixed bits must be
    - In the example, row bits 12, 11, 10 must be 1,0,0
    - Bank bits 1,0 must be 0, 1 (i.e. BA1 = 0, BA0 = 1)
    - Column bit 8 must be 0
    - Column bits 6, 5, …, 0 must be 0,1,0,0,1,0,0
- Data pattern:
  - Which bits can be wrong
    - In the case of the Elpida x4, we know the data pattern is _,X,X,_ or X,_,_,X – where 'X' represents a bit that can be wrong
    - In the Elpida x8, the observed patterns are _,_,X,X,X,X,_,_, and X,X,_,_,_,_,X,X
  - In other parts, the patterns may be more complex and analysis will have to watch for this
- Error mix:
  - The distribution of observed bit errors in words

	Frequency		
Addr Bit#	1's	0's	ratio
31	0	2680	0.00
30	2680	0	1.00
29	0	2680	0.00
28	2680	0	1.00
27	2680	0	1.00
26	2680	0	1.00
25	0	2680	0.00
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7	1295	1385	0.48
6	0	2680	0.00
5	2680	0	1.00
4	0	2680	0.00
3	0	2680	0.00
2	2680	0	1.00
1	0	2680	0.00
0	0	2680	0.00

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Examples of SEFI Structure in EDS5108ABTA

- 3 Observed SEFI Types:
  - Band SEFI
  - Row SEFI
    - Note that on the EDS51xx devices some Row SEFIs respond differently than others to device reset
  - "mini SEFI"
- A few ground-based SEFIs:

Address Extent

Error Mix

Data Pattern

	Row Rng		Column	Col Mask	Bytes in					
	Row	Bank	Row Mask		SEFI	SBEs	DBEs	TBEs	QBEs	Err. Patt
Band SEFIs	1C00-1FFF	0	178	1FF	4096	1426	879	1444	174	000000C3
	1C00-1FFF	2	168	1FF	4096	727	2510	737	50	0000003C
	0000-03FF	0	158	1FF	4096	2440	2921	2499	173	004300C3
	1800-1BFF	2	050	0FF	8192	5111	1475	1064	274	0000C300
	1C00-1FFF	3	0B8	1FF	4096	1047	1131	1030	477	C3C1FFC3
	1000-13FF	2	084	1FF	4096	2582	3141	1526	226	C200C300
	0C00-0FFF	2	000	1FF	4096	1041	1597	1019	243	3C34EB3C
	1C00-1FFF	2	048	1FF	4096	4096	0	0	0	00000020
	0C00-0FFF	0	04C	1FF	4096	1015	1510	1050	261	003C0000
	0C00-0FFF	1	044	1FF	4096	1170	1296	1236	204	3C[illegible]000
Row SEFIs	1C00	3	1DFF		4096	1017	1694	1004	182	C3[illegible]FC3
	1000	3	1DFF		4096	1467	808	1474	174	C3C3C3C3
	0DFF	2	1DFF		4096	1179	758	1207	480	3C3CFF3C

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Program Use Cases

- Data Storage
  - Data is written to the SDRAM and will be needed later, storage time may be long (>days)
  - Primary impact of SEFI: lost data
- Buffering
  - Data is written to the SDRAM with intent to be transferred to another subsystem rapidly (<minutes)
  - Primary impact of SEFI: minor due to reduced likelihood SEFI impacts relevant data (unless SEFI is more disruptive)
- Computer Memory
  - SDRAM provides main memory function to a computer
  - Primary impact of SEFI: double bit error interrupt, loss of thread, and depending on software a possible reboot

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Example:
Cross Mapped SEFI

- Many observed SEFIs (especially on flight lot parts) show very regular error patterns…

- This sort of regularity suggests that although data is not correct, it is regular.
- The most likely way to pick up regular but incorrect data is if the incorrect data was initialized
- Further examination of patterns like that above suggest error pattern does not follow test data pattern…

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SEFI "Recovery"

- The symptoms of certain SEFIs can be recovered
  - Most commonly this occurs throug01010h reloading the mode register (device reset)
- Requires the data still exist somewhere on the chip… but where?
  - Redundancy
  - Cross Mapping? (Discussed in Bougerol 2010)
- Program impact
  - None?
    - If the memory is unused during the SEFI and recovery
  - Temporary
    - If the SEFI causes momentary loss of data
    - If the SEFI can be identified and the system allowed to re-try operation
  - Problematic
    - If the symptoms of the SEFI cause immediate problems (processor crash)

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