Array Technology for Terahertz Imaging

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ABSTRACT

Heterodyne terahertz (0.3 – 3THz) imaging systems are currently limited to single or a low number of pixels. Drastic improvements in imaging sensitivity and speed can be achieved by replacing single pixel systems with an array of detectors. This paper presents an array topology that is being developed at the Jet Propulsion Laboratory based on the micromachining of silicon. This technique fabricates the array’s package and waveguide components by plasma etching of silicon, resulting in devices with precision surpassing that of current metal machining techniques. Using silicon increases the versatility of the packaging, enabling a variety of orientations of circuitry within the device which increases circuit density and design options. The design of a two-pixel transceiver utilizing a stacked architecture is presented that achieves a pixel spacing of 10mm. By only allowing coupling from the top and bottom of the package the design can readily be arrayed in two dimensions with a spacing of 10mm x 18mm.

Keywords: Terahertz, Imaging, Array, Silicon, Micromachining

1. INTRODUCTION

Person-borne concealed weapon or contraband detection at long distance is an urgent national security need, but presently there is no adequate solution available. Terahertz radiation is of great interest for this application because of its ability to penetrate clothing and provide resolution on the order of millimeters. Although this does not have the resolution of X-rays, the energy is low enough to not be ionizing, avoiding any health concerns. Two primary approaches are used from imaging at these frequencies, active and passive. Passive imagers capture differences in black body temperatures between a person and any concealed items [1]. These systems are limited in sensitivity due to the minor temperature and emissivity differences that define the image and improvements in image quality are primarily made by cryogenically cooling the system [2]. In contrast, active imagers paint the target with a low-power terahertz signal and form the image from the energy reflected from the target.

The active radar developed at the NASA Jet Propulsion Laboratory operates in a frequency-modulated continuous-wave mode (FMCW). By acquiring high resolution time-of-flight measurements between the system and target a virtual “pat-down” at a standoff distance of 25m is obtained [3]. Previous generations of the JPL radar have operated around 670GHz, but this paper discusses a new frontend transceiver design operating at 340 GHz. Although this lower frequency has a lower resolution, greater clothing penetration and higher transmitter power are achieved with a simpler transceiver design [4].

For most security screening applications, near video rates (> 4 Hz) are required to allow for adequate security checkpoint throughput. To scan, the active radar mechanically steers a single beam across the target area in a serpentine pattern. Currently this mechanical scanning limits the frame rate of the system to approximately 1 fps for a 0.4m x 0.4m target area. This is set by the mechanical behavior of the scanning mirror, which begins to deteriorate the angular accuracy of the optical system when the mirror is scanned faster. To overcome this limitation, an array of transceivers can be used to reduce the required angular rotation in one of the scanning dimensions. If an N-transceiver array, the frame rate can be increased by a factor of N since the angle required to scan the mirror is reduced.
Fabrication of an array of transceivers with sufficient pixel density to efficiently couple to a compact optical system is not a trivial task at submillimeter wavelengths. For example, Figure 1(a) shows a diagram of the single beam transceiver frontend. The transceiver is fed an LO with a frequency of 108-118 GHz which is amplified to 100mW. This amplified signal drives triplers that produce approximately 10mW of output power. The output of one of these triplers is the transmitted signal and the other provides the LO for the receive mixer. Previously, each of these components has been packaged individually into metal machined blocks, as shown in Figure 1(b). This results in a large system, with pixel spacing being limited by the diameter of the flanges that couple the devices (approximately 2 cm). Clearly, an array of transceivers based on modular components would not be practical.

The transceiver components need to be integrated into a single package to create an array of sufficient pixel density. Metal machining could be used, but suffers for several drawbacks. First, CNC milling which are used to form the passive structures is an expensive, serial procedure. 2-D arrays are difficult to design, since signals must be routed through the split in the middle of the metal package. Finally, with all the components cascaded in a single package,
testing of each stage individually becomes impossible.

2. STACKED SILICON ARCHITECTURE

Silicon micromachining is being applied to produce packaging for the transceiver array that avoids many of these problems. This technique applies a microelectronics-based fabrication technique to etch the waveguide components from silicon wafers. Since this is a batch process, multiple devices can be produced with the same effort, reducing costs and production time. All the features are photolithographically defined resulting in higher precision and uniformity compared with CNC milling[5]. Finally, with the packaging material being a semiconductor, bias circuitry and IF routing can be integrated into the packaging, increasing the circuit density and simplifying assembly.

Towards developing an architecture that can support 2-D arrays, 3-D integration is applied to minimize the area, not just the length, of each pixel. Figure 2 shows the wafer stack-up of the two-pixel transceiver. Many benefits are gained by stacking layers of silicon. By separating each functional component the fabrication of each layer is simplified. This stackable architecture allows for testing of each stage, significantly reducing troubleshooting times. Most importantly, integration of the bias and IF lines through the wafer stack eliminates routing these signals out the sides of the assembly. This enables the design to be arrayed in two axes if higher pixel counts are required.

Figure 3 shows the entire two pixel array with all the supporting fixtures which couple to and from the silicon stack. The transceiver is fed two LO signals through LO power division fixture, which incorporates Y-junctions for both transmit and receive channels so that only two waveguide flanges are required to couple to the 2-pixel array. This fixture is relatively large due to these two WR-8 UG-386 flanges, but would only need to be as large as the silicon array for higher pixel counts.

Surface mount GPPO connectors are used for routing of the bias and IF signals. This type of push on connector is chosen because of its small size (3.5mm diameter). Its tolerance to axial misalignments enables direct connection to a PCB board, simplifying the routing of the signals to the array.

As mentioned earlier, the bias circuitry can be fabricated as part of the packaging to decrease the pixel spacing of the array. Figure 4 (a) shows the layer that houses the MMIC power amplifier and the bias circuitry with surface mount components. Vias between the front and back of each layer provide routing of drain and gate voltages for four amplifiers.

Figure 4(b) shows the receiver layer which houses the mixer and duplexer. Since the transmit and receive signals must be duplexed by a 3-dB hybrid, the fourth port of the hybrid is coupled out of the stack into an orthogonal polarization instead of a matched load. This allows for recovering half the transmit power using time-delay multiplexing and doubles the effective pixel count of the system [6].
Figure 4 (b) shows the IF output of the mixer being coupled to a vertical transition. This routes the IF output of the mixer to the bottom of the silicon stack. Figure 5 shows the design and simulation results of this vertical transition through eight 800um thick silicon wafers. The design couples from a CPW transmission line to the quasi-coaxial mode formed by the gold plated thru-wafer vias. By etching away the majority of the silicon between the center and edge vias, a compact 50 Ohm coaxial line can be formed vertically through the wafer stack. This vertical transition directly couples to the GPPO connector at the bottom of the assembly. Using a high resistivity substrate (2 kOhm-cm) the predicted loss is 17 dB/ft, which is comparable with coaxial cables of a similar diameter.

3. CONCLUSION

A high circuit density package for submillimeter-wave arrays is being developed by combining a 3-D stacked architecture with silicon micromachining. This architecture is applied to the frontend transceiver components of the JPL active imaging radar. A two-pixel transceiver design is present that achieves a pixels spacing of 10mm. The vertical

Figure 5: The IF vertical transition simulation model and results. Insertion loss is less than 0.4dB through a silicon stack of eight 800um thick wafers with a resistivity of 2 kOhm-cm.
routing through the silicon stack allows this design to be arrayed in two dimensions with a pixel spacing of 10mm x 18mm.

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5. REFERENCES


