SiGe based Low Temperature Electronics for Lunar Surface Applications

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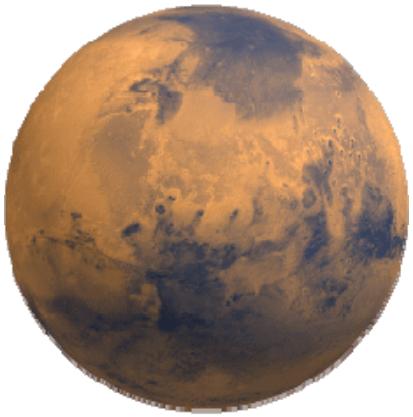
Agenda

- Background
- Cryogenic Operation of SiGe HBT
- Cryogenic Operation of CMOS
- Distributed Motor Controller (DMC)
  - DMC ASIC designs
  - Breadboard implementation
- Testing and Characterization
- Future Direction

BACKGROUND

Motor Control Architectures

Extreme Environment Missions

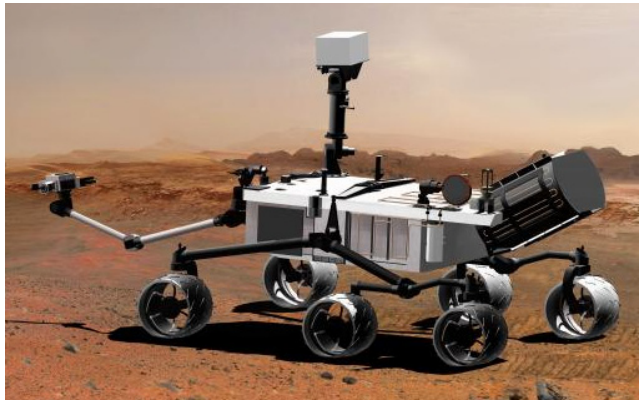


Mars
Temperature Range
[-125°C , 20°C]

Vulnerable to radiation

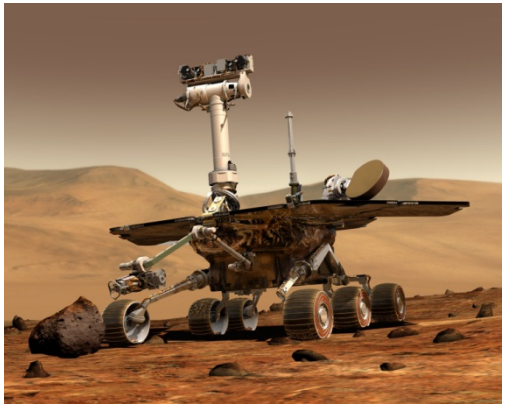
- Thin atmosphere
- Lack of magnetic field

Mars Science Laboratory [2011]



40 actuators

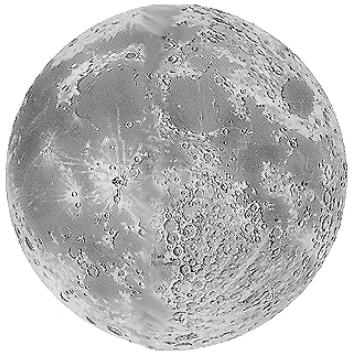
Mars Exploration Rover [2003]



20-25 actuators

- Centralized WEB based architecture
- Wet lubricated and heated actuators

Moon
Temperature Range
[-185°C , 120°C]



ATHLETE Lunar Rover [2010+]

60+ actuators

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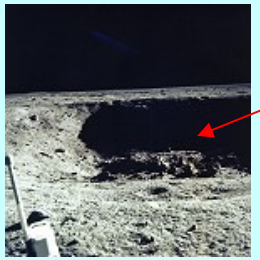
State of Practice: Lunar Systems

Hardware tested at Moses Lake

Lunar Surface Temperature:
120C Days, -180C Nights



Excursions into permanently shadowed craters (as low as -233 °C)

Shading by local topography

Hardware located on appendages

Self shadowing of hardware

Operations during night cycle

Payload Handling: Lunar Crane

Rover: Lunar CHARIOT

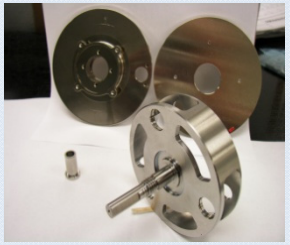
Cargo Carriers: ATHLETE

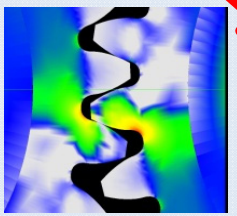
- Electronics in “Warm Electronic Box” (WEB)
- Wet lubricated and heated actuators

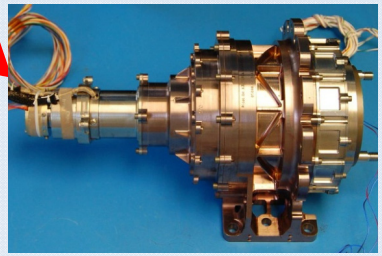
Low Temperature Mechanism

LTM revolutionizing the design of next generation space systems with low temperature motors, drive electronics, gearboxes, actuators, seals and dry lubricants all integrated together for the extreme environment of space

"State of Practice": MSL actuators motor / gearbox combination that is wet lubricated, heated and controlled from warm electronic box

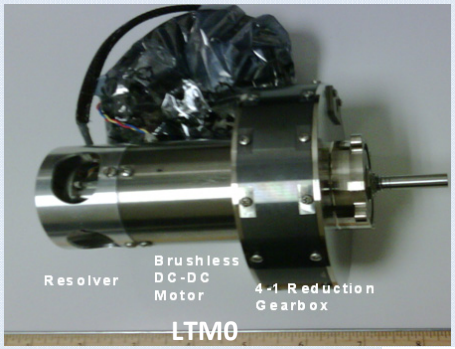






Gear Box Components & Housing

Bearings

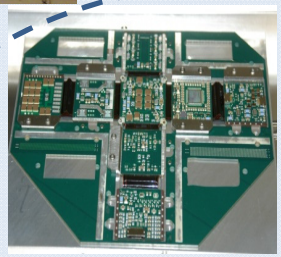


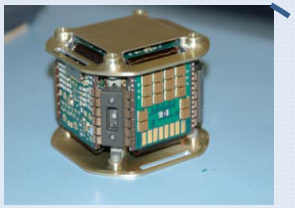
LTM0

LTM1

Resolver

Dust seal

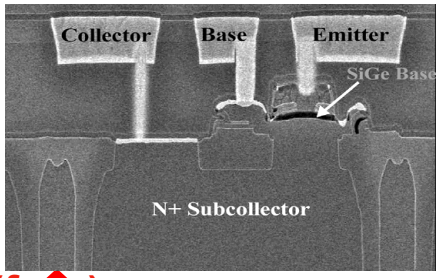




Control Electronics

Cryogenic Operation of SiGe HBTs

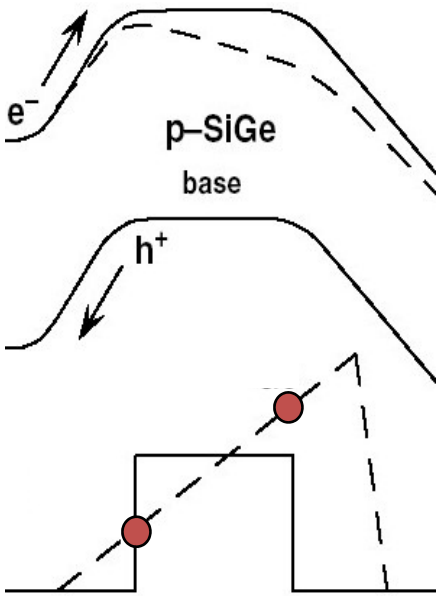
SiGe HBTs for Cryo-T



The Idea: **Put Graded Ge Layer into the Base of a Si BJT**

Primary Consequences:

- **smaller base bandgap increases electron injection** ($\beta\uparrow$)
- **field from graded base bandgap decreases base transit time** ($f_T\uparrow$)
- **base bandgap grading produces higher Early voltage** ($V_A\uparrow$)



$$\left.\frac{\beta_{SiGe}}{\beta_{si}}\right|_{V_{BE}} \equiv \Xi = \left\{ \frac{\tilde{\gamma}\,\tilde{\eta}\,\Delta E_{g,Ge}(grade)/kT\; e^{\Delta E_{g,Ge}(0)/kT}}{1 - e^{-\Delta E_{g,Ge}(grade)/kT}} \right\}$$

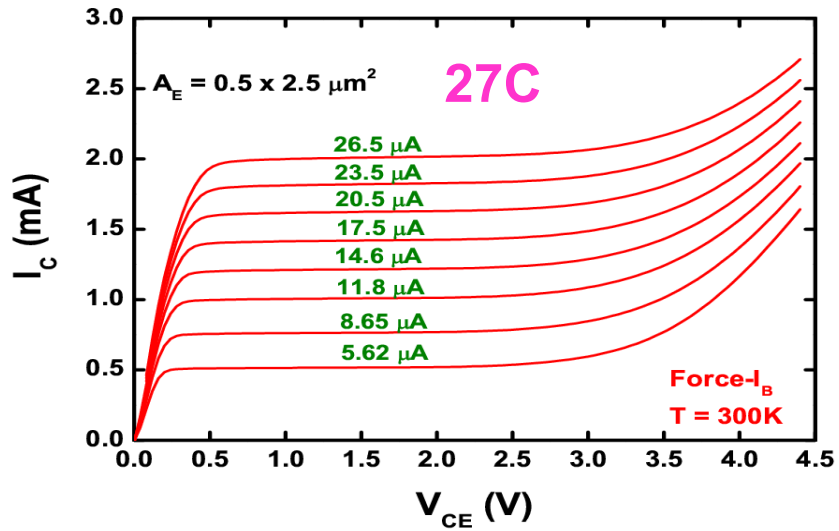
$$\frac{\tau_{b,SiGe}}{\tau_{b,Si}} = \frac{2}{\tilde{\eta}} \frac{kT}{\Delta E_{g,Ge}(grade)} \left\{ 1 - \frac{kT}{\Delta E_{g,Ge}(grade)} \left[1 - e^{-\Delta E_{g,Ge}(grade)/kT} \right] \right\}$$

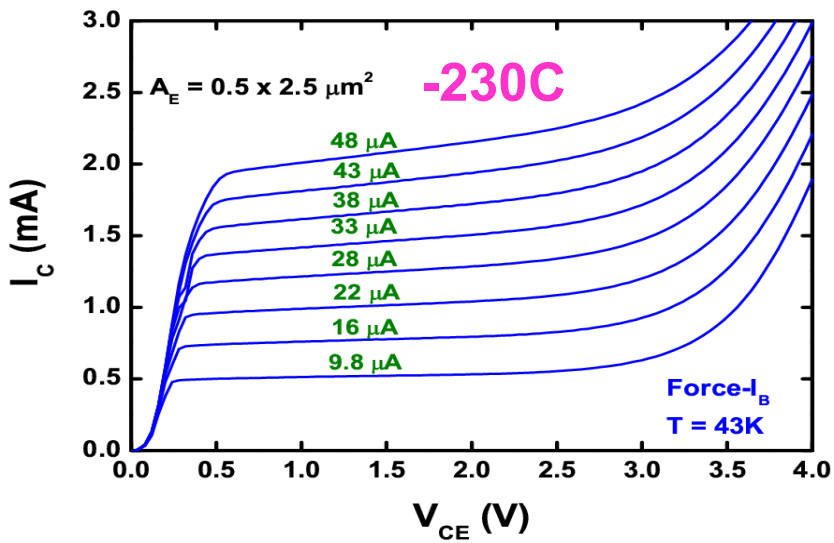
$$\left.\frac{V_{A,SiGe}}{V_{A,Si}}\right|_{V_{BE}} \equiv \Theta \simeq e^{\Delta E_{g,Ge}(grade)/kT} \left[\frac{1 - e^{-\Delta E_{g,Ge}(grade)/kT}}{\Delta E_{g,Ge}(grade)/kT} \right]$$

All kT Factors Are Arranged to Help at Cryo-T!

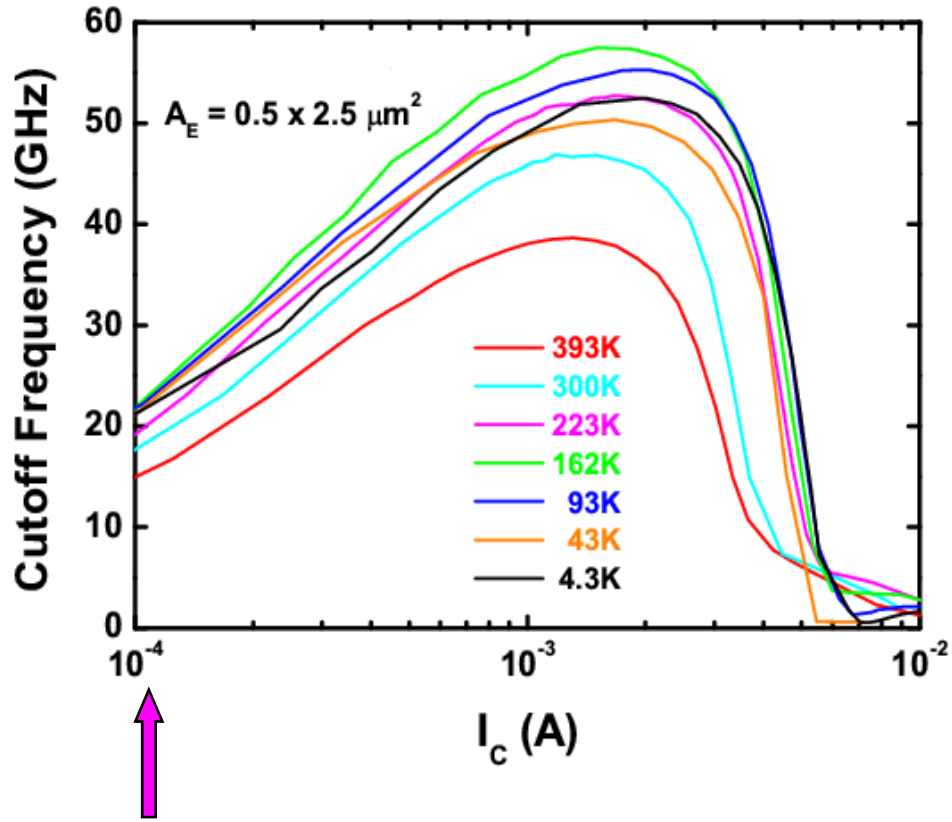
SiGe HBTs at Cryo-T

dc





ac



SiGe Exhibits Very High Speed at Very Low Power!

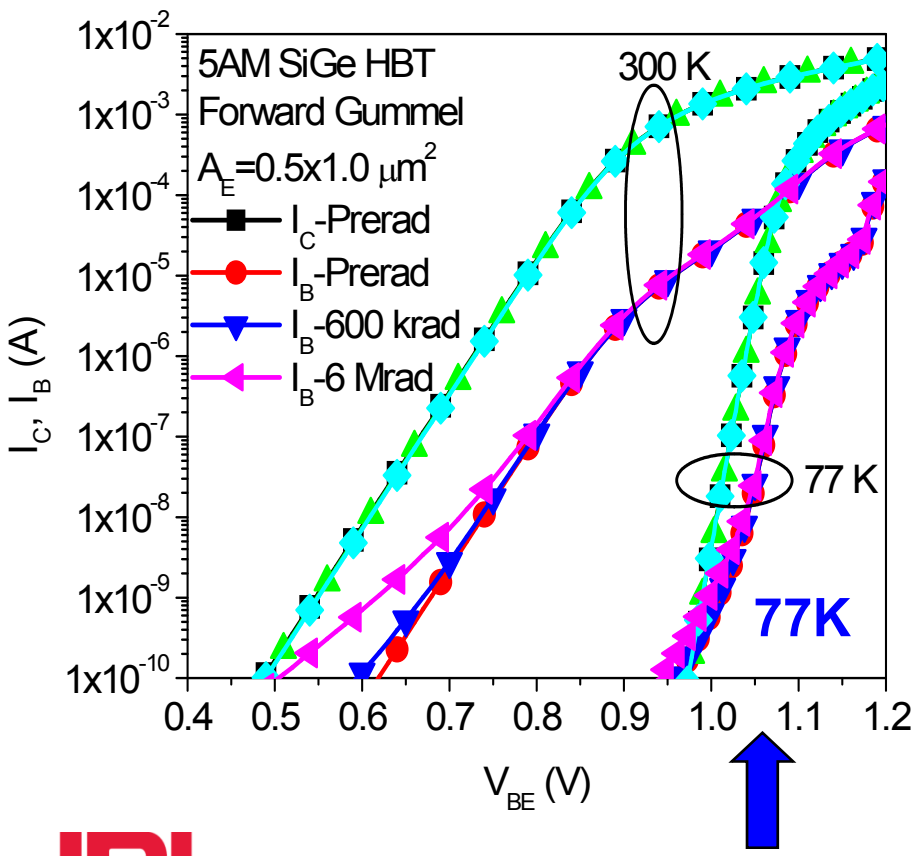
First Generation SiGe HBT

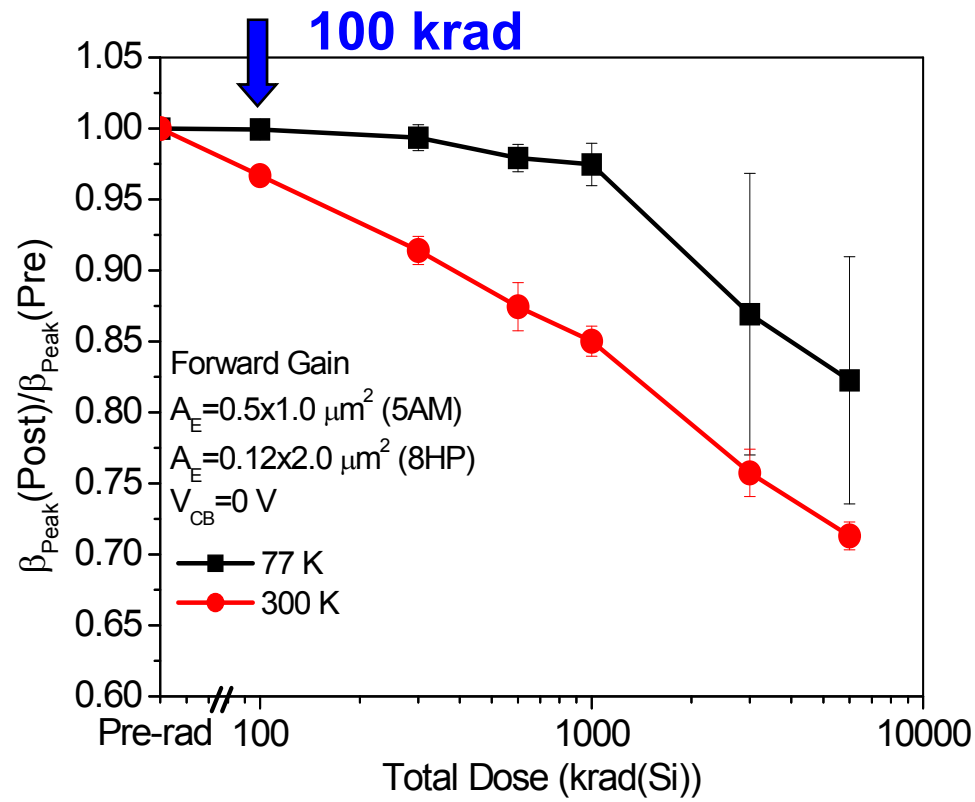
Cryo-T Radiation

First 77K Proton Irradiation Experiment in SiGe Technology

- 63 MeV protons at UC Davis

- **Radiation Damage Smaller at 77K Than at 300K (great news!)**





no change in peak β at 100 krad at 77K!

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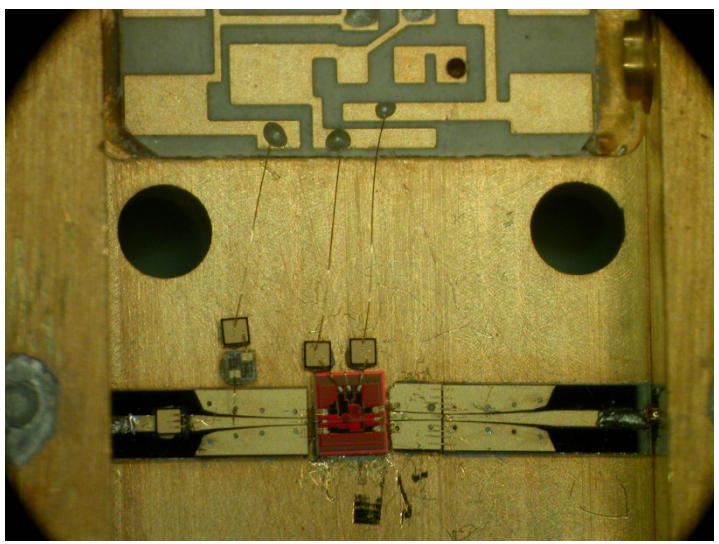
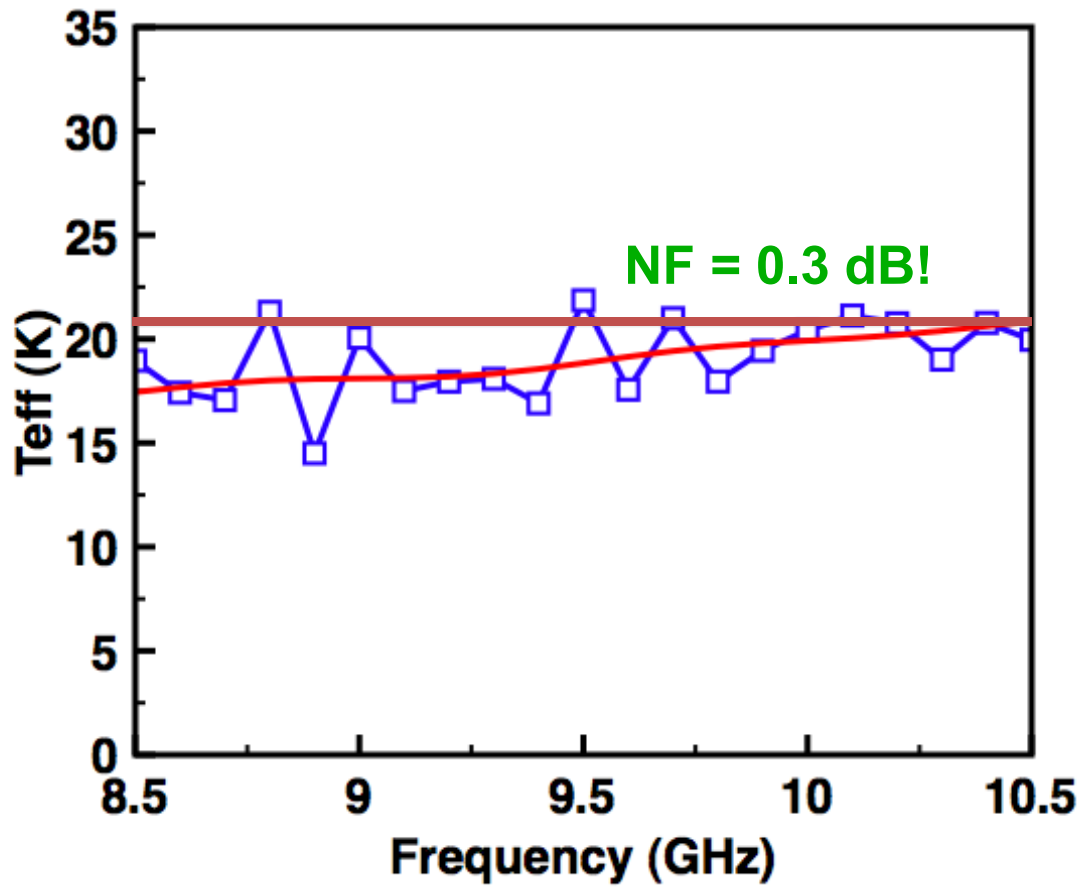
Cryogenic SiGe LNAs

X-band LNA Operation at 15 K (Not Yet Optimized!)

- T_{eff} < 20 K (noise T)
- NF < 0.3 dB
- Gain > 20 dB
- *dc* power < 2 mW





Collaboration with S. Weinreb, Cal Tech

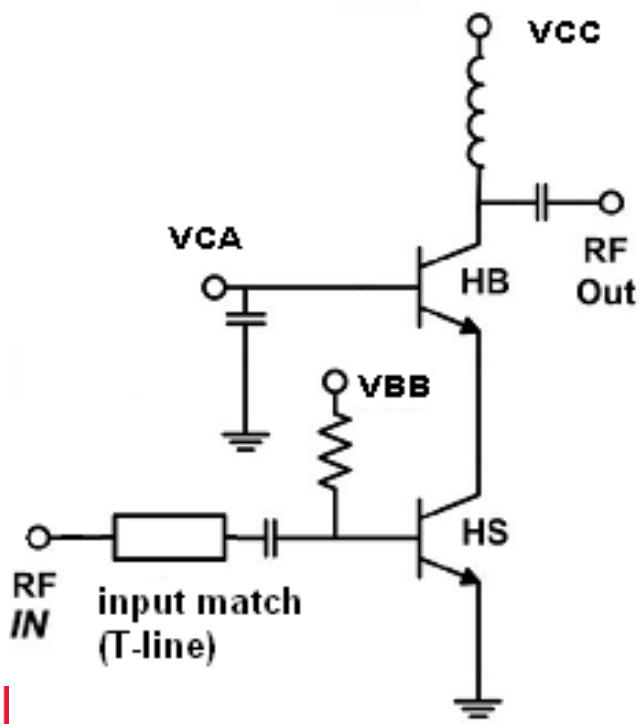
This SiGe LNA is also Rad-Hard!

Aggressive Cascode X-band SiGe PA

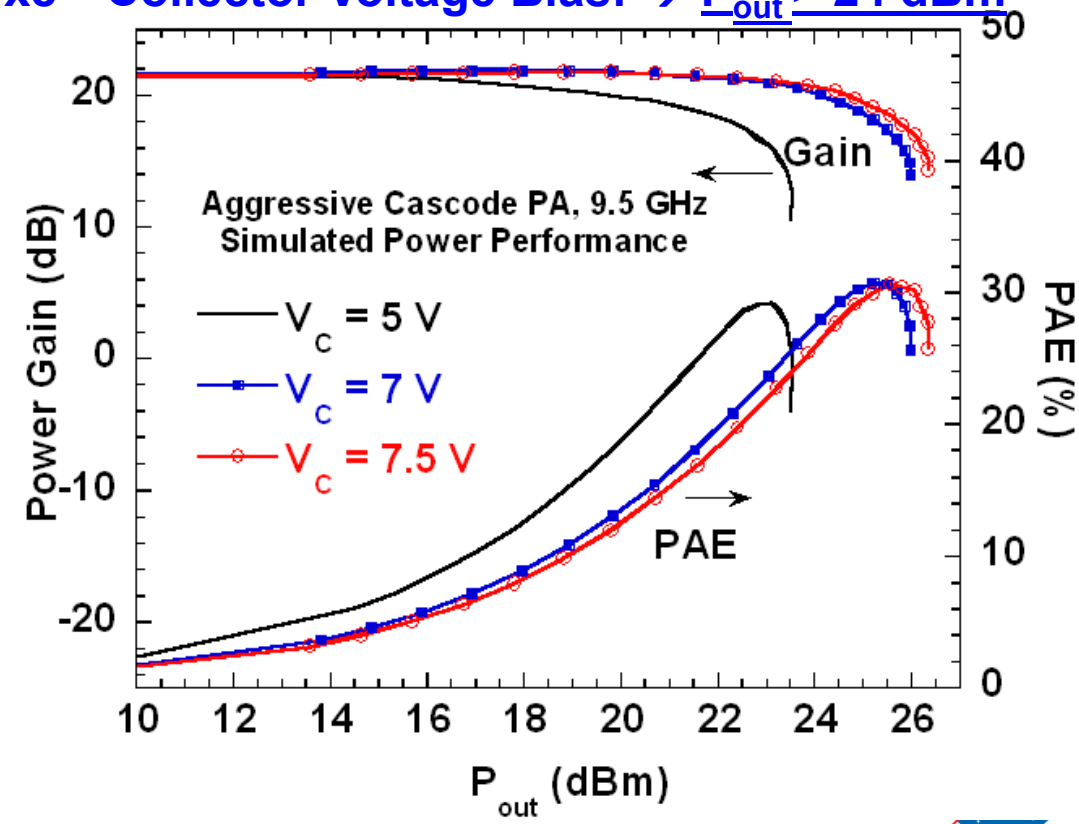
- **Current ¼-W SiGe X-band solution (5V): 32 parallel devices**
- **Can this P_{out} be achieved with a smaller (20 dBm) PA core?**

→ Design Cascode PA Using Aggressive V_C Bias

Single-stage Cascode PA Schematic: (0.12x18um² HS → 0.6x18um² HB) x8



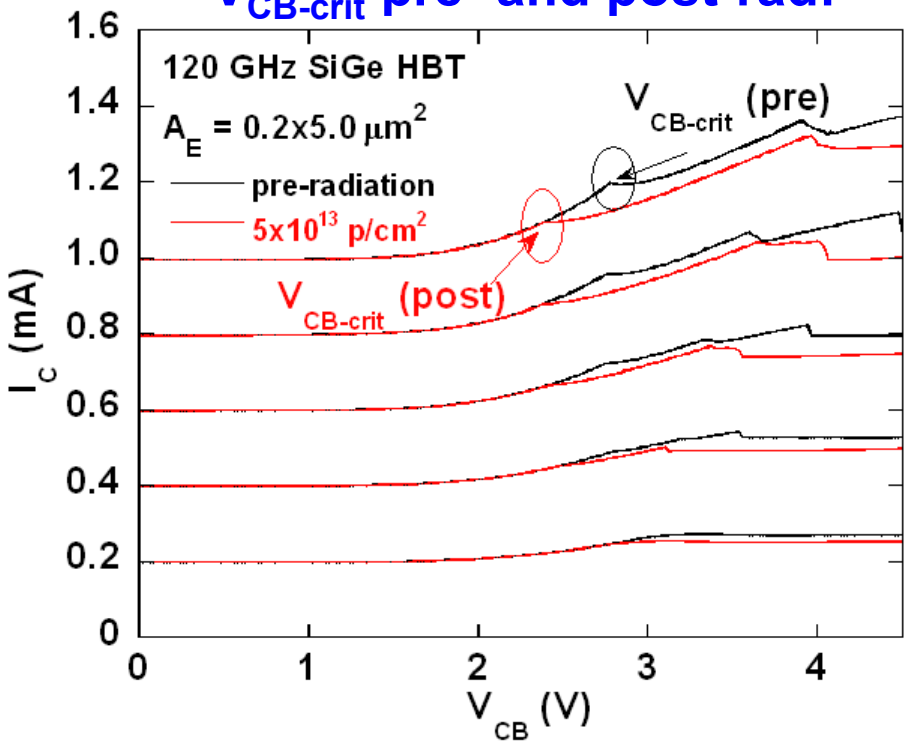
Power Simulations With Aggressive Collector Voltage Bias: → P_{out} > 24 dBm



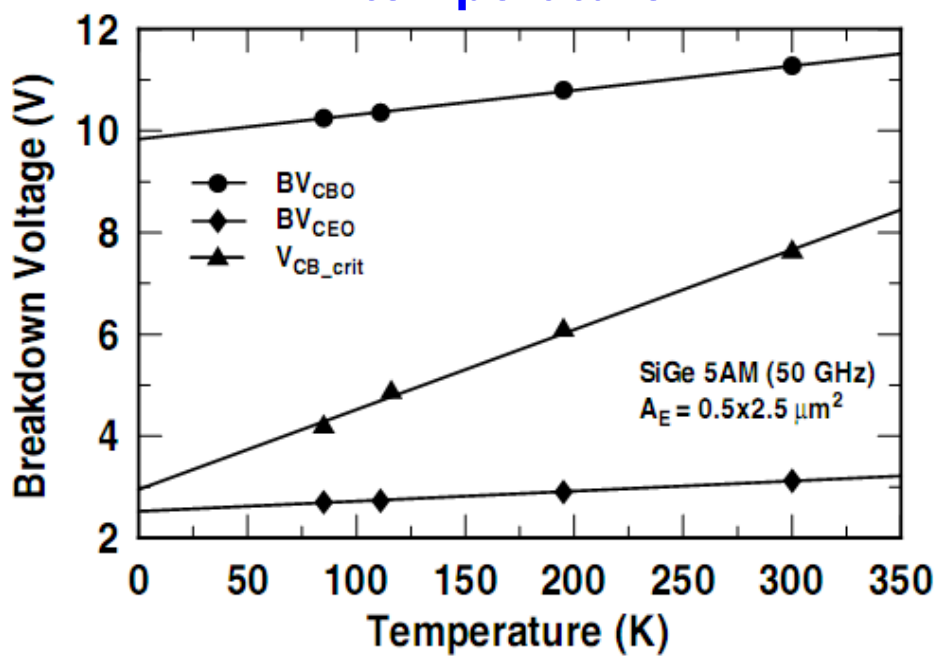
SiGe BV - Extreme Environments

- **Both radiation and low T degrade the CB SOA**

CB – forced I_E measurement $V_{CB\text{-}crit}$ pre- and post-rad:



Breakdown voltage across temperature:



[21] C. Zhu et al. "Assessing reliability issues in cryogenically-operated SiGe HBT's," IEEE BCTM, pp. 41–44, 2005.

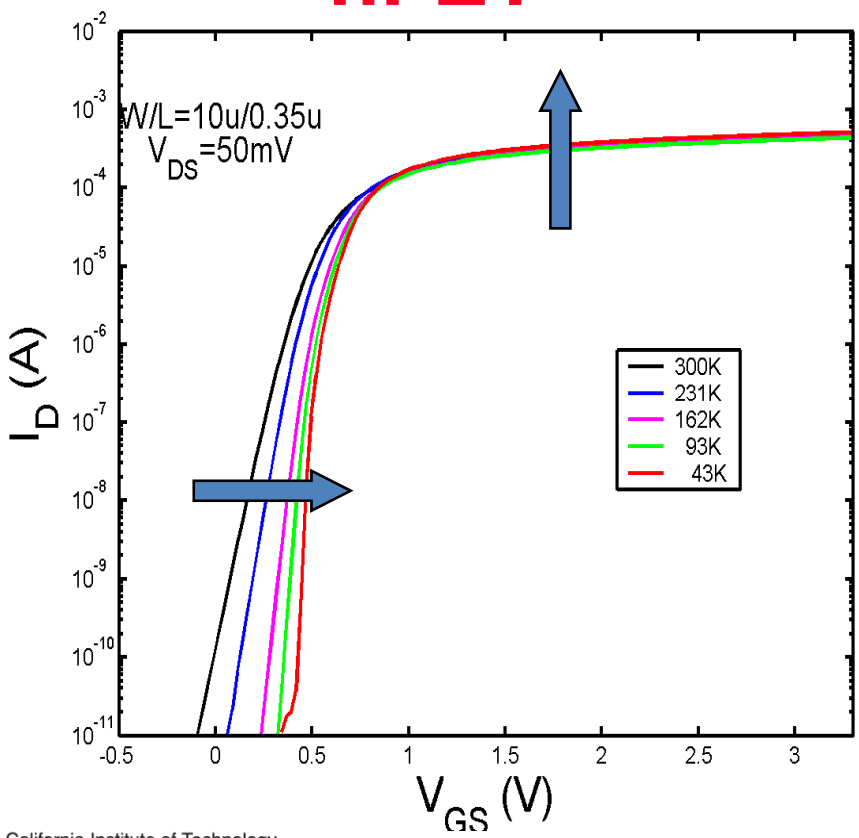
➢ **CB stability analysis used to examine various pinch-in influences**

Cryogenic Operation of CMOS

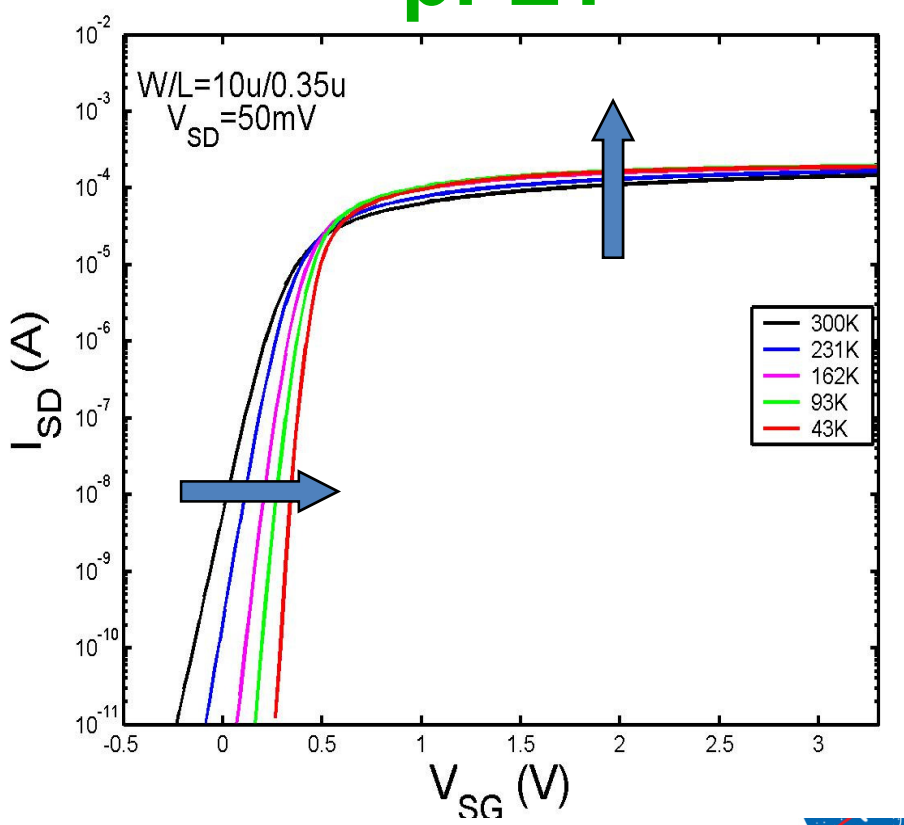
Sub-Threshold Behavior

- **First Generation SiGe BiCMOS (0.35 um L_{eff})**
- **V_T and Subthreshold Swing Increase with Cooling**
- **Output Drive Improves with Cooling**

nFET



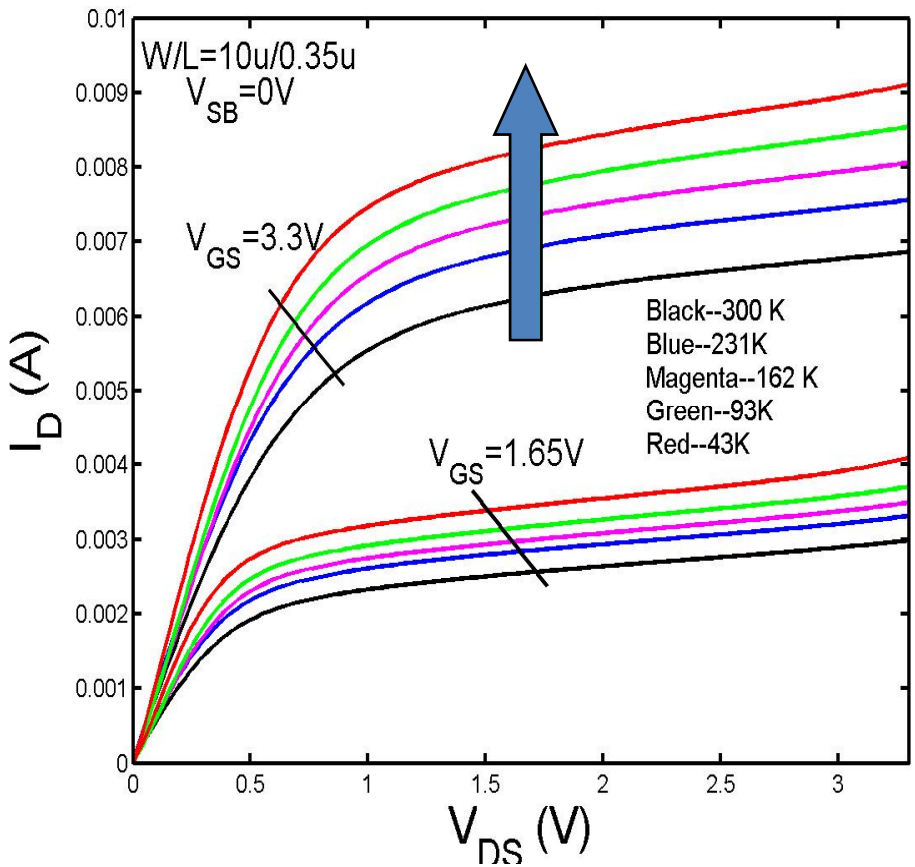
pFET



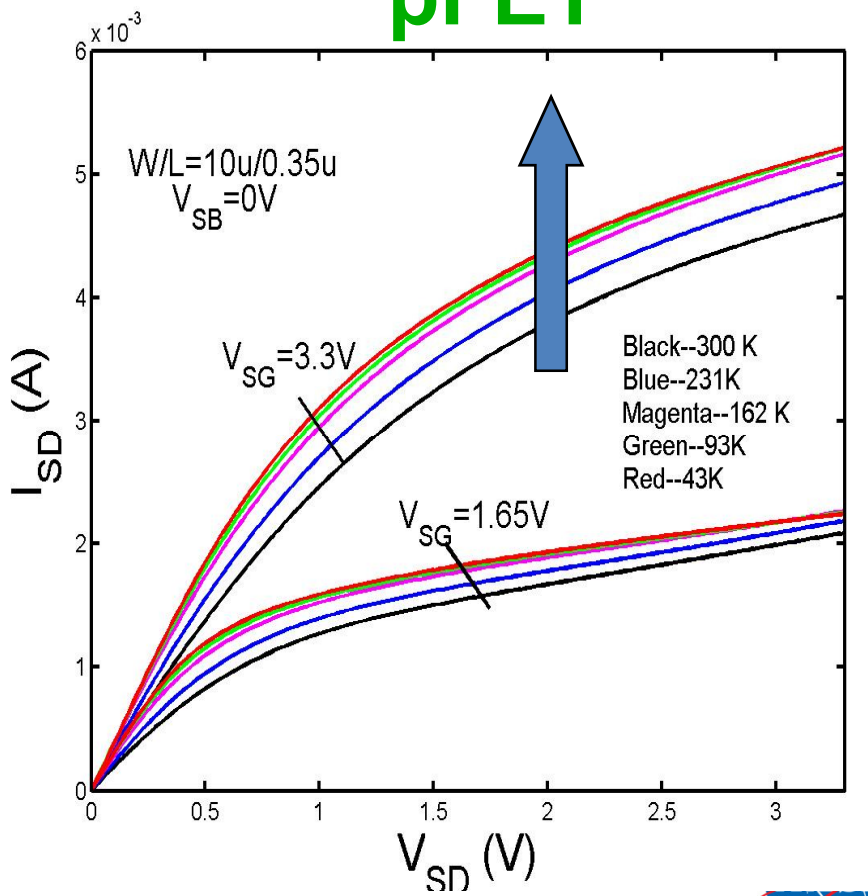
Output Characteristics

- **Improved Current Drive With Cooling**
- **Modest Degradation in Output Conductance**

nFET

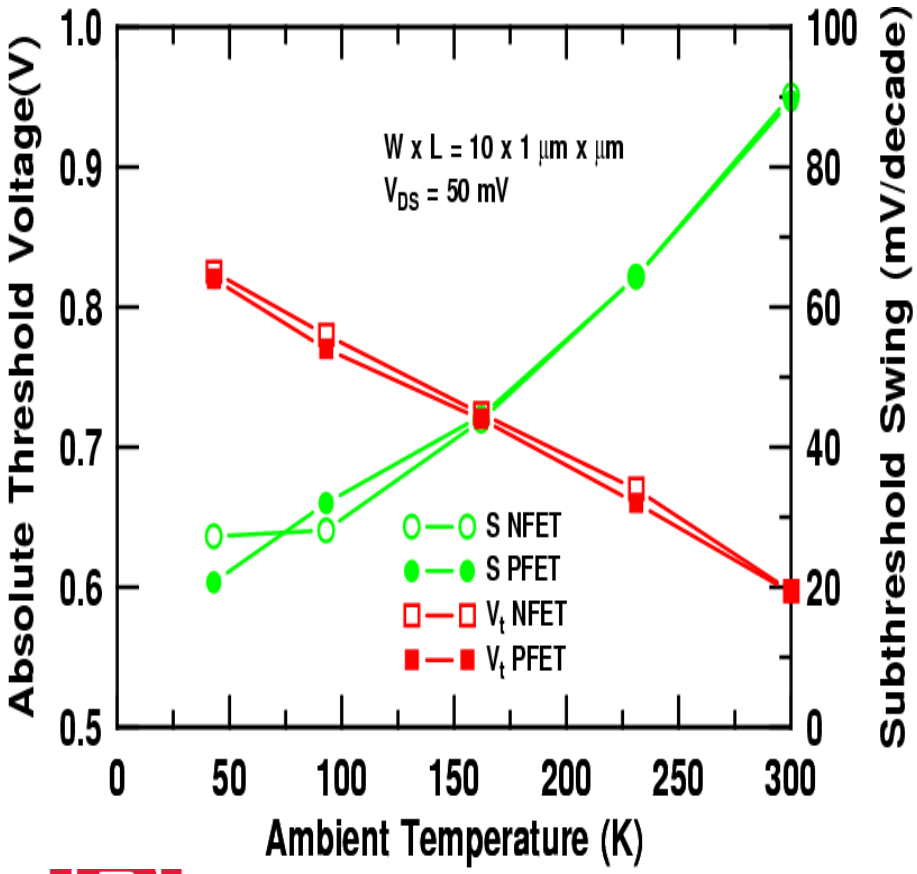


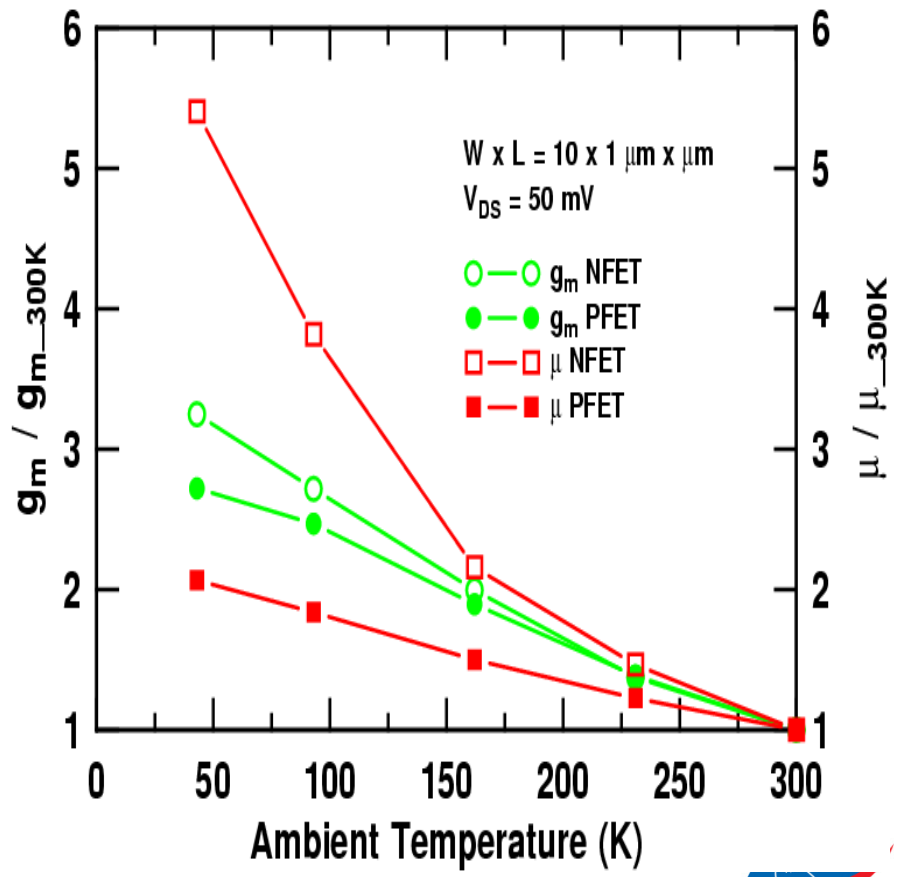
pFET



T Dependence

- V_T Increases with Cooling / S Decreases with Cooling
- g_m Increases with Cooling / μ Increases with Cooling





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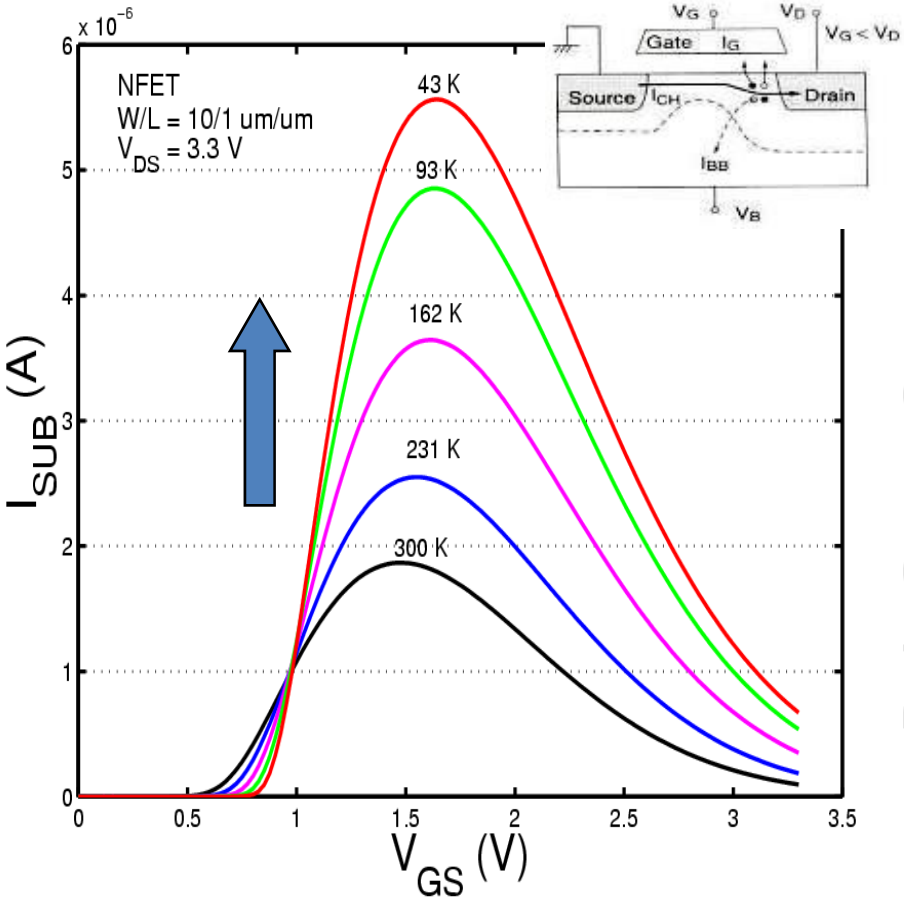
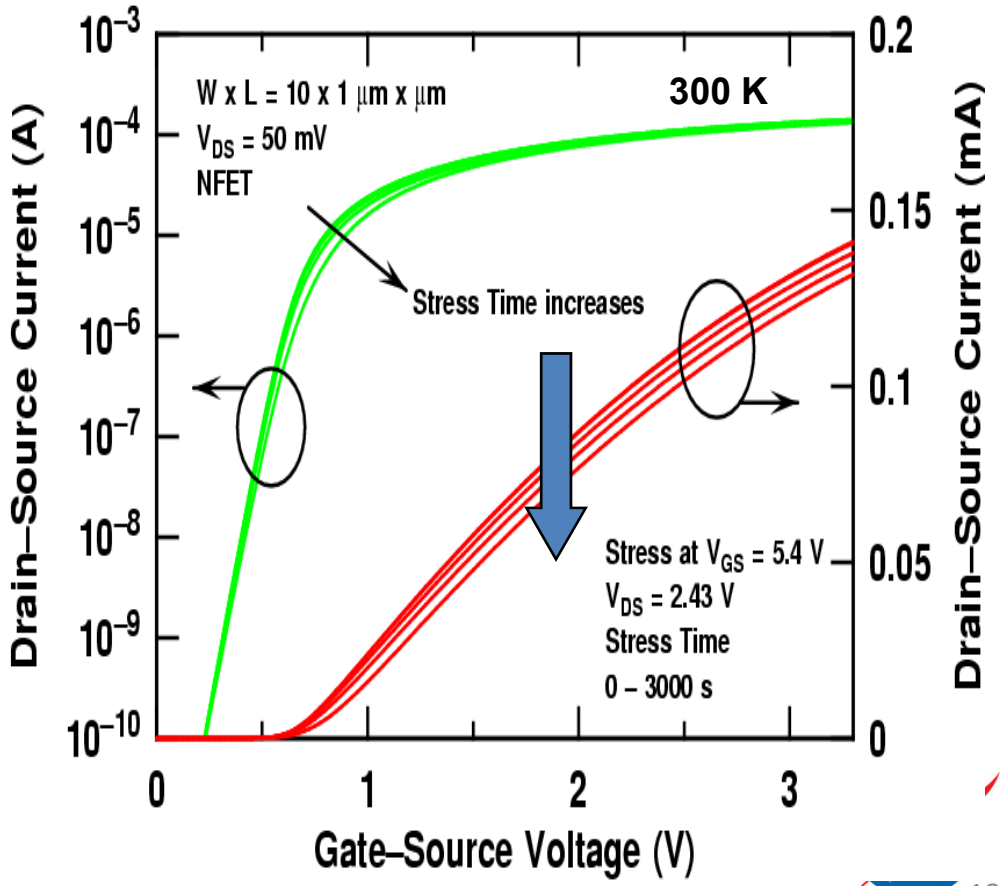
How About Reliability?

Device Reliability

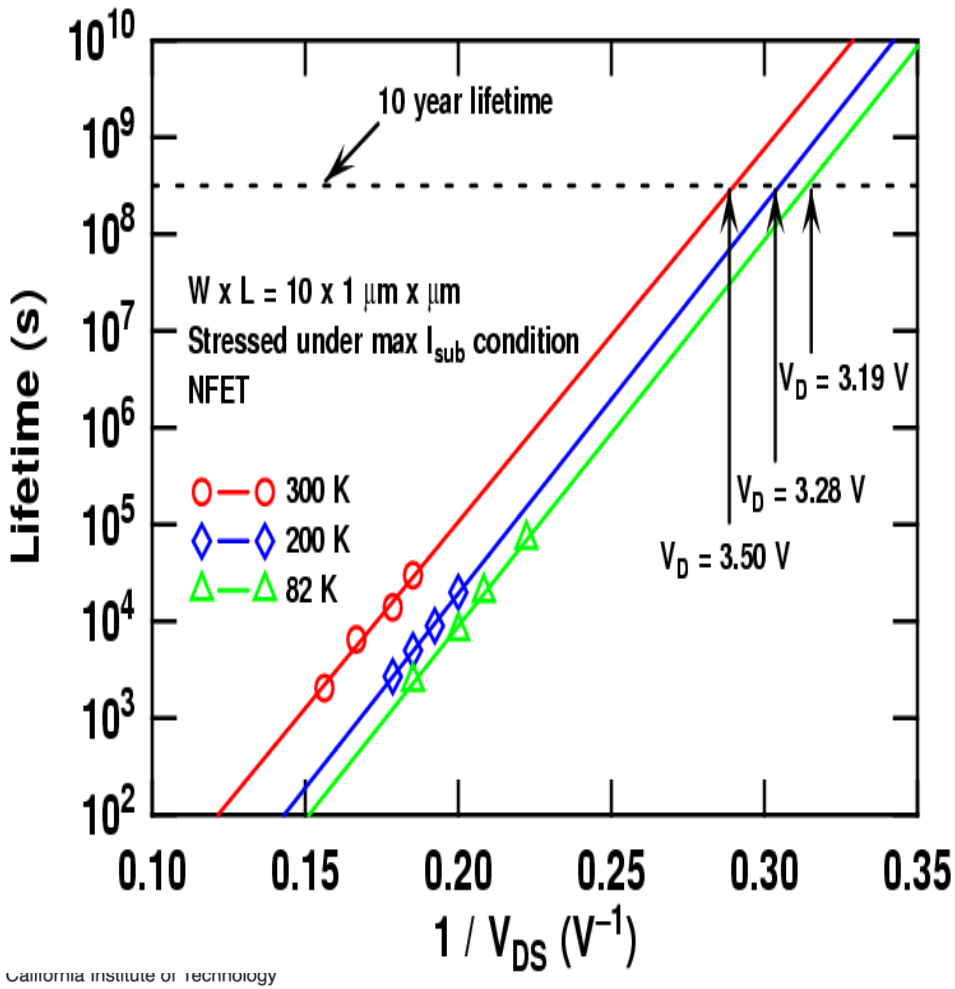
- I_{SUB} is a Good Monitoring Parameter for HCE
- After Stress, I_d and g_m Decrease While V_T and S Increase

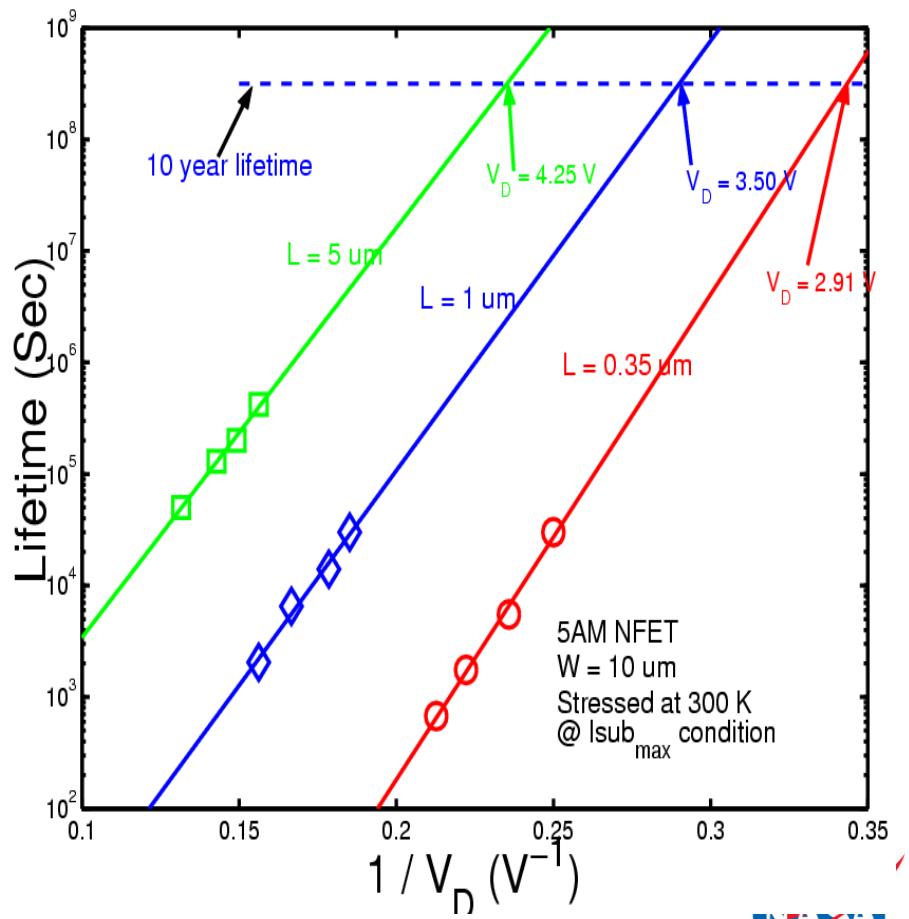




MOSFET L,T Dependence

- **Lifetime Decreases with Cooling at Fixed L**
- **Lifetime Decreases with L at Fixed T (Mitigation Path)**

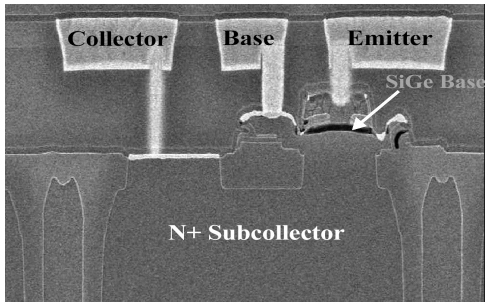


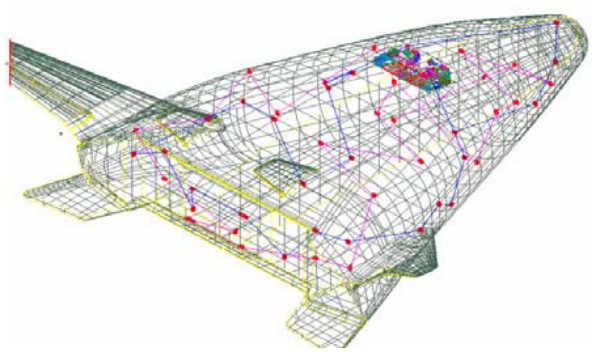


COLD CAPABLE SIGE ASICS

Cold Capable SiGe ASICS

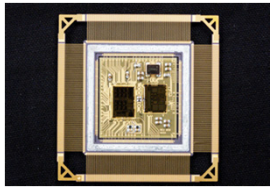
Present	Thinking out of the box
Commercial and military components operate at T > −55°C	CMOS and SiGe BiCMOS circuits designed for T = −180°C
Electronic packaging systems for T > −55°C	Cryogenic packaging technology shown to operate at T = −180°C





X-33 space plane with distributed RHN health management system

RHN health management system



SiGe Low Temp Electronics for Vehicle Health Monitoring

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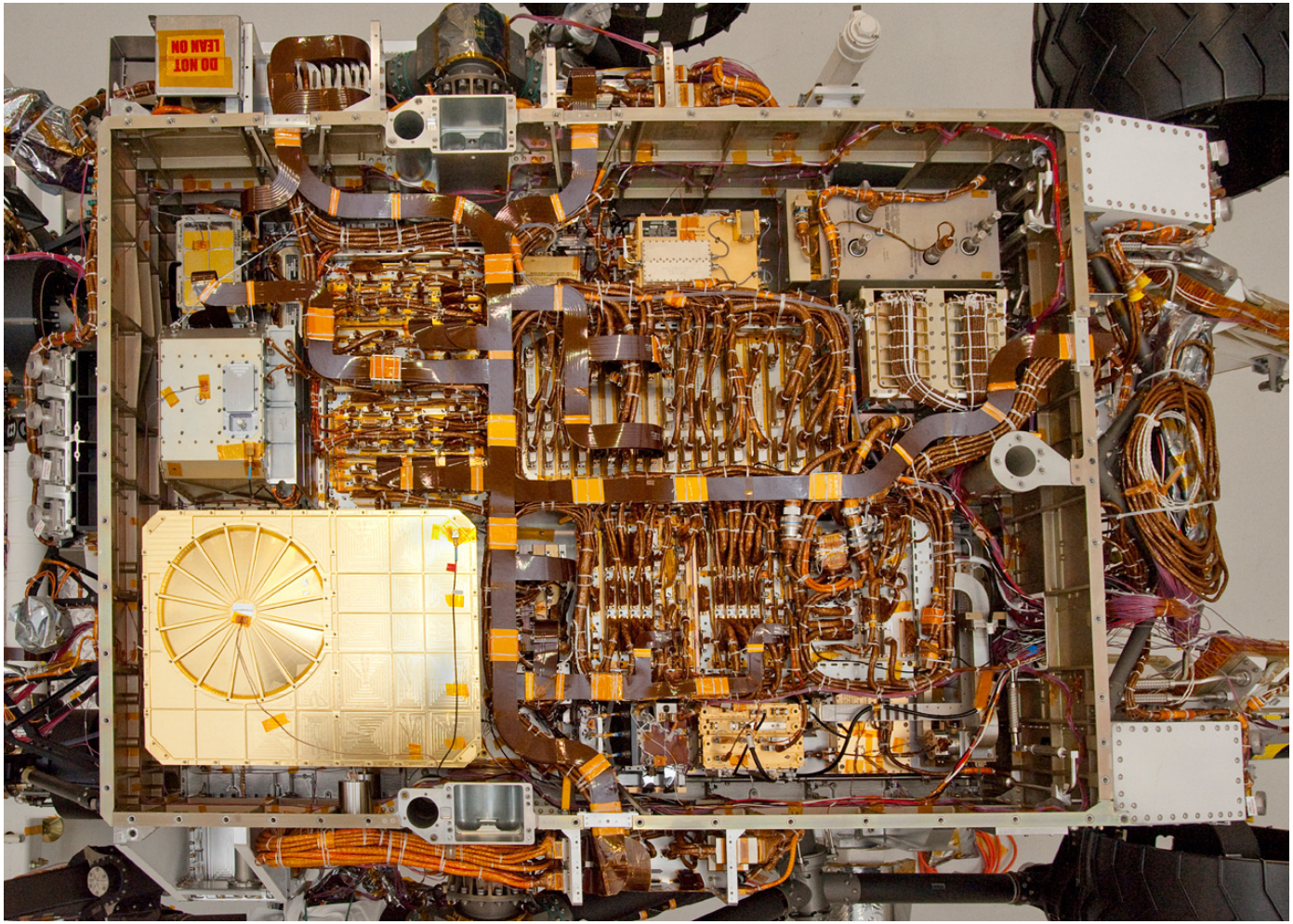
DISTRIBUTED MOTOR CONTROLLER (DMC)

Electronics architecture, ASIC design and Breadboard implementation

Centralized Motor Control

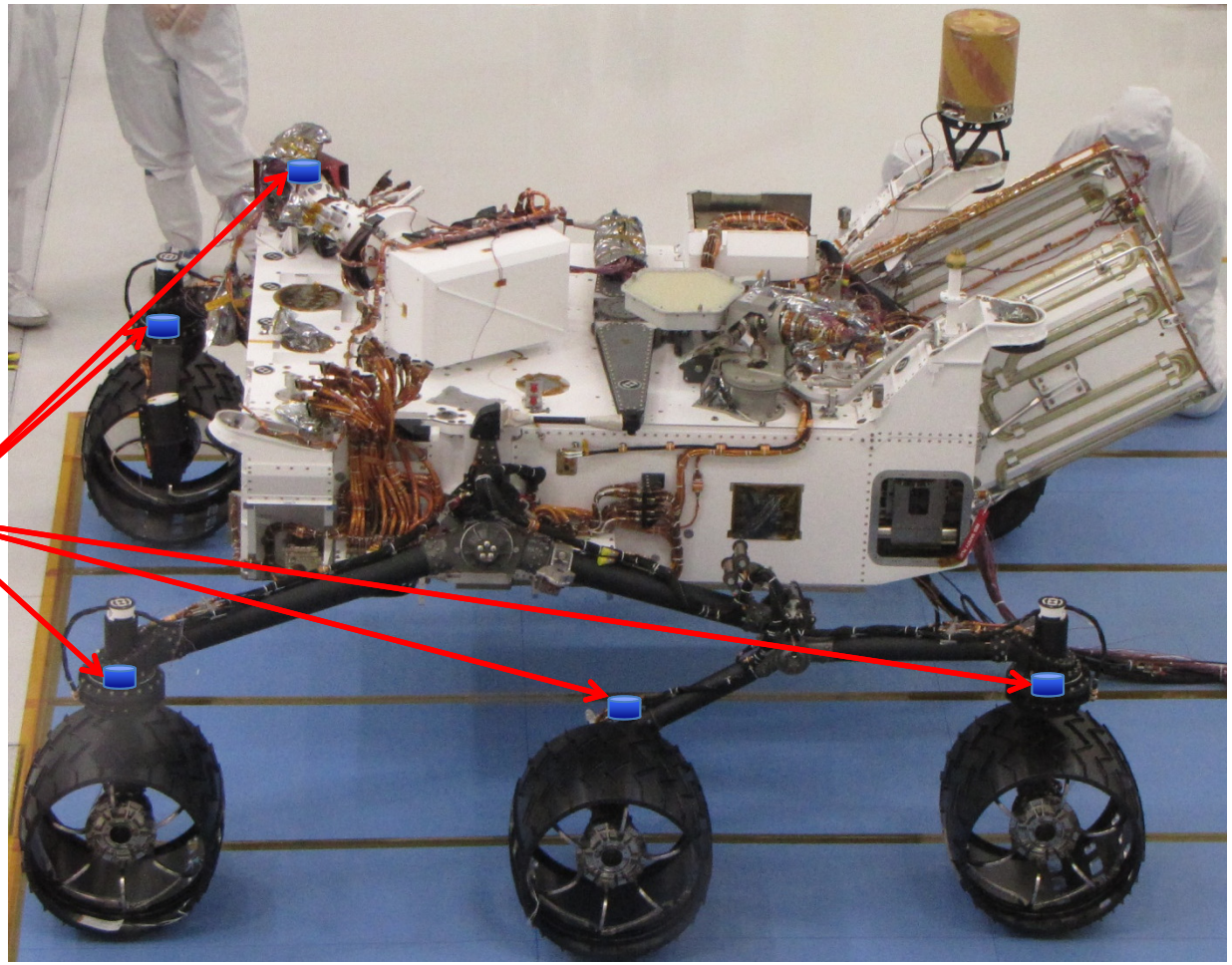


MSL Warm Box top view

Distributed Motor Control

Reduction in Wiring
-Power Bus
-Network Bus

Localized
Motor
Controller



Hardware Specifications
-Wider Temperature
-150°C , 85°C
-Radiation Tolerant

Rover System	Pathfinder	MER	MSL	MSL w/DMC (Projected)
Total Wiring Mass	1.4 Kg	10.4 Kg	52.7 Kg	37 Kg
Actuator Wiring Mass	0.35 Kg	3.0 Kg	17.4 Kg	1.8 Kg
Percentage of Actuator Harness Mass	25 %	29 %	33 %	5 %

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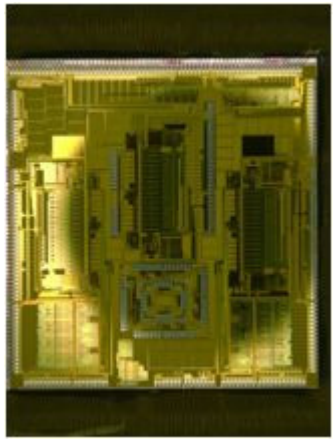
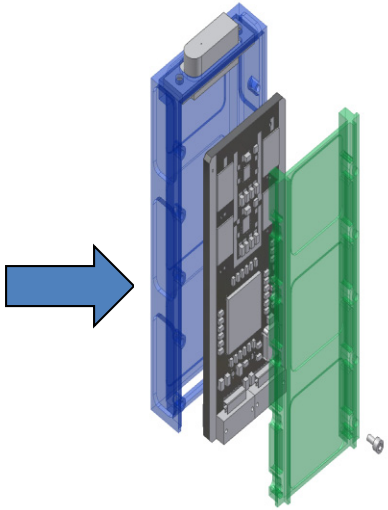
SiGe ASIC for Dist Motor Controller

MSL Warm Electronics Box

MSL Actuator wiring Harness

MSL in High Bay





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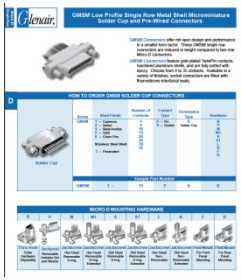
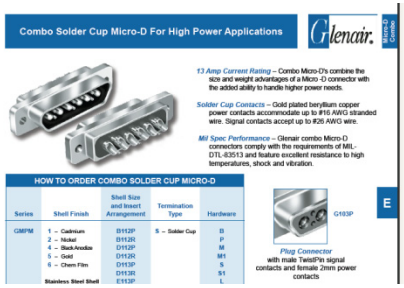
DMC II Baseline Packaging Approach

Allows for
95 IOs

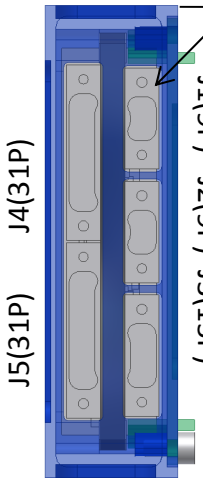
CBE = 99.32 gm

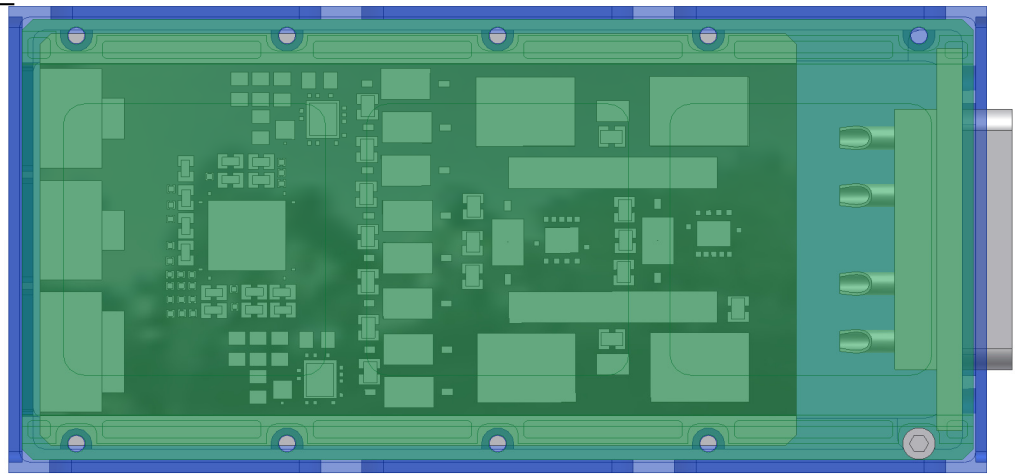


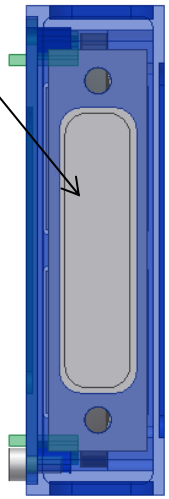
- **J1 – Bus ID (8 pins/1 spare)**
- **J2 – Warm Card I/F (7 pins/2 spares)**
  - >4 pins – motor Bus A & B
  - >3 pins – phantom power A & B
- **J3 – Bus Power 28V**
- **J4 & J5 – I/F to Actuator**
  - >21 pins – Resolver/LVDT
  - >16 pins – Encoder
  - >3 pins – potentiometer
  - >6 pins – Temp Return
  - >10 pins – Digital I/F
  - >4 pins - Force Sensor



- 4pins Motor Phase
- 2pins Brake
- 4pins Heater







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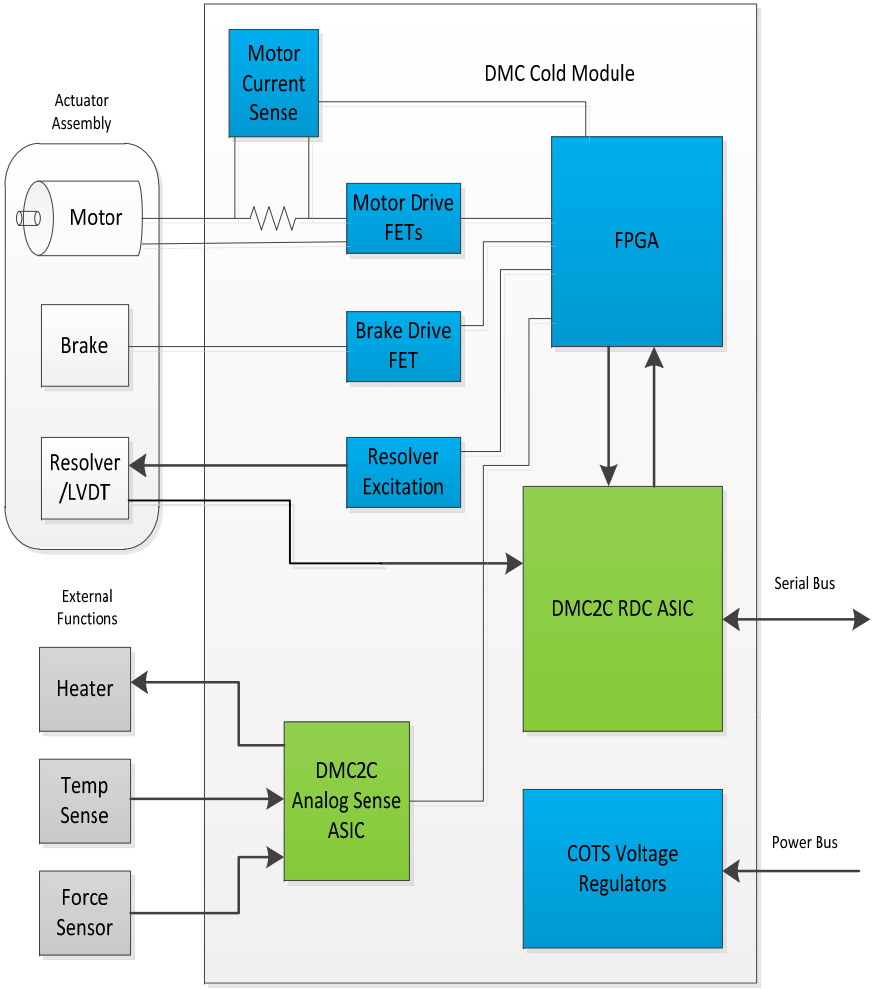
Update 05/13/2011

DMC Electronics Architecture

DMC electronics module includes:

- Two custom mixed-signal ASICs in IBM SiGe 0.5um
  - Resolver-to-Digital Converter (RDC) chip
  - Analog Sense chip
- COTS FPGA
- 10A motor drive power FETs and gate drivers
- Brake drive
- Resolver excitation for position feedback
- Onboard power regulation from single +28V supply



IBM Silicon Germanium (SiGe) 0.5um

IBM SiGe 5AM process technology is the key enabling feature

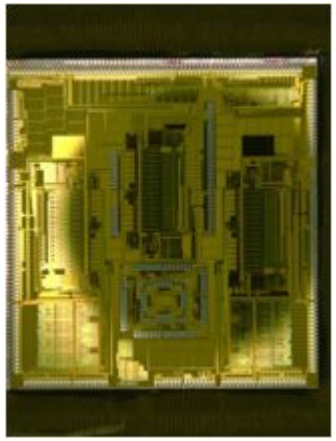
- Wide temperature (-150°C to +85°C) operation
- Radiation tolerant (> 100kRad Total Integrated Dose)
- Excellent analog circuit performance
- Low cost
- Leveraging proven performance at temperature through past JPL and NASA (Exploration Development Technology Program) efforts

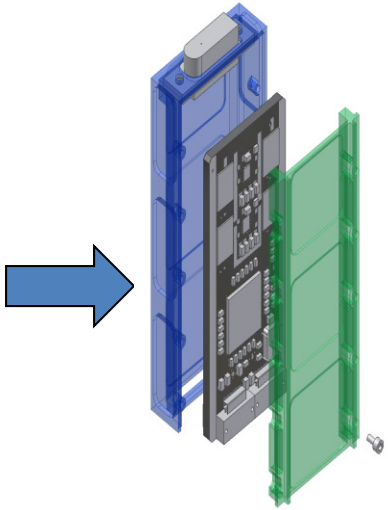
SiGe ASIC for Dist Motor Controller

MSL Warm Electronics Box

MSL Actuator wiring Harness

MSL in High Bay





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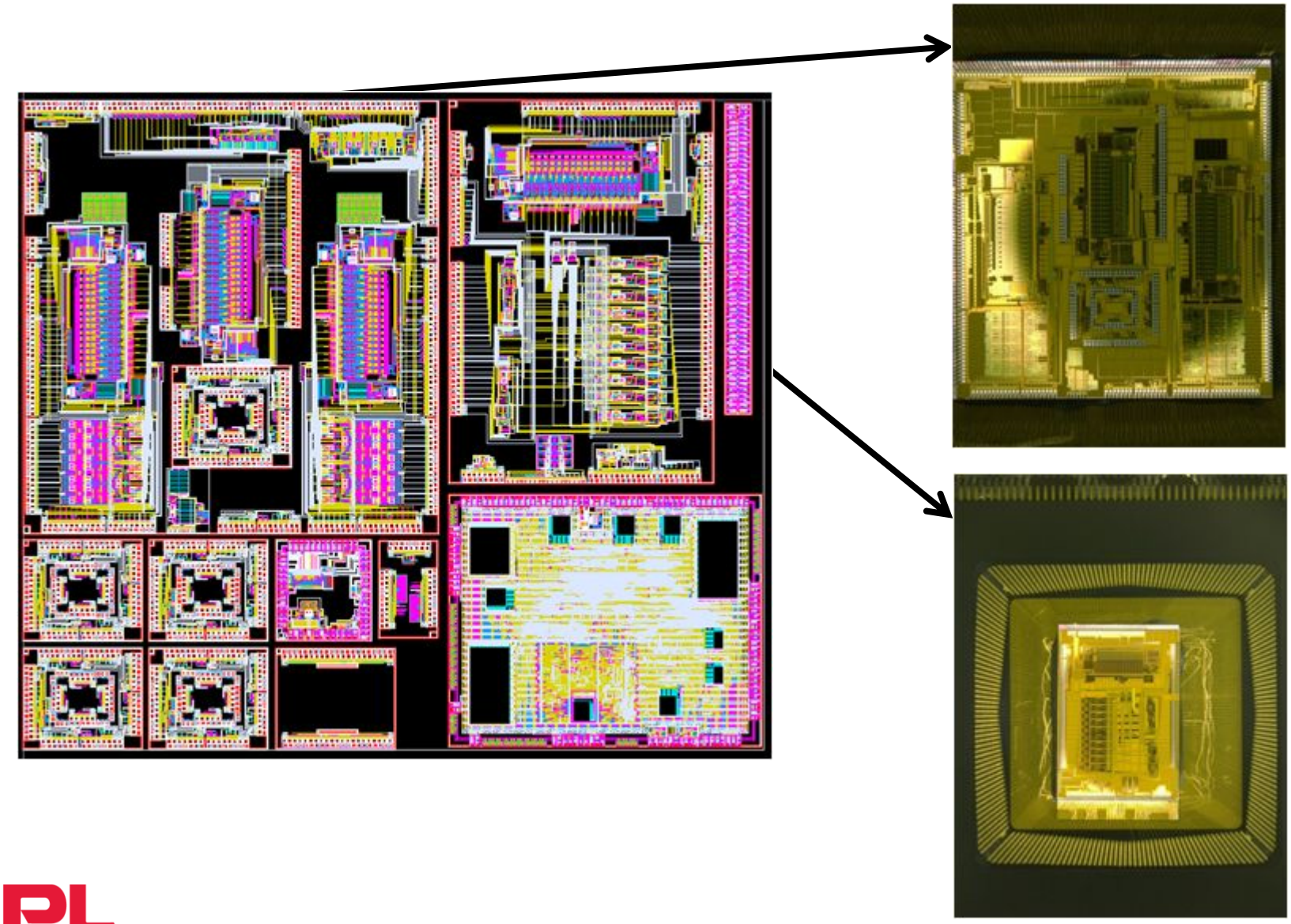
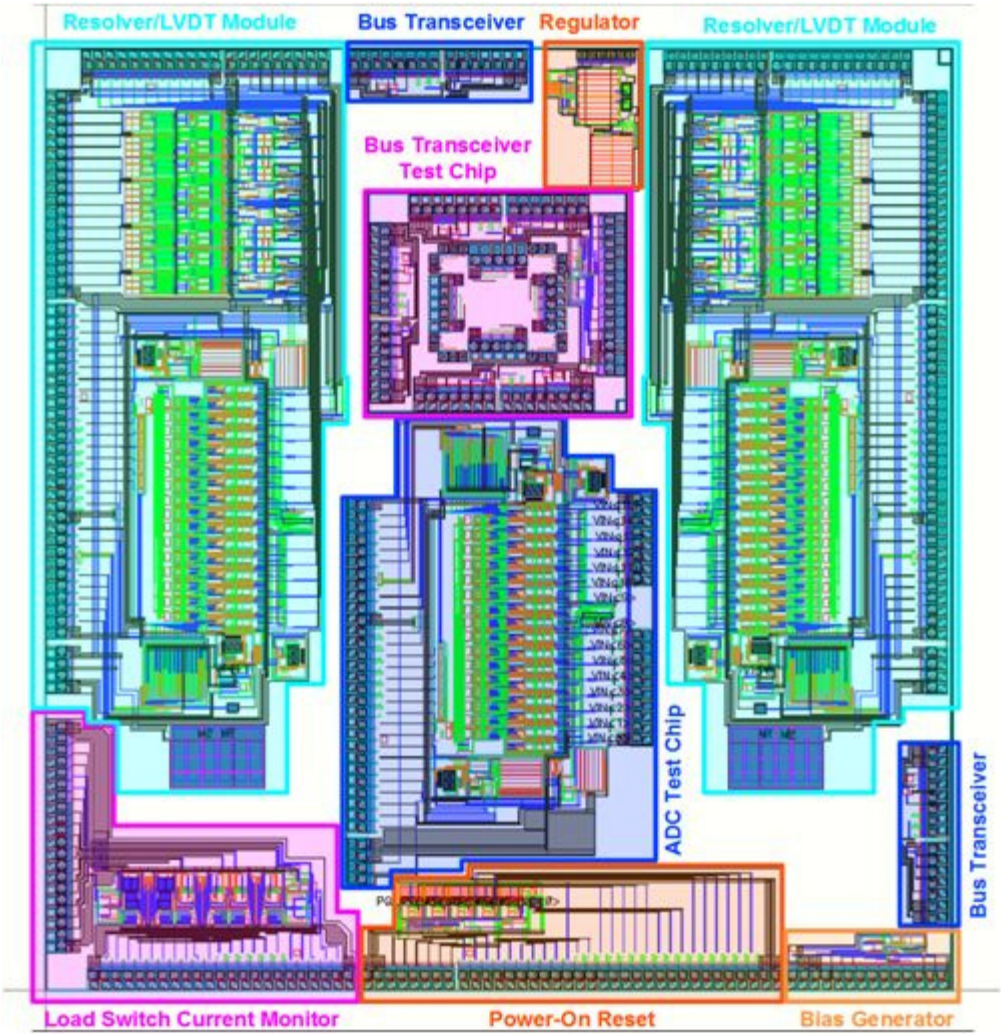
DMC ASIC Reticule

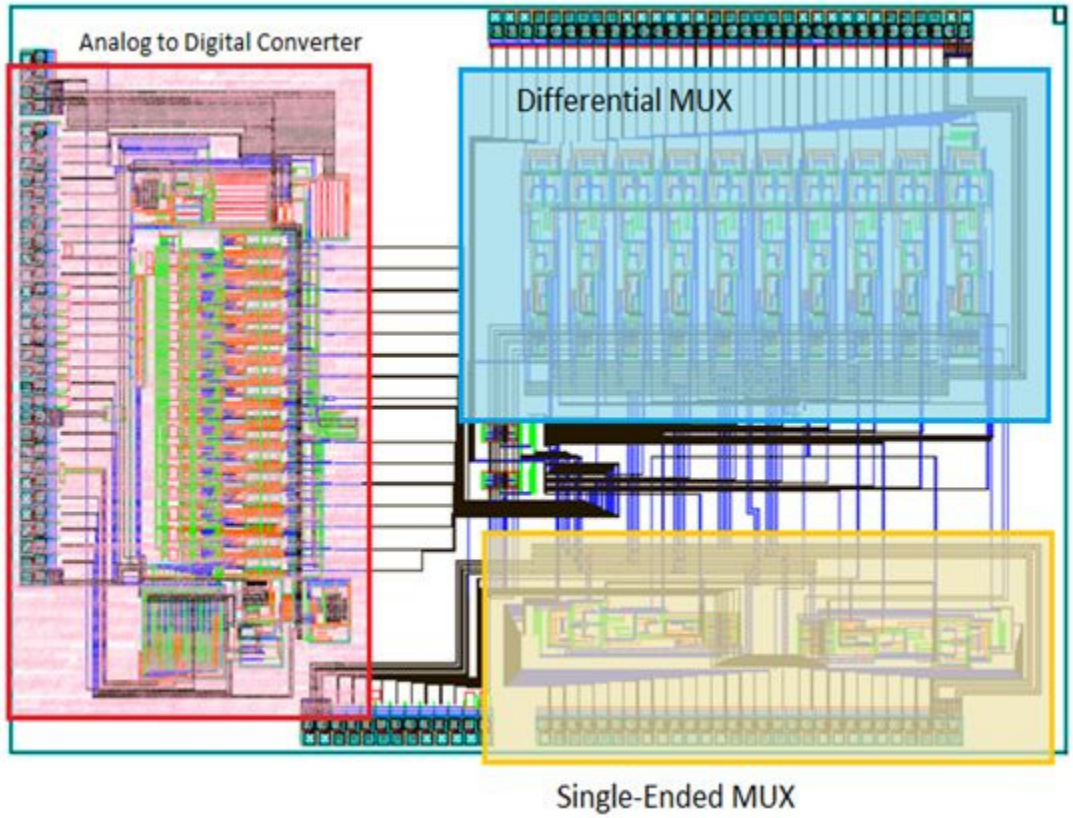


RDC ASIC

- Operates on single 3.3V supply
- Two Resolver/LVDT-to-Digital Converter circuits
  - Digitizes resolver waveforms to deduce motor position to 0.1°
- Load Switch controller
  - Gate driver for power MOSFET enable/disable
- Power-On reset
  - Monitors system voltages and flags FPGA if out of tolerance
- Bus Transceiver
  - 50 Mb/s galvanically-isolated redundant digital bus for communicating with host computer and other DMC modules



Analog Sense ASIC

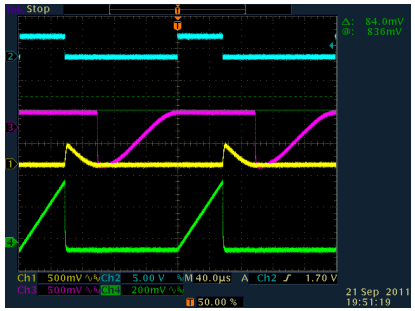


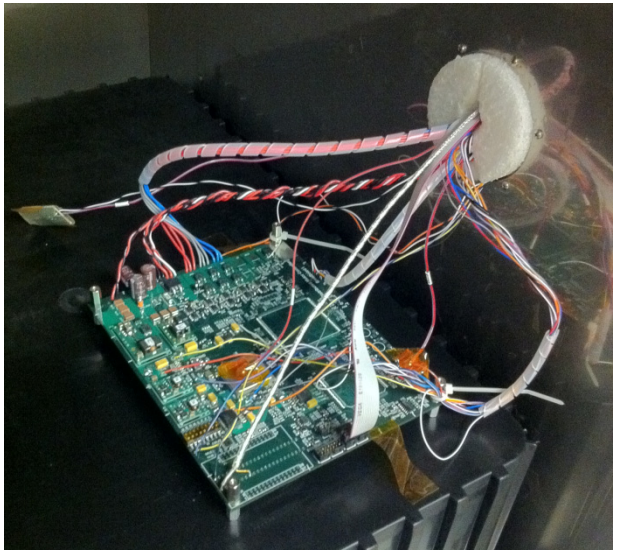
- Operates on single 3.3V supply
- Housekeeping chip to monitor system voltages/currents and motor telemetry
  - 16-input Differential and Single-ended MUXs with independent gain settings
  - Stimulus driver capable of providing 1.2V or 1mA to sensors external to chip
  - Serial digital communication to FPGA

Breadboard

DMC Breadboard 1 (DBB1)

- Single +28V power bus input
- Virtex-5 FPGA
- RS-232 port for PC interface/control
- Power FETs for motor drive and switched power bus





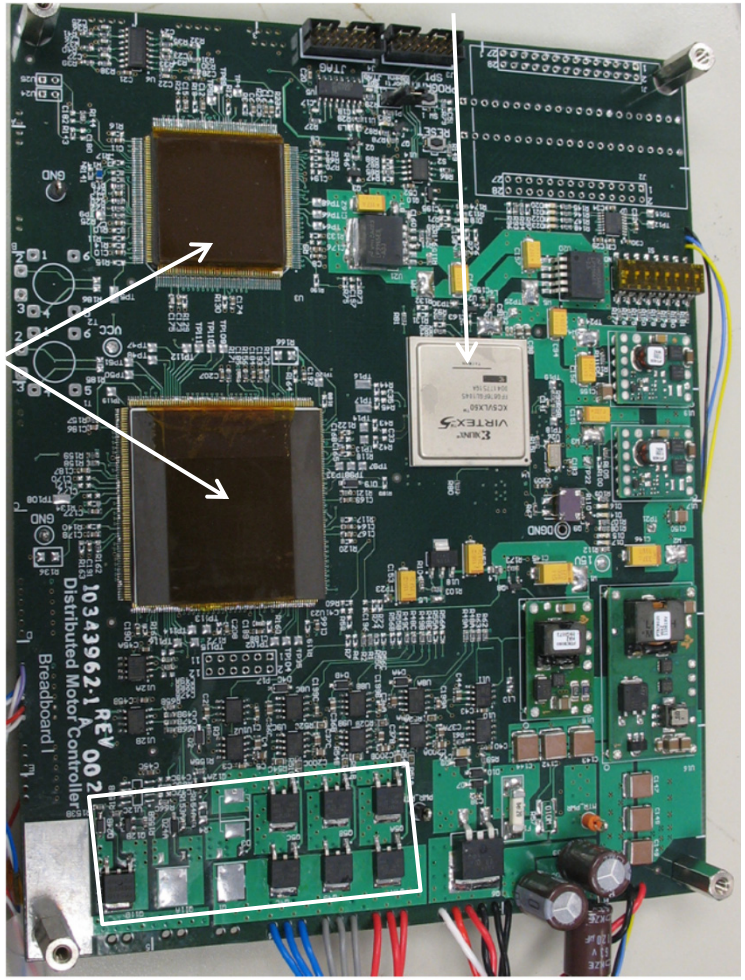
DMC_Video_9_28_11.MOV

DMC_Motor_Running.wmv

Motor + Resolver

FPGA

ASICs

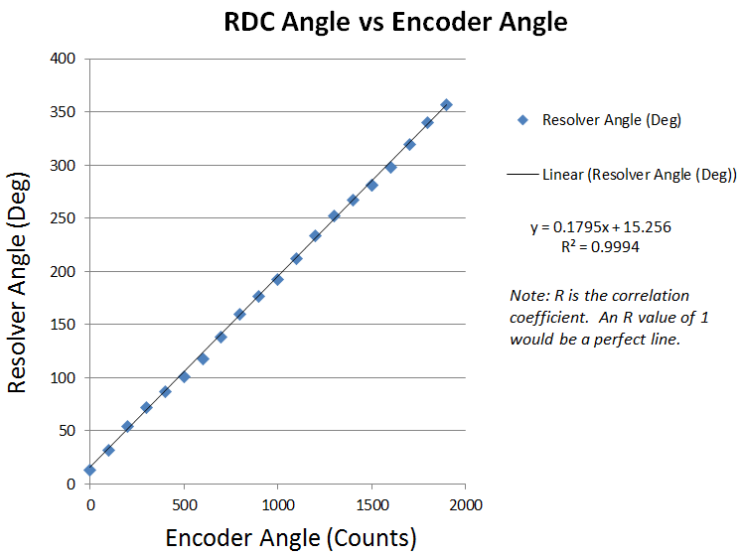


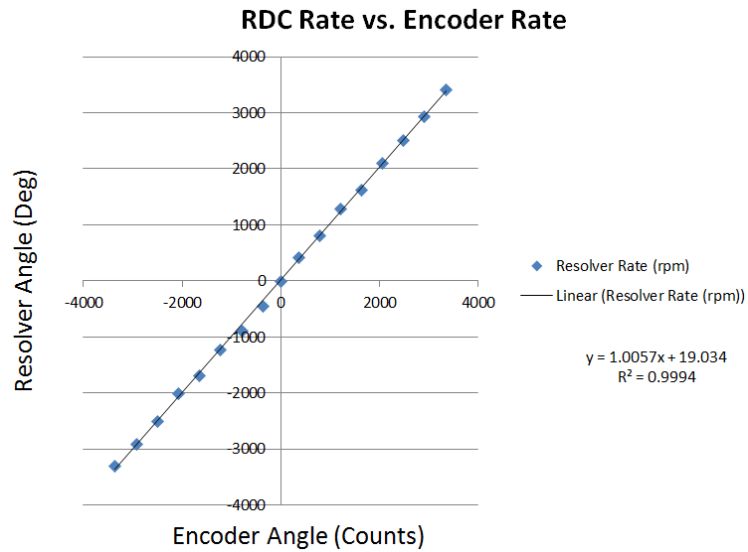
Drivers

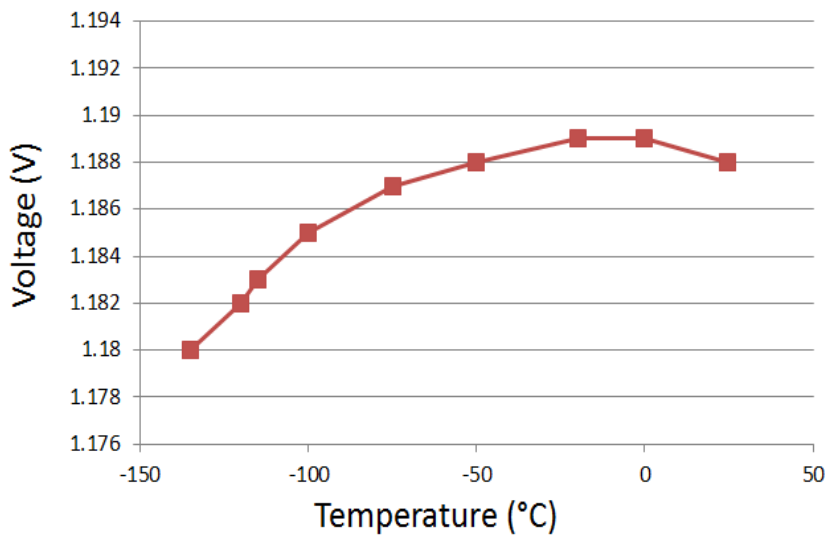
TEST RESULTS

Operation of motor at -135°C

Cold test results

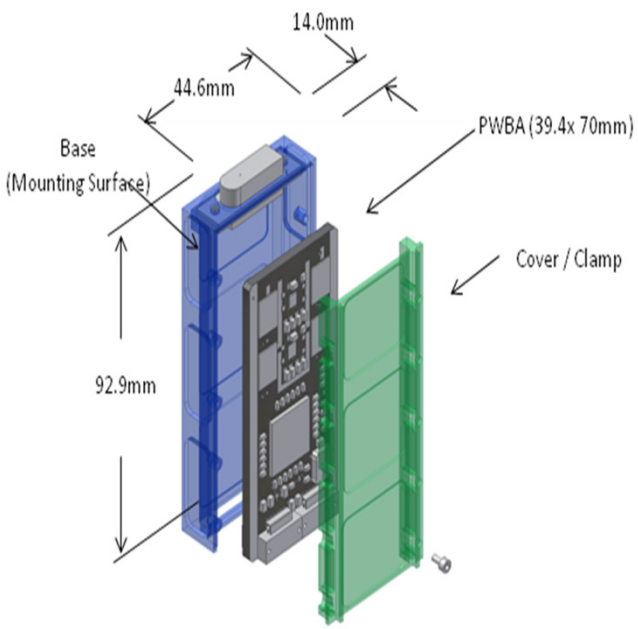


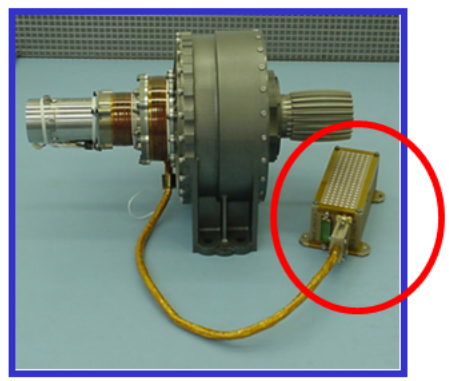


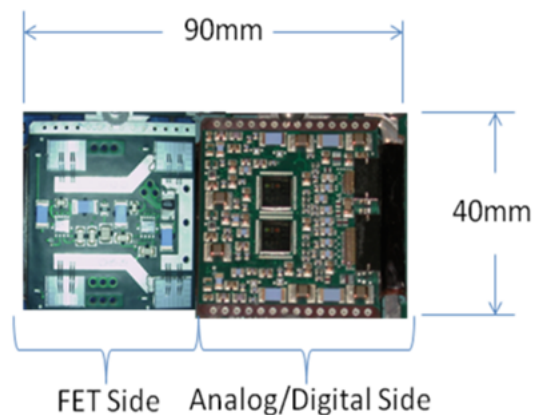


Future work

- Next iteration of mixed-signal ASIC to include
  - Single chip solution
  - Four channel switch-mode power supply controller
  - Fully serial interface between ASICs and FPGA
  - Motor phase current sense
- Digital ASIC from finalized FPGA code
- Extreme environment enclosure







Acknowledgments

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BACKUP MATERIAL