The COVE Payload
A Reconfigurable FPGA-Based Processor for CubeSats

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August 8, 2010
Small Satellite Conference
Logan, UT

Outline

COVE: CubeSat On-board processing Validation Experiment

NASA/Earth Science Technology Office (ESTO) sponsored

- Motivation for COVE
- JPL/U. Michigan Collaboration
- COVE Payload Processor: High-Level Block Diagram
- COVE Development Stages
- Operational Housekeeping
- Final Stages
- Any Interest?
- Acknowledgements

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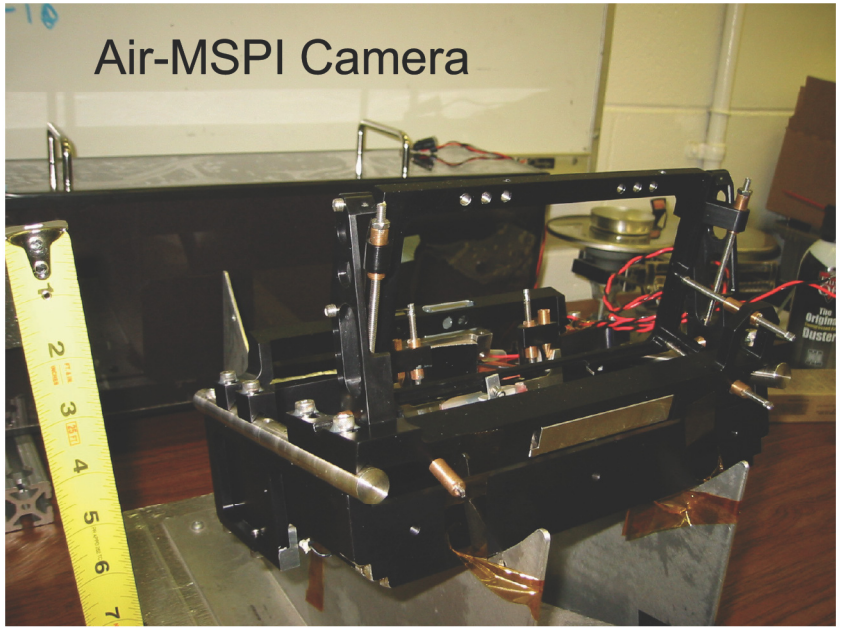
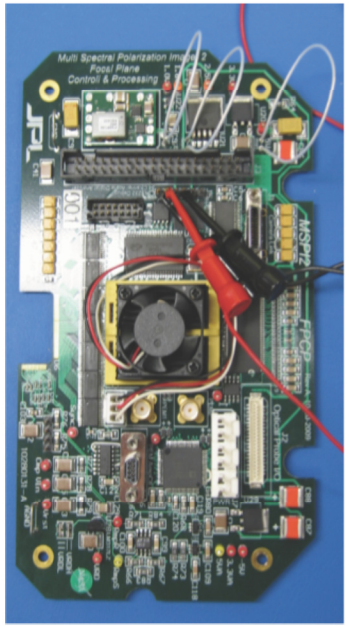
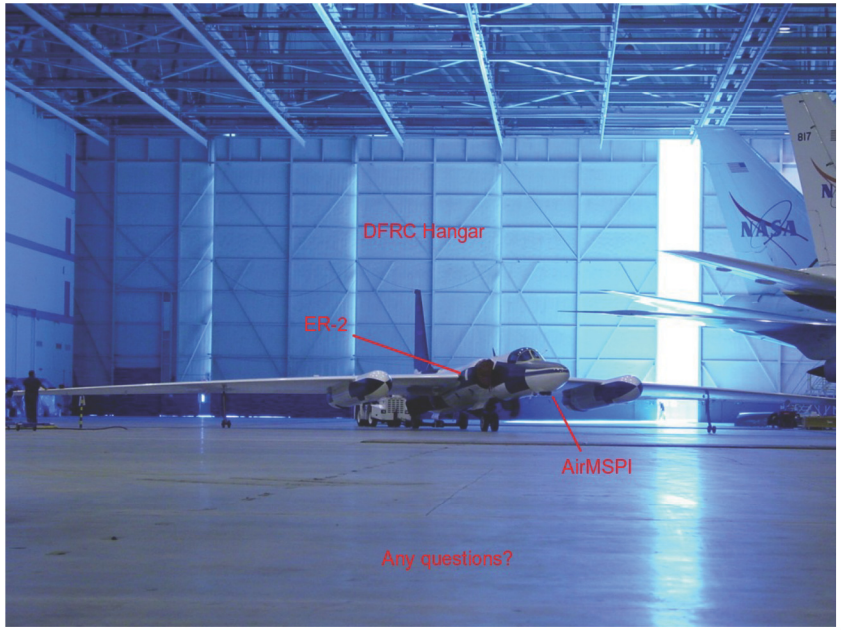
Motivation for COVE

MSPI: Multi-angle SpectroPolarimetric Imager

- Measures cloud and aerosol properties
- 8-fixed and 1-gimballed cameras, each with 16 channels
- A single MSPI camera must process 95 Mbytes/sec of raw video data; data reduction to 0.45 Mbytes/sec is required





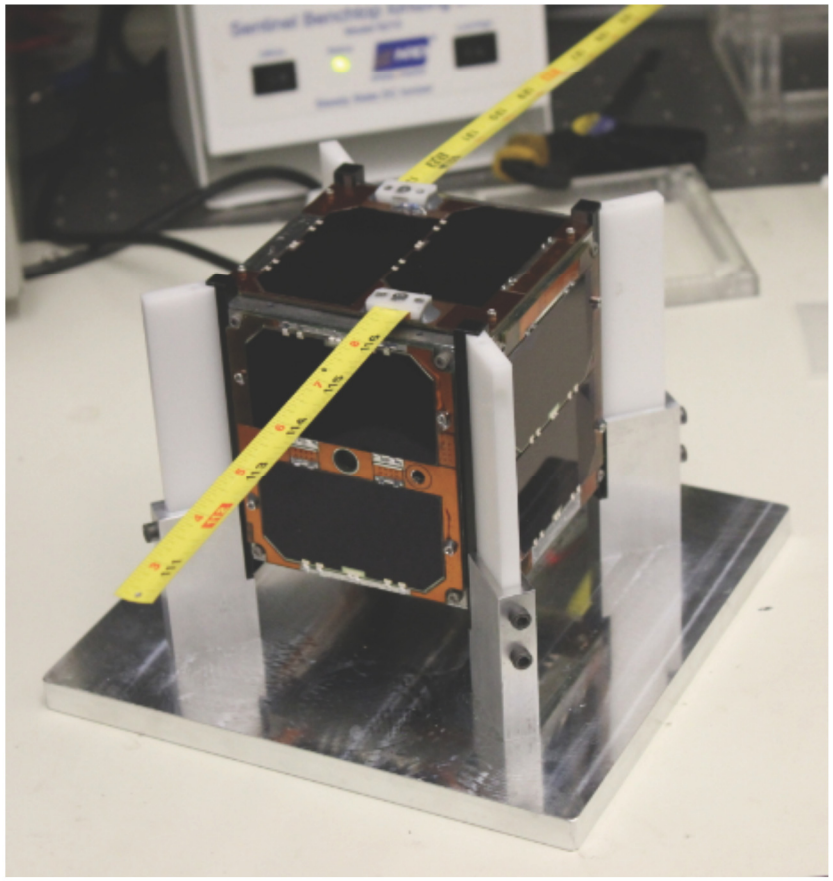


The information technology processing challenge is to apply on-board processing to extract intensity and polarimetric parameters from the real-time data stream across each camera thereby reducing the data volume by 2-orders of magnitude without loss of science information.

JPL/U. Michigan Collaboration

M-Cubed/COVE OBJECTIVES:

- Raise TRL of ESTO Technologies relevant to the Earth Science Decadal Survey Missions
  - MSPI On-Board Processing (OBP) algorithm
  - Xilinx Virtex-5QV Single event Immune Reconfigurable FPGA (SIRF)
- Capture and downlink mid-resolution images of the Earth
- Educate and train the next generation of engineers in the Aerospace Industry



M-Cubed CubeSat Flight Model
Image Courtesy of U. Michigan

SmallSat platforms can rapidly advance the TRL of key instrument components and serve as platforms for new science observations

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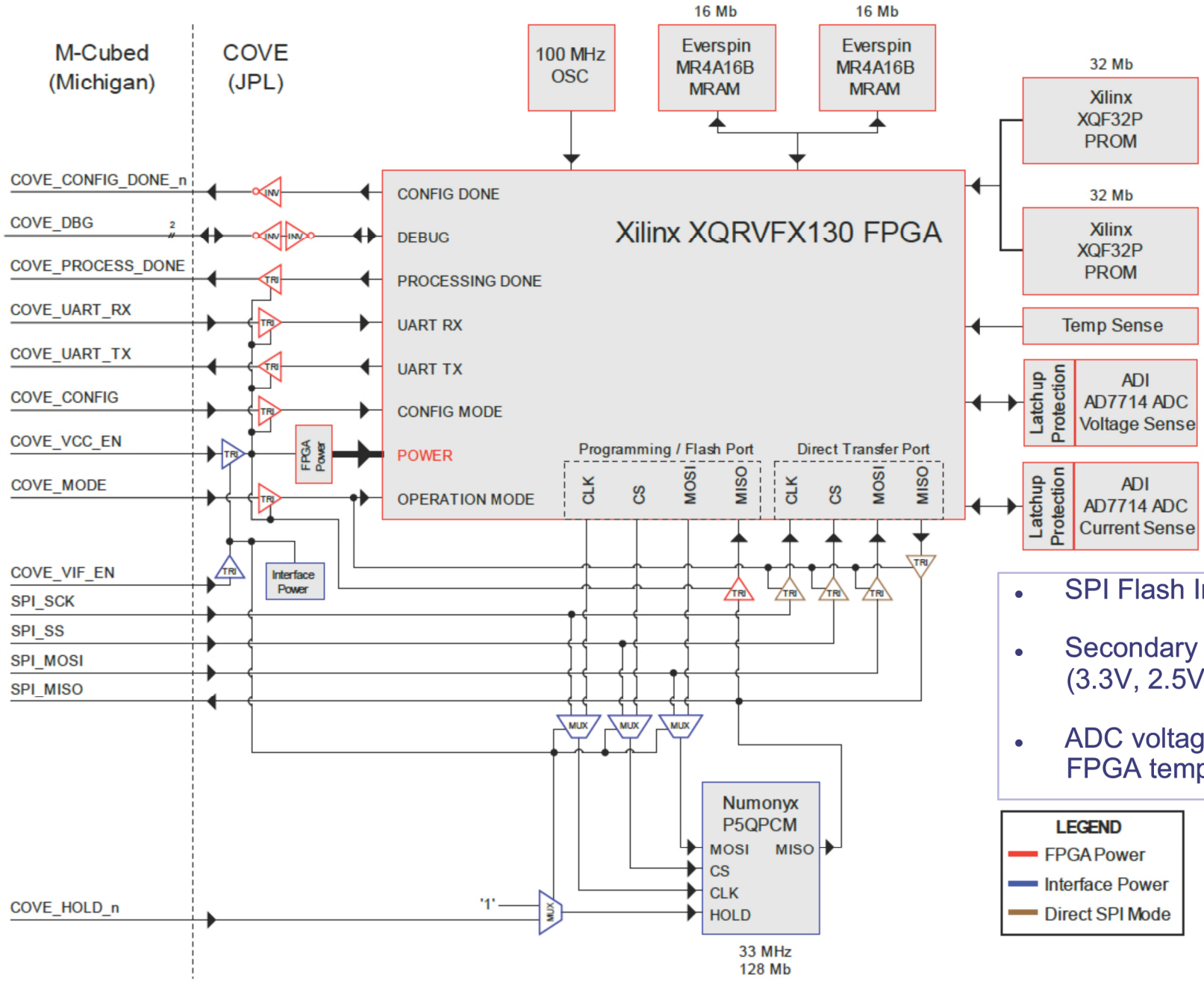
COVE Payload Processor

High-Level Block Diagram

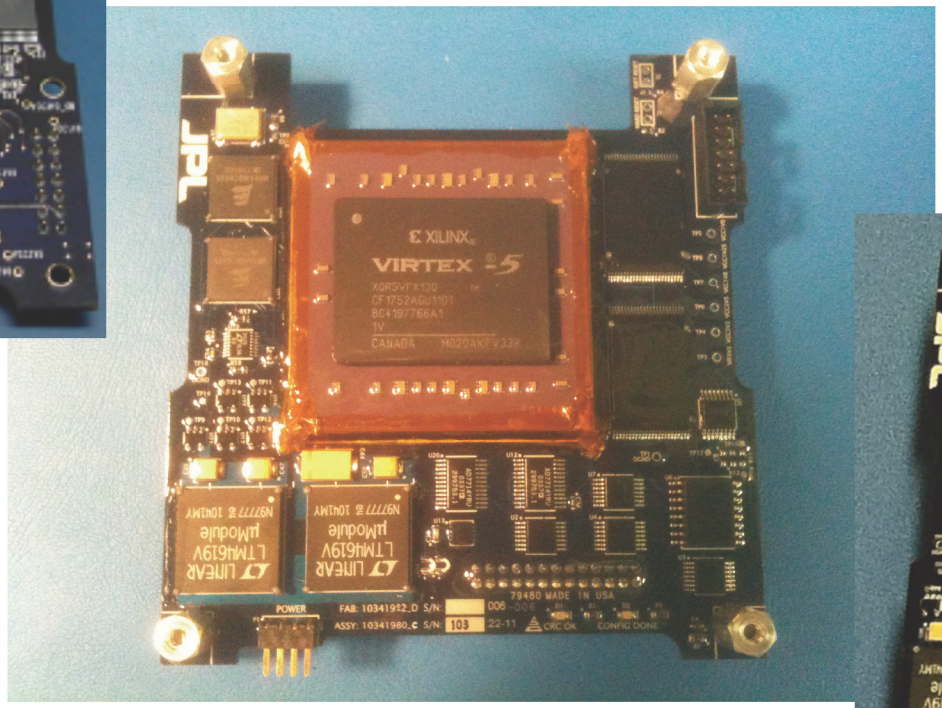


- SPI Flash Interface
- Secondary voltage regulation (3.3V, 2.5V, 1.8V, 1.25V, 1.0V)
- ADC voltage and current sense; FPGA temp sense

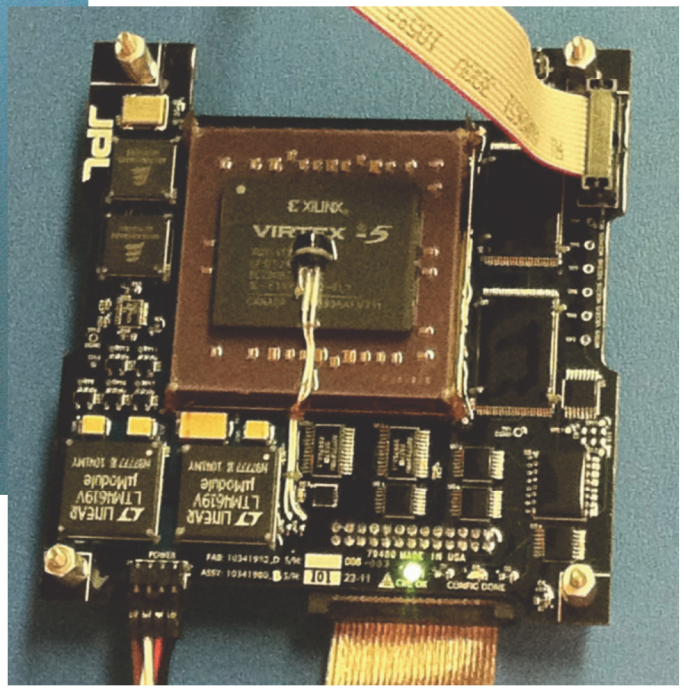
LEGEND
- FPGA Power
- Interface Power
- Direct SPI Mode

COVE Development Stages

Engineering Model
(Commercial Virtex-5)



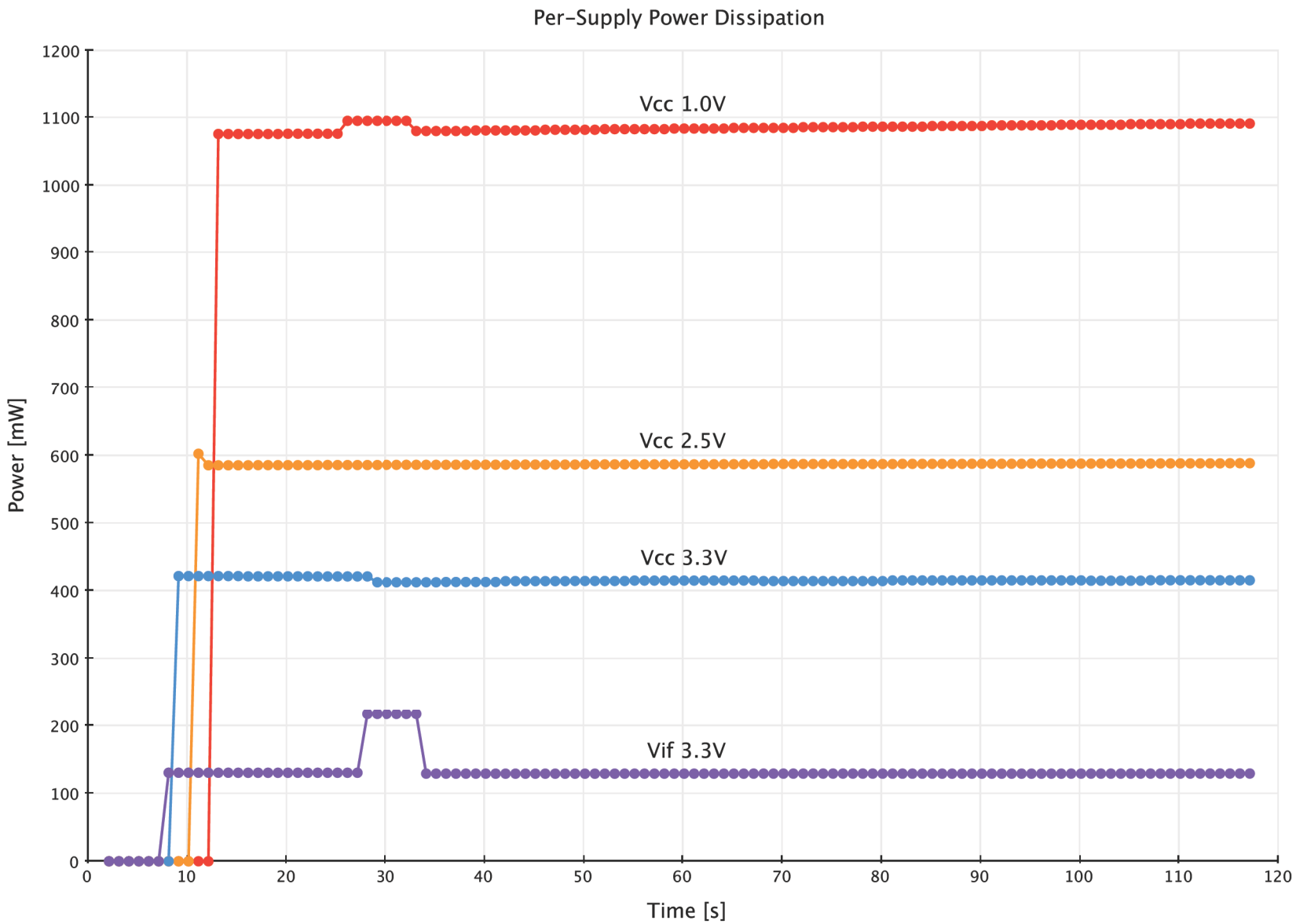
Flight Model
(V5QV Production SIRF)



Flight Spare
(V5QV Engineering Sample SIRF)

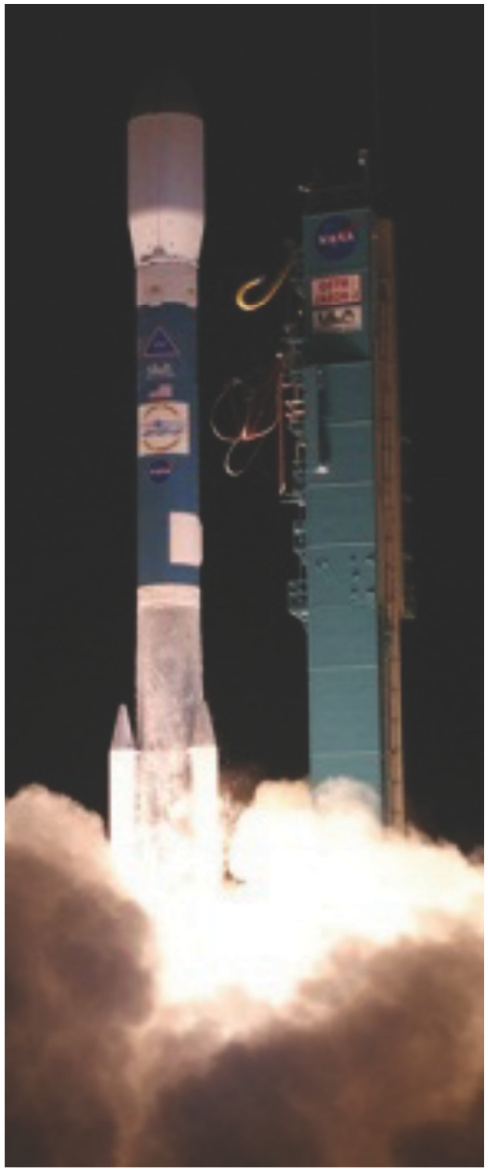
Press Release: Xilinx Space-Grade Virtex-5QV FPGA in Production with Mega-Rad Capability (July 21, 2011)

Operational Housekeeping



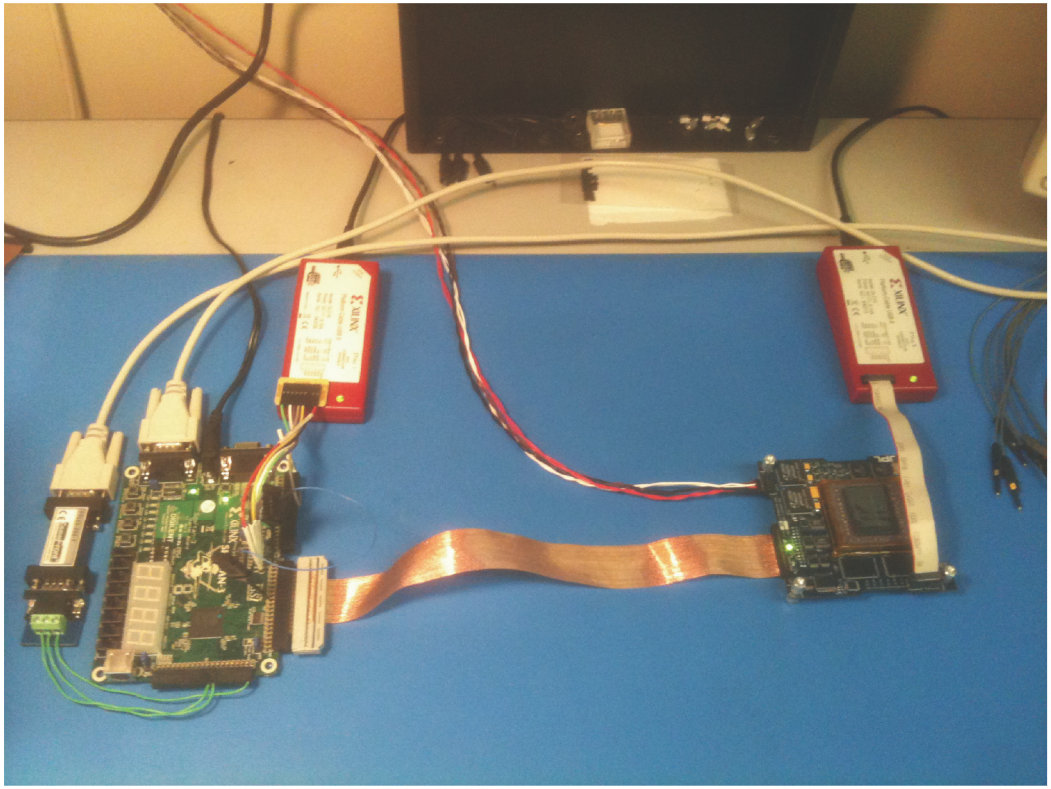
Final Stages

- COVE FM Payload (V5QV SIRF) delivered to U. Michigan, July 27
- M-Cubed/COVE Integration
- M-Cubed Vibration, Thermal & Shock Tests
- Deliver to Cal Poly, San Luis Obispo, Aug. 22
- P-Pod Integration
- Launch via NASA Space Operations Mission Directorate (SOMD) CubeSat Launch Initiative
  - NPP Mission (as a secondary payload)
  - VAFB on Oct. 26, 2011



Any Interest?

- An M-Cubed/COVE OBJECTIVE: Educate and train the next generation of engineers in the Aerospace Industry
- NASA/JPL is targeting the Virtex-5QV SIRF to meet demanding on-board processing requirements for future space science instruments



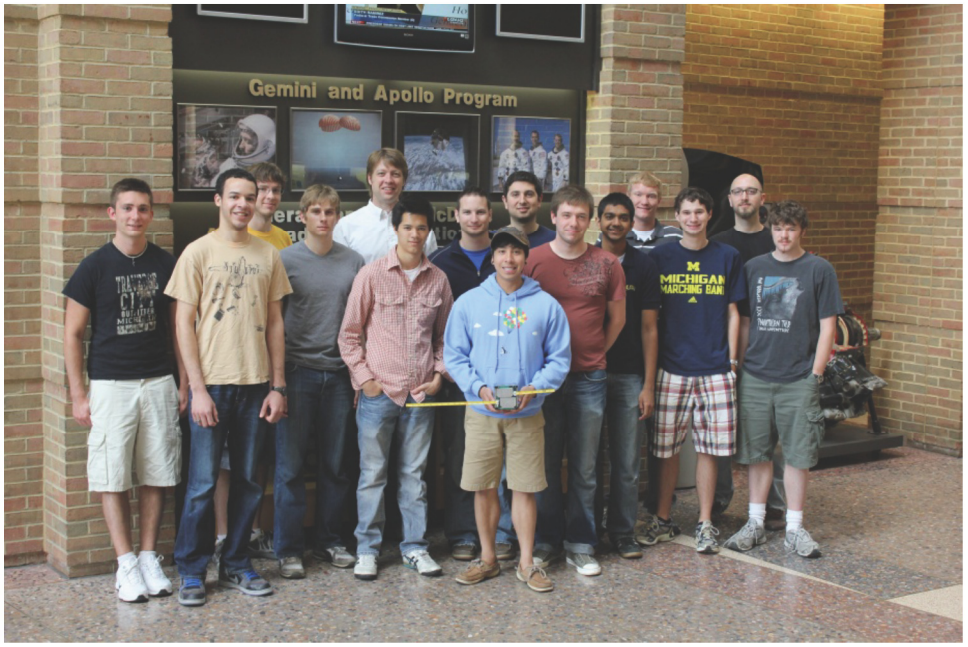
Fly the COVE Payload Processor
(with Commercial-grade Virtex-5 FPGA)
on your next CubeSat

Learn FPGA development and demonstrate your application in space!

Acknowledgments

JPL COVE Payload Team

U. Michigan M-Cubed Team



The research described in this presentation was carried out at the Jet Propulsion Laboratory, California Institute of Technology, under contract with the National Aeronautics and Space Administration

Sponsored by NASA/Earth Science Technology Office (ESTO)

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