Implementation of a Digital Signal Processing Subsystem for a Long Wavelength Array Station

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Abstract—This paper describes the implementation of a Digital Signal Processing (DP) subsystem for a single Long Wavelength Array (LWA) station.[1][2] The LWA is a radio telescope that will consist of many phased array stations. Each LWA station consists of 256 pairs of dipole-like antennas operating over the 10-88 MHz frequency range. The Digital Signal Processing subsystem digitizes up to 260 dual-polarization signals at 196 MHz from the LWA Analog Receiver, adjusts the delay and amplitude of each signal, and forms four independent beams. Coarse delay is implemented using a first-in-first-out buffer and fine delay is implemented using a finite impulse response filter. Amplitude adjustment and polarization corrections are implemented using a 2x2 matrix multiplication.

Each beam has a digital receiver which can select two independent sub-bands, with bandwidths adjustable from 25 KHz to 19.6 MHz. The sub-bands are processed by a filterbank into 4096 frequency channels and sent as Ethernet packets via a 10 Gigabit Ethernet link to the LWA Data Recorder subsystem for to the Data Recorder subsystem for later analysis. The DP subsystem also provides two transient buffer capabilities, a Transient Wideband Buffer (TBW) and a Transient Narrowband Buffer (TBN). The TBW captures the raw output of each analog-to-digital (A/D) converter, sampled at 196 MHz for about ~50 msec at a time. The TBN allows for continuous capture of the raw A/D output at a particular center frequency for bandwidths of 1 kHz to 100 kHz.

The DP subsystem interfaces with the LWA Analog Receiver, Monitor and Control, and Data Recorder subsystems. Command and control of the DP subsystem is achieved through communication with the Monitor and Control subsystem via Ethernet. The DP subsystem software provides commands to configure the TBW, TBN, the digital receivers, and beams. A command is also provided to configure individual filter coefficients.

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1. INTRODUCTION

The Long Wavelength Array (LWA) is a radio telescope that will consist of 53 receiving stations located throughout southwest New Mexico [1] and operating in the frequency range 10 to 88 MHz. About 15 of the stations will form a compact core in a log-spiral design [2]. Key science drivers for the LWA include the study of cosmic evolution and the high redshift universe, acceleration of relativistic particles, plasma physics (including the Earth's ionosphere) and space science, and exploration science [3]. Other low frequency radio astronomy arrays nearing completion or under construction include the Low Frequency Array (LOFAR) [10], the Murchison Wide Field Array (MWA) [15], and the Precision Array Probing the Epoch of Reionization (PAPER) [16]. Of these, only LOFAR covers frequencies below 70 MHz, and its collecting area is substantially less than that of the LWA. Much larger arrays are proposed, including the Square Kilometer Array [11] and the Lunar Radio Array [17].

The overall range of baseline lengths will be 200 m to 400 km. Signals from the stations will be combined by cross-correlating all pairs at a central facility, allowing detailed images of the sky to be formed. When completed, the LWA will provide unprecedented effective aperture and thus sensitivity, as well as unprecedented angular resolution, in its frequency range.

Each station is a phased array of 256 pairs of dipole-like elements. The elements are distributed in a pseudo-random manner within a circle of approximately 100 m diameter, giving a beam width of 2° at 80 MHz [3, 4]. The element gain at zenith is approximately 5 dB [12], which leads to an effective area for each station that varies from approximately 6400 m^2 at 30 MHz to 750 m^2 at 88 MHz,

and thus the entire 53-station array provides about 340,000 m^2 to 40,000 m^2, respectively.

Figure 1- LWA-1, August 2010

Signals from the elements are combined locally so as to form four beams simultaneously, each rapidly and independently steerable to any direction in the sky. The beamformers are broad-band, covering the entire 10 to 88 MHz RF range. A portion of each combined signal is then selected for further processing. Bandwidths of 250 kHz to 19.6 MHz are available, independently tunable across the RF range.

The Earth's ionosphere is a major impediment to low-frequency radio astronomy, and the challenges increase as frequency is reduced. It is necessary to track and correct for the ionospheric signal delay as a function of direction. To accomplish this, one beam of the LWA will normally be devoted to calibration. There are engineering challenges as well, including making simple and low-cost antennas which are efficient over a large fractional frequency range; providing signal processing electronics with sufficient flexibility at an affordable cost; and transmitting the signals to the central correlator.

At present, the first LWA station ("LWA-1") is under construction. It is located near the core of the National Radio Astronomy Observatory's Expanded Very Large Array (EVLA) [8]. All of the antennas have been installed, and a significant portion of the electronics, including the initial modules of the hardware and software described here, is in operation.

This paper is organized as follows: In Section 2, the overall system is described. In Section 3, details of the digital signal processing (DP) design are presented. Section 4 describes the implementation of the DP. In Section 5, some early test results are presented. Finally, in Section 6, conclusions are reached.

2. System Description

Each LWA station includes several subsystems which work together to form beams from its antenna array as shown in Figure 2. The array (ARR) subsystem includes the antennas and associated front-end electronics, as well as the RF and power distribution. The antenna signals travel into the shelter subsystem through the shelter entry panel. The shelter subsystem also provides power and conditioning to the other subsystems. Once inside the shelter, the analog input signals are amplified and filtered by the Analog Signal Processor (ASP) subsystem's Analog Receiver (ARX). Each signal is digitized by the Digital Signal Processing (DP) subsystem, which forms beams and sends data in packetized form to the Data Aggregation and Communication (DAC) subsystem. Command and control of the station is accomplished by the Monitor and Control subsystem (MCS). The DAC subsystem will not be needed until multiple stations and the central correlator are available, and as of this writing, has not been implemented. Therefore, the DAC is not shown in Fig. 1. Instead, data is recorded by the Data Recorder subsystem (DR). The Timebase and Clock Distribution (TCD) subsystem provides time information to other subsystems, including a 1 Hz and a 10 MHz clock [6].

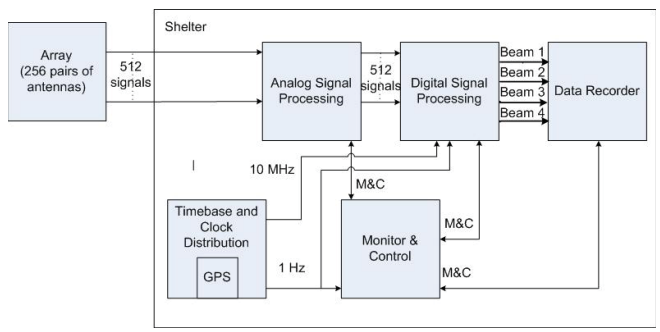

Figure 2- LWA station subsystem architecture

The DP subsystem digitizes the dual polarization signals at 196 MHz, adjusts the delay and amplitude of each signal, and forms four independent beams over the full 10 to 88 MHz band. Each beam has a digital receiver which can select two independent sub-bands. The sub-bands are processed by a filter bank into 4096 frequency channels and the data is sent to the Data Recorder subsystem for later analysis. The DP subsystem also provides two separate outputs intended to support detection of transient signals, known as the transient wideband buffer (TBW) and a transient narrowband buffer (TBN). These buffers are described in more detail below. The MCS subsystem monitors and controls the DP and other subsystems via 1 Gigabit Ethernet links [14].

3. DIGITAL PROCESSING SUBSYSTEM: ARCHITECTURE

Key design considerations of the DP subsystem include modularity, expandability, and cost-effectiveness. A modular design allows individual submodules of the DP subsystem to be designed and tested individually. It is desirable for the system to be expandable so that the design may be implemented, validated, and utilized to obtain useful scientific results at LWA-1 and duplicated as additional stations are constructed. Cost effectiveness is crucial in enabling implementation of the system with available funding.

The system must also be able to meet the LWA timing requirements. An observation is defined as all parameters that define a beam, including the center frequency, bandwidth, delays, and gains. The time between the beginning of one observation and the beginning of the next observation is required to be 55 ms or less. A short minimum observation duration allows calibration of the system to be accomplished more quickly. Other requirements include the ability to schedule events with a time resolution of 50 ms, sample timing accuracy of 709 ps, and the capability to initiate 106 observations per second [4]. Another important consideration is the minimization of board-level interconnections.

The digital processing subsystem architecture for a pair of dual polarization signals is shown in the block diagram in Figure 3. The signals are digitized at 196 MHz and 12 bit resolution by a pair of analog-to-digital converters. The samples are distributed to four beam forming units (BFU), a TBW unit, and two TBN units [6].

The beam forming units adjust the delay and amplitude of the signals to form four beams. Each beam forming unit adds the processed samples to the partial sums from the previous antenna pair, outputting a new partial sum. The final sums are sent to four digital receivers (DRX). Each digital receiver provides two independent sub-bands with user-selectable center frequency and bandwidth. There are 256 identical processing units, one for each antenna pair, the last of which is shown. Beams are formed by passing partial sums from one unit to the next. The final sums are further processed by Digital Receivers.

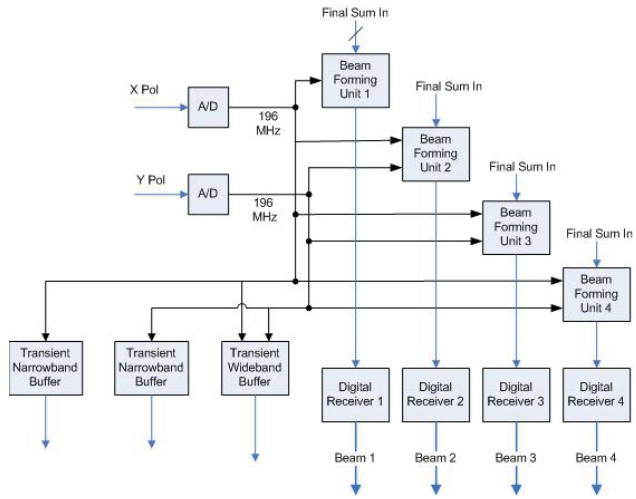

Figure 3- Digital Processing Subsystem block diagram

The transient wideband buffer consists of a memory that can be filled with raw data samples from all antennas upon receipt of a trigger signal from the monitor-control subsystem. A 32-MB RAM module is provided for each of the 2x256 signals, enough for 57 ms of recording. This data is then packetized and transmitted more slowly to the data recording subsystem. Each transient narrowband buffer unit consists of a digital down converter and filters that decimate the samples to a specified center frequency and bandwidth.

Beamforming— Each pair of signals is distributed to four beam forming units, which adjust the delay and amplitude of the signals and adds them to the results from the previous antenna pair, so that in the end we have the delayed and weighted sum of all signals for each polarization. A block diagram of a beam forming unit is shown in Figure 4. The delays are programmed so that a signal from the desired beam direction is time-aligned among all antennas, compensating for geometrical and cable delays. Coarse delay to the nearest sample is implemented using a first-in-first-out buffer. Fine fractional-sample delay is implemented using a finite impulse response (FIR) interpolation filter [5]. Each pair of signals is then multiplied by a 2 x 2 matrix. This provides programmable amplitude weighting for beamforming and also allows correction of any misalignment of polarization among the antennas.

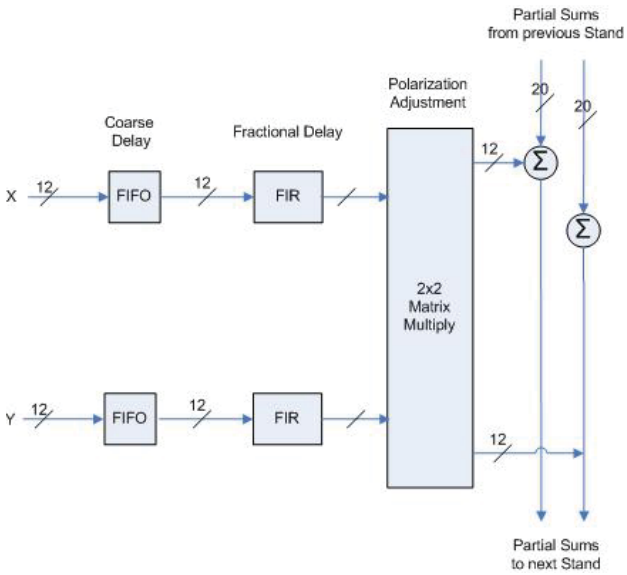

Figure 4- Beam forming unit block diagram

Digital Receivers— The summed signals from each beam are processed by a digital receiver. A block diagram of the digital receiver submodule is shown in Figure 5. Each includes two quadrature down-converters with independently selectable center frequency between 10-88 MHz and bandwidth from 25 kHz to 19.6 MHz. Each uses a two stage low pass filter, where the first stage is a cascaded integrator-comb (CIC) filter [18] and the second stage is a FIR filter . The sub-bands thus selected are then broken into 4096 narrow-band channels by a uniform filter bank. Each frequency channel sample is 8 bits of complex data (4 bits I, 4 bits Q). These samples are packed into Ethernet frames and sent to the Data Recorder subsystem via a 10 Gigabit Ethernet link. Each frame contains 4096 frequency channel samples for a particular time (and therefore 4096 bytes of data) .

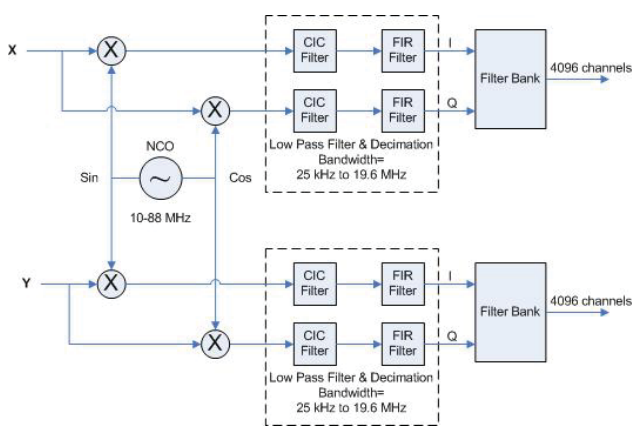

Figure 5- Digital receiver block diagram

Transient Wideband Buffer— Each pair of signals from an antenna has a Transient Wideband Buffer submodule that can capture the raw output of each ADC. Each TBW can record up to 12,000,000 samples of 12 bit data to a 32 MB RAM. When the buffer is full, its contents are read out and formatted into UDP packets and sent to the Data Recorder subsystem via a 1 Gigabit Ethernet link. Each packet contains data from a particular antenna and both polarizations (X and Y). The packets include a header with the antenna number and time tag. Each packet contains 1200 bytes of data (400 samples of 12 bit data for each of the two polarizations). Although the TBW modules for the various antenna pairs are physically separate, they are synchronized under software control so that data from all antennas is captured simultaneously.

Transient Narrowband Buffer— Each pair of signals has a Transient Narrowband Buffer submodule, where the signal is digitally down converted, filtered using a two stage low pass filter, and decimated to the specified reduced Nyquist frequency. A block diagram of a transient narrowband submodule is shown in Figure 6. Each submodule contains two downconverter/filter circuits, with independently settable center frequency and bandwidth. The first stage of each circuit is a CIC filter and the second stage is a FIR filter. The center frequency is specified by the user and has a range of 10-88 MHz. The bandwidth is also specified by the user and has possible values of 1 kHz, 3.125 kHz, 6.250 kHz, 12.50 kHz, 25.0 kHz, 50 kHz, or 100 kHz. This bandwidth reduction allows for continuous capture of the raw ADC output. TBN data is 16 bits (8 bits each, I & Q). The data is formatted as UDP packets and sent to the Data Recorder subsystem via the same 1 Gigabit Ethernet link as TBW. Each packet contains data from a particular antenna and polarization. The packets include a header with the antenna number and time tag. Each packet contains 500 samples or 1000 bytes of data . Although the TBN modules are physically separate for each antenna pair, software ensures that all are set to the same center frequency and bandwidth.

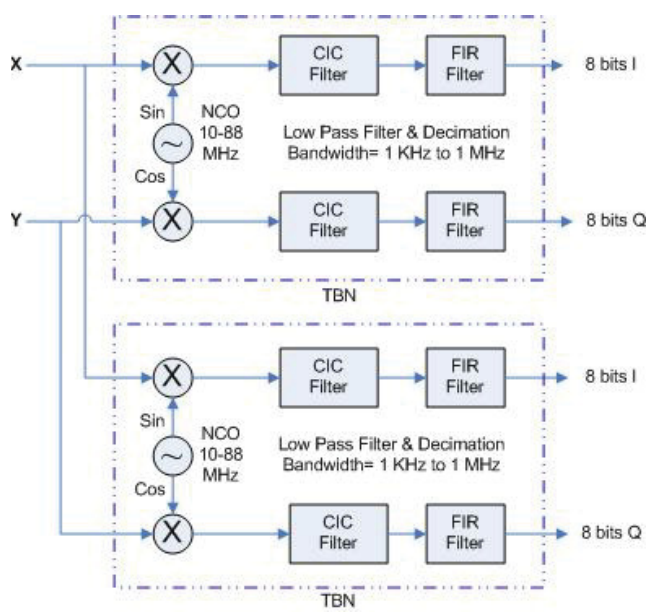

Figure 6- Transient narrowband buffer block diagram

4. DIGITAL PROCESSING SUBSYSTEM: IMPLEMENTATION

The DP subsystem is implemented using custom printed circuit boards: a Digitizer board which digitizes the signals and a Processor board which performs signal processing, arranged as shown in Figure 7. The Processor board includes 5 Xilinx Virtex-5 Field-programmable gate arrays (FPGA). This is sufficient to provide beamformer, TBW and TBN modules for 10 antennas (20 signals). All processing for a signal pair is kept together in order to minimize board-level interconnections. Each Processor board mates with a Digitizer board, which carries the corresponding 20 analog-to-digital converters. Thus, 26 of these board pairs are needed to implement the 256-antenna system.

An advantage of using FPGAs is that they may be reprogrammed to allow the Processor boards to have different capabilities. Two additional Processor boards are used to implement the four Digital Receiver modules. These boards are identical to the 26 that are used for the antenna-by-antenna processing except for programming.

The DP subsystem is housed in two 14-slot commercially available Advanced Telecom Computing Architecture (ATCA) chassis with high speed backplanes. Each Processor board has a 1-Gigabit Ethernet link to the 1/10 Gigabit Ethernet switch that is used to communicate with the DP subsystem computer for monitor and control and to send the TBW and TBN data. Each chassis contains 13 Digitizer boards, connected to 13 Processor boards, each of which handles 10 pairs of signals. The partial sums are daisy chained together via the ATCA backplane for each chassis, and via cables to the other chassis. The final sums are routed to another Processor board in each chassis; each of those boards provides two of the Digital Receivers. Each dual-polarization beam is sent from the latter boards to the Data Recorder subsystem via a 10 Gigabit Ethernet link [5].

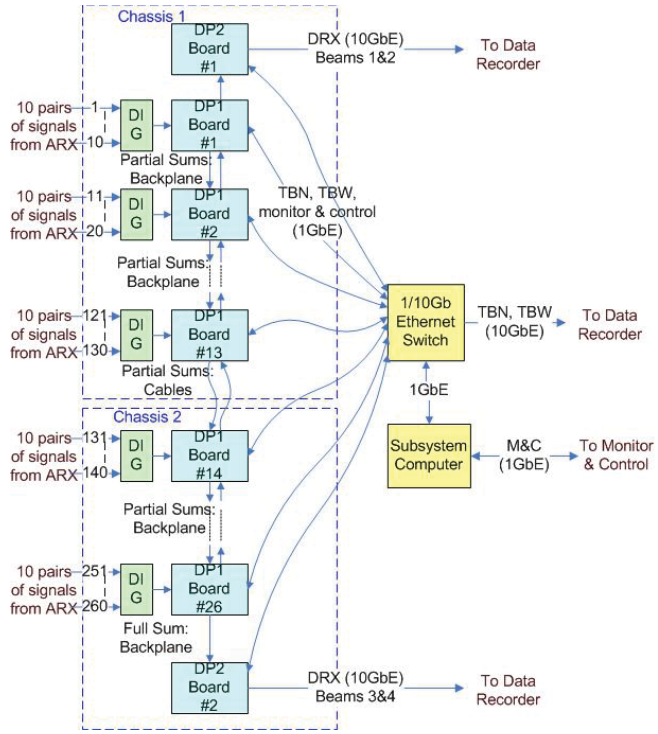

Figure 7- DP Subsystem Block Diagram

Clock Synthesizer Board— The DP subsystem's clock synthesizer box accepts as inputs 10 MHz and 1 Hz clocks from the Timebase and Clock Distribution (TCD) subsystem. The connection between the TCD subsystem and the DP subsystem consists of one Category 7 cable. This cable has four individually shielded pairs, two of which are used A phase locked loop and voltage controlled crystal oscillator are used to generate the 196-MHz sampling clock that is phase locked to the 10-MHz and 1-Hz signals. The 196-MHz and 1-Hz clocks are copied 28 times using distribution buffers. Each pair of output signals is provided to a Digitizer board, which passes these clocks to a Processor board Clock distribution is shown in Figure 8.

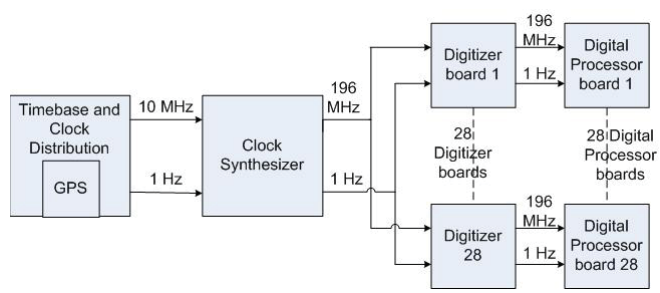

Figure 8- Clock distribution block diagram

Digitizer Board— The Digitizer boards are custom printed circuit boards with 16 layers. The Digitizer boards sample signals from the ASP's Analog Receiver (ARX) at a clock rate of 196 MHz with 12-bit resolution, using Analog Devices AD9230 analog-to-digital converters (ADC). The connection between the ASP and the Digitizer boards consists of 130 Category 7 cables. Each cable includes four individually shielded twisted copper wire pairs which are used for differential signals from both polarizations of two pairs of signals [12]. Shielded RJ-45 connectors are used for each cable. Each Digitizer board digitizes 10 pairs of signals. The analog signals from the ASP are sent over differential pairs using Category 7 cables. Five of these cables provide the 20 input signals to a Digitizer board. The Digitizer output data is distributed to the TBW, TBN, and BFU submodules on the Processor board. Gray code data format is used for the ADC output [5].

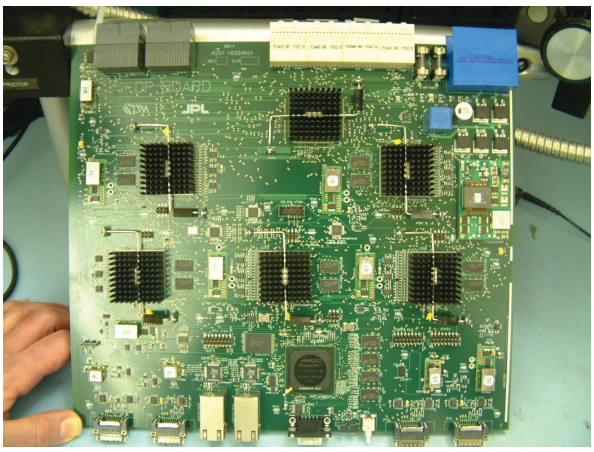

Figure 9- Digital Processing Board

Digital Processing Board— The Processor boards are custom printed circuit boards with 20 layers. A digital processing board is shown in Figure 9. Each Processor board connects to a Digitizer board via two HM-Zd high speed differential connectors. Each Processor board includes a PPC440EPx embedded processor, a MirrorBit 512-MB flash memory, five Xilinx Virtex-5 XC5VSX50T FPGAs, ten 32-MB RAM modules, two Vitesse Gigabit Ethernet physical interface chips, and four 10-Gigabit Ethernet CX4 connectors. The PPC440EPx utilizes a processor speed of 533 MHz, has a built-in Floating Point Unit and interfaces with the FPGAs for monitor and control using the External Bus Controller (EBC). The flash memory is loaded with a custom version of the open source U-Boot bootloader. For the Processor board, each FPGA processes data from two pairs of signals, so each DP1 board is capable of processing a total of 10 pairs of signals. Each FPGA has multi-gigabit transceivers which connect to the ATCA backplane to implement the partial sum daisy chain for the beam forming units. The Transient Wideband Buffer records data from each pair of signals to a 32-MB RAM module. Each board's TBW and TBN data is sent as UDP packets across one of the 1-Gigabit Ethernet interfaces to the DP subsystem switch.

Embedded Software— The Processor boards utilize the Debian Linux operating system, which is hosted by the DP subsystem computer. When a Processor board is first powered on, the U-boot bootloader that is in its flash memory downloads a custom version of the Debian Linux DENX kernel from the DP subsystem computer. Each Processor board's file system is also provided by the DP subsystem computer and accessed using Network File System. Several Linux device drivers provide an interface for the software to the Processor board hardware. These device drivers are designed to be modular. The EBC device driver configures the EBC bank parameters and allows the embedded processor to communicate with the Xilinx FPGAs as memory mapped devices. The general purpose input/output (GPIO) device driver provides read/write access to the embedded processor's GPIO pins. The I2C device driver provides read/write access to any device on I2C bus, including an I2C to Serial Peripheral Interface (SPI) converter chip that is used to implement the interface between each Processor board and Digitizer board.

5. RESULTS

As of December 2010, all 256 antennas have been installed at LWA-1. One Digitizer board digitizes dual-polarization signals from 10 antennas and provides this data to one Processor board. The transient wideband buffer and transient narrowband buffer capabilities have been implemented.

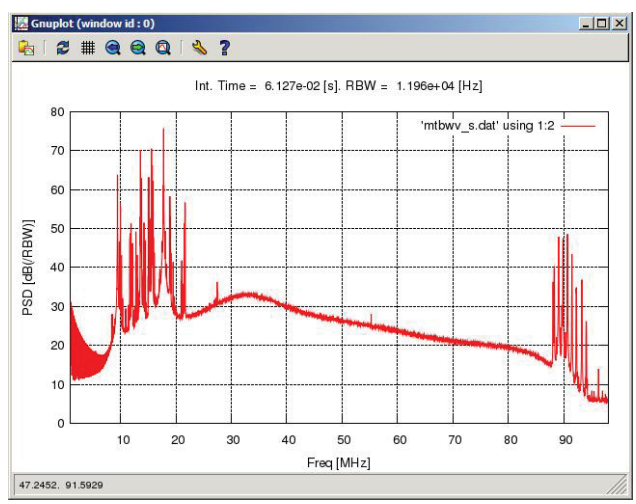

Figure 10- Frequency vs power spectral density of 12,000,000 samples of 12-bit TBW data of a sky signal

The plot shown in Figure 10 illustrates the power spectral density computed from 12,000,000 samples of 12-bit TBW data of an sky signal from a single antenna, single polarization. Recording time was 12,000,000/196 MHz = 0.0612 seconds. The Fast Fourier Transform uses 16384

samples per block, so resolution bandwidth is 196 MHz / 16384 = 11.96 kHz. At frequencies above 88 MHz, signals from FM broadcast stations are seen. The LWA will restrict its upper frequency limit to <88 MHz to avoid these signals. From 10 to 20 MHz, signals from various service providers are seen, as well as reflection and absorption due to the ionosphere [13].

Figure 11 is a plot of the theoretical and measured magnitude response of a TBN channel using a bandwidth and output sample rate of 100 kHz. The complex passband is symmetrical about zero frequency, with a Nyquist range of -50 kHz to +50 kHz. The 3 dB bandwidth is 2/3 of the sample rate. The filter suppresses signals outside the Nyquist band by at least 40 dB.

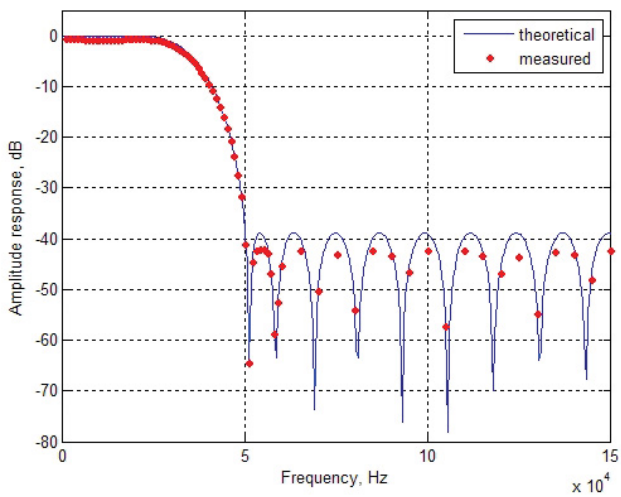

Figure 11- Magnitude response of TBN filter

6. CONCLUSION

We have described the design of a signal processing system for an LWA station. Although this is only one station of the full array, its 256 dual-polarization elements make it a large-number-of-antennas ("large N") telescope by current standards. The processing system provides beamforming for four independent, rapidly-steerable beams. It also provides narrow-bandwidth continuous streaming outputs for all element signals, and full bandwidth (10 to 88 MHz) capturing of short segments of all element signals. The architecture was chosen to make efficient use of available technologies, including modern FPGAs and high-speed backplanes, so as to minimize interconnections. The result is a compact and cost-efficient implementation.

7. ACKNOWLEDGEMENTS

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The LWA is being developed by a consortium of institutions including the University of New Mexico, Naval Research Laboratory, University of Iowa, Virginia Tech, and Los Alamos National Laboratory, and JPL. Many scientists have been involved in establishing its concept and specifications (e.g., [3-7]). Steve Ellingson of Virginia Tech has designed many parts of the LWA, and in particular he is responsible for the Monitor and Control subsystem and the Data Recorder subsystem, both of which connect to the Digital Signal Processing subsystem described here; we are grateful for his collaboration on those interfaces [14]. Joseph Craig of the University of New Mexico has designed the Analog Signal Processing subsystem and has also been responsible for much of the system-level design (e.g., [6]); we are grateful for his collaboration as well. Direct support of our work by Gregory Taylor and Lee J. Rickard of the University of New Mexico is also gratefully acknowledged.

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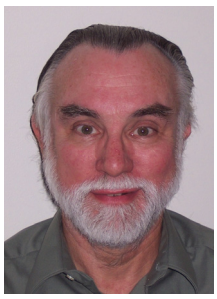
BIOGRAPHY

Melissa Soriano *is a staff software engineer in the Tracking Systems and Applications Section at the Jet Propulsion Laboratory. She has developed real-time software for the Long Wavelength Array, NASA's Breadboard Array, and the Wideband VLBI Science Receiver used in the Deep Space Network. Melissa also developed software to implement a Near Real-time Altimeter Validation System for the Ocean Surface Topography Mission. She has a BS from Caltech, double major in Electrical and Computer Engineering and Business Economics and Management. She also has an MS from George Mason University.*

Robert Navarro *has been with JPL since 1991. He has worked on DSN and ground systems for radio science and VLBI recording as well as correlators and antenna arrays as an engineer and a manager. He is the supervisor of the Processor Systems Development Group. Robert received a B.Sc in Eingeering from Harvey Mudd College in 1986 and an M.Sc in Electrical Engineering from the University of Southern California in 1987.*



Larry R. D'Addario *received the B.S. degree from the Massachusetts Institute of Technology, Cambridge, in 1968 and the M.S. and Ph.D. degrees from Stanford University, Stanford, CA, in 1969 and 1974, respectively, all in electrical engineering. At Stanford, his thesis work was connected with the development of a five-element synthesis radio telescope and its use in astronomical observations of ionized hydrogen regions and Jupiter. He subsequently joined the National Radio Astronomy observatory, where he worked from 1974 through 2004 on a wide variety of projects, including assisting in the development of the VLA, VLBA, GBT, and ALMA radio telescopes. He also contributed to the early development of SIS mixer technology for millimeter wavelength receivers. From 1989 through 1995, he led the design and construction of an Earth station to support orbiting radio telescopes for VLBI; the station was successfully used with the Japanese VSOP mission. Since 2004, he has been with the Jet Propulsion Laboratory, where he has worked on improving communication with spacecraft in deep space, including development of transmitting arrays for possible use in the Deep Space Network and the modernization of transponders for use on spacecraft; on instruments to measure fluctuations in microwave delay through the troposphere; and on digital signal processing for large radio telescopes arrays like the future Square Kilometer Array.*

Elliott Sigman *has a Ph.D. in Electrical Engineering from University of Michigan. A former professor at Harvey Mudd College, he has been at the Jet Propulsion Laboratory for 30 years. He is accomplished in many areas of electronic design including RF, analog, high speed digital, A/D conversion, high speed ECL circuitry, FPGA design, high speed printed circuit board design, and digital signal processing design. He has done top level system design along with the detailed circuit design, printed circuit board design, firmware design, and software code generation for phase calibration systems, and deep space probe receivers which have been in use in JPL's Deep Space Network for over 15 years.*

Douglas Wang *is a senior hardware design engineer. He developed many electronic components for flight control computers, autonomous landing guidance, millimeter wave radar, cell phone GPS receiver, and the MSL rover power analog module. He has a BSEE from Cal Poly Pomona and a master's degree from USC.*