Status on Radiation Qualification Methods for SOC Devices

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• Eurotech Adbc7517
  – Freescale P4080 with 8 e500 cores, ~30W, 1.5GHz
  – On-chip XAUI, SGMII, PCIe, RapidIO, SD/MMC, etc... (not all supported by the card)
Outline

• What we’re talking about – what SOCs?
• Why it’s needed?
• What we are trying to do –
  – Develop qualification approach
  – Develop test methods
• What work has been done?
• Findings thus far...
Computer Trends

• System on a Chip Trends:
  – Wikipedia: “... System on a chip is hyperbole, indicating technical direction more than reality: increasing chip integration to reduce manufacturing cost and to enable smaller systems.”
  – Most microprocessor manufacturers are moving towards multicore devices necessitating on-chip support such as coherency and standard buses

• Space Trends
  – Increasing Fault Tolerance
  – More RHBD offerings, such as Maestro
  – Use of commercial/embedded SOCs in redundant configurations
  – Embrace SOCs due to close ties to embedded market
A couple examples...

- Freescale MPC8641D
  - P2020
  - P4080
  - ...

MPC8641D Block Diagram

1 MB L2 Cache
1 MB L2 Cache

e600 Core

e600 Core

32 KB L1 i-Cache
32 KB L1 i-Cache

32 KB L1 D-Cache
32 KB L1 D-Cache

MPX Coherency Module

System Bus

4 x Gigabit Ethernet

On-Chip Network

PCI Express
PCI Express
Serial RapidIO
4-ch. DMA

8-lane SerDes
8-lane SerDes

DDR/DDR2 SDRAM Controller
DDR/DDR2 SDRAM Controller
Local Bus
Performance Monitor, DUART, MPC, 2 x I²C, Timers, GPIO, Interrupt Control

Core I/O
A couple examples...

- Freescale MPC8641D
  - P2020
  - P4080
  - ...

- Atmel 7913
  - Aeroflex UT699
  - ...

NEPP SOC Update for ETW 6/29/2011
A couple examples...

- Freescale MPC8641D
  - P2020
  - P4080
  - …
- Atmel 7913
  - Aeroflex UT699
  - …
- Boeing Maestro
NEPP Interest in SOCs

• SOCs gain popularity and will likely fly soon
  – UT699 is a controller on MISSE-7
  – Several programs interested in flying Maestro
  – SpaceMicro building Proton400k-L with Freescale P2020

• Single Event Effects Test methods unclear
  – Very complex devices
  – Multiple elements – do all need to be tested?
  – Hardware simulation of SEEs?
  – Manufacturing processes impact test methods
    • RHBD
    • Fault Tolerance
    • Multicore
NEPP Approach

- Devices are too complex for full characterization
- Test methods must target basic information needed for manufacturers and provide useful information for users to be aware of and/or mitigate radiation effects
- This approach seeks to provide the information necessary to understand the most important radiation effects for a given system, utilizing manufacturer assistance, and targeting actual application needs.

NEPP SOC Update for ETW 6/29/2011
Quick Word on Rad Effects

• TID
  – Accumulated total ionizing dose to a part
  – Impact can be evaluated by vendor or vendor-specific device parameter test hardware
  – Can be utilize normal reliability flow

• DDD
  – Accumulated displacement damage dose to a part
  – Testing is essentially the same as for TID

• SEE
  – Bit flips, voltage transients, or latchup
  – Testing requires special setup to operate part during exposure
  – Some types of events require observing the device perform the wrong operation
  – Terrestrial testing often requires mechanical modification to test boards and test parts
  – Failure or error modes do not necessarily follow a set of standard part screening methods – may be device specific.
Roadmap to Qualification Methods

• Identify the direction space-borne SOC utilization is going
• Establish requirements for applications
  – Communication with application users
  – Establishing viable test approaches
• Gain understanding of test methods for SEE evaluation of SOCs
  – Through partnerships with SOC manufacturers
  – And direct testing of SOCs to determine what works and what doesn’t
• Verify test methods and data by community review with users and manufacturers
• Establish a set of tools to enable qualification methods
  – Application user/manufacturer dialog
  – List of standard interfaces and device architecture elements to target
  – Standardized test approach(es)
  – Box of standard test algorithms for specific internal components
  – Data collection and analysis recommendations
  – Examples of interpretation of results
Target Areas under Development

- Collaboration with Manufacturers and Users
- On-Chip Peripheral Approach/Prioritization
- Fault Tolerant Device Test Approaches
- RHBD Device Challenges to Test Development
- Multicore Device Unique Challenges
- General Test Methods
- Collecting Results from Sample Testing
Collaboration Considerations

• Direct subjects: Aeroflex UT699, Freescale P2020, Boeing Maestro, and some others under development

• Working with users to identify most important devices and most important SEE modes: JPL, GSFC, and industry partners

• Test collaborations:
  – User input on key test needs
  – Test collaborators elsewhere in the SEE community
  – Industry test partners are especially needed – the current work reflects interaction with Aeroflex, Boeing, SpaceMicro, and others
SOCs are Complex Devices

• Built from many sub-units
  – When designing a test approach we must prioritize – what is most likely to be used
  – Each likely unit requires a special approach to test methods
  – Some common structure can be exploited, but requires manufacturer participation

• Developed test approaches
  – Hardware development not feasible – have to use demonstration boards
  – Microprocessor approach is the most developed
  – Memory and spacecraft communications are next priority – Some SpaceWire methods developed
Fault Tolerant Considerations

- **Fault Tolerant Methods:**
  - Bit errors: Parity, ECC, Reed-Solomon
  - Device Fail: Reed-Solomon, Redundancy

- **What does this mean for testing?**
  - Testing these devices usually requires operating the device during testing – test code must handle faults
  - Ground testing is sped up compared to space
    - Requires significantly increased scrub rates
    - Creates test anomalies
  - Temptation to characterize things protected by fault tolerance must be avoided
RHBD Considerations

- Multi-part SEE sensitivity curve
  - Multiple leading event types at different LETs (see plot)
- Increase in SET sensitivity
  - Dynamic testing more important
  - May require better optimization of test code (to mimic compilers)
  - More detailed clock frequency testing
Multicore Considerations

• Isolation & Error propagation
  – Multiple simultaneous operations
  – Working on ways to orthogonalize problem
  – There are lots of propagation paths – we may have to focus on one device at a time (i.e. Maestro vs. multicore Freescale)

• System-level errors
  – PLL hits
  – Failed Communications or common sub units
Generalized Test Approach

• Approach must be Multi-stage
  – Realistic assumption, going to require a couple stages to the test approach

• Initial/early-stage approach – find out what you got
  – Establish methods to examine if device has big problems

• Establish basic sensitivities
  – Registers, caches, buffers, computation blocks, and modules that can be switched on or off

• Go after key items of the architecture
  – IO
  – Unique coexisting capabilities

• Application sensitivity – what the users really need to know
  – /100 or maybe even 1e3-1e4 reduction in application response
  – But may also miss sensitivities in real applications (like Branch History Table)
Testing Update Overview

• UT699 Test Results – tested with Aeroflex
  – SRAMs sensitivity,
  – Partial address reset,
  – SpaceWire

• Freescale P2020 efforts – tested with SpaceMicro
  – Measurement of basic processor sensitivities
Results – UT699 I of II

- UT699 SRAM Sensitivity
- There are 3 different dominant SEU modes
  - Below 20, see next; Between 20 and 60 – SRAM SEU; Above 60 – Flip Flop SEU

Original plot: Hafer et. al. 2009 NSREC DW
• Identified a special upset mode where 16 bits in a register get 0’d out.
• This is likely a SET effect
• We verified the cross section was independent of flux and fluence.
• This is an example of how RHBD devices have difficult SEE modes.
P2020 Testing

• Testing of P2020 in collaboration with SpaceMicro
• SpaceMicro uses the P2020 in their Proton400k-L space computer
• Testing was performed with a P2020RDB from Freescale
Results – P2020 I of II

• P2020 tested for SEUs using 55 MeV protons at UCB
  – Cores tested for L1, L2, and GPR sensitivity
  – L2 (4194304 bits – tested as SRAM):
    • ECC disabled
    • 10079 upsets in 2.36e11 protons/cm²
    • Yields cross section of 1.0e-14 cm²/bit
  – L1 (about 278528 bits – due to tags and invalidations)
    • Parity exceptions/checking disabled
    • No SBU seen until MBU, but disproportionately high invalid lines
    • We assume lines being invalidated by parity checking
    • 779 invalid lines in 2.36e11 protons/cm²
    • Yields cross section of 1.2e-14 cm²/bit
  – GPRs (704 bits)
    • 1 upset in 2.36e11 protons/cm²
    • Yields cross section of 0.6e-14 cm²/bit

• Only tested P2020 processor core thus far other test targets are:
  – Multi-processor coherency module
  – On-chip peripherals, especially: Ethernet, PCIe, MMU, Serial Rapid I/O, (SERDES)

#1: All tested elements have cross section about 1e-14cm²/bit @55MeV protons
#2: Basic microprocessor items tested – still need to do peripherals and coherence
Results – P2020 II of II

• Comparing 45nm P2020 results...
  – plotted with IBM750FX – 90nm
  – similar to e600-based Freescale parts (7448, 7447A)
  – Protons only... still need to do heavy ion testing

• Also looking at other Freescale multicore
  – Looking at P4080 and MPC8641D
Future Directions

• Continue collaboration building – especially on the user side.
  – Building goals based on desired data for users
  – But also need manufacturer support for correct sensitization and to provide input on what users desire to be hardened
  – Especially looking to orthogonalize the problem of error/fault propagation in complex multicore devices

• Continue improvement of test methods targeting the key areas discussed
  – Key peripherals, Fault Tolerance, RHBD elements, specific Multicore concerns
  – And overall improvement of generalized test approach to provide a roadmap for efficient device SEE research

• Immediate development targets
  – Freescale multicore devices, from P2020 to P4080
  – Others in our sites but not active: Maestro, Atmel AT7913, Aeroflex LEON 4
  – If you have other specific devices of interest, please contact steven.m.guertin@jpl.nasa.gov to discuss potential options

• Recommendations for SOC SEE test methods
  – Expect to develop this work into a general guideline for SEE evaluation and testing of complex SOCs
• SOCs are becoming more common and are expected to impact NASA soon
  – SOC here generally means devices complex devices carrying out multiple roles (rather than carrying out ALL roles)
  – Some are already flying or in planning stages
• NEPP approach is to try to close the loop between vendors, users, and radiation testers
  – Basic test data is needed,
  – But certain types of questions may require special test approaches (such as fault propagation)
  – Users may be unaware of how SEE testing maps to application sensitivity.
  – Many test types would benefit from manufacturer involvement, and some cannot be done without it.
Summary II of II

• Currently targeting 7 areas for development
  – Collaboration
  – Prioritizing device resources for evaluation
  – Approaches for Fault Tolerant element testing
  – Approaches for RHBD device testing
  – Multicore challenges
  – General test methods for SEE testing
  – Field validation by testing devices of interest

• Current or past testing targets
  – Aeroflex UT699 – found rare partial register reset (below 1 in 1e5 years in GEO), found very low SpaceWire upset rate
  – Boeing Maestro – Worked on methods for testing including identification of manufacturer functional test codes recommended for SEE testing, NEPP efforts on hold
  – Freescale P2020 and other devices – working on initial verification of test methods. Eventually plan to establish and demonstrate test methods on at least one of Freescale device.