



High-Density 3D TSOP Stack Packaging NEPP FY11 Summary Report

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1.0 INTRODUCTION

This report documents a reliability evaluation of a particular implementation of package-on-package (PoP) high-density electronic packaging technology. Package-on-package is just one of several new high density packaging technologies that offer significant reductions in overall required PCB board area while allowing for significant and often unique increases in device performance and functionality. The particular PoP technology tested for this report was provided by Interconnect Systems, Inc. (ISI). ISI utilizes standard, readily available device packaging methods in which high-density packaging is achieved through a combination of several technologies:

- Standard packaged memory devices
- 3-dimensional (3D) interconnect assembly

In general, 3D packaging provides a high level of functional integration in well-established package families (i.e., ball grid arrays [BGAs] and lead-frame packages) by using stacking die, stacking packages, or a mix of both, and a combination of assembly technologies including wire bonding, flip-chip, and surface mount solder operations. These technologies offer cost-effective solutions for low or medium volume applications, typically used in NASA projects. This task examined a particular type of high-density packaging used for flash memory in thin, small outline packages (TSOPs) in a soldered, stacked configuration. The stackable package contains pads on the top of the package that facilitate the stacking process.

This task is a result of a recommendation from the 2007 NEPP Packaging Roadmap.

2.0 HIGH-DENSITY 3D PACKAGING TRENDS

Flash memory has become a fundamental building block in today's electronic systems and is an ideal candidate for integrated memory implementation. Its content can be changed in the field and thus provides broad flexibility in applications. The increasing use of flash memory in today's electronic systems is helping drive the trend in high-density electronics packaging to the extent that packaging has migrated to the third dimension (3D) and has now become mainstream technology. These new packaging configurations can combine flip chips, wire-bond interconnection, solder, laminate substrates, and over-molding of module assemblies. Package-level integration of disparate device functions is possible and produced through 3D die and package stacking. However, wire-bonding remains the most popular method for low-density connections of less than 200 input/output (I/O) per chip; although it is becoming more difficult to meet the demands for wiring connectivity merely by increasing the number of the peripheral wire-bonds. In order to overcome such wiring connectivity issues, 3D chip stacking technology using through-silicon-via (TSV) technology is attractive because it offers the possibility of solving the serious interconnection problems while offering integrated functions for higher performance. TSV is a novel packaging technology that JPL continues to monitor for future NASA applications.

2.1 Stacked Wire-Bonded Die

Vertical chip stacking is performed as chip-to-chip, chip-to-wafer, or wafer-to-wafer processes. Stacked die packages consist of bare die stacked and interconnected using wire-bond and flip-chip connections in one standard package. Figure 2.1-1 shows an example of this. This packaging technology results in the thinnest package with the lowest assembly cost and the potential for the highest board-level reliability. This is due to the fact that soldered interconnects are minimized. Low-profile wire bonding is a critical process for this technology. Stacked die utilizing silicon spacers or epoxy filled with spherical spacers are used to control die-to-die spacing. From a reliability standpoint, the addition of silicon into the package increases the bending resistance and the risk and/or vulnerability for cracks during assembly or qualification testing. These cracks can occur, either in the package body (molding compound) or in the die itself.

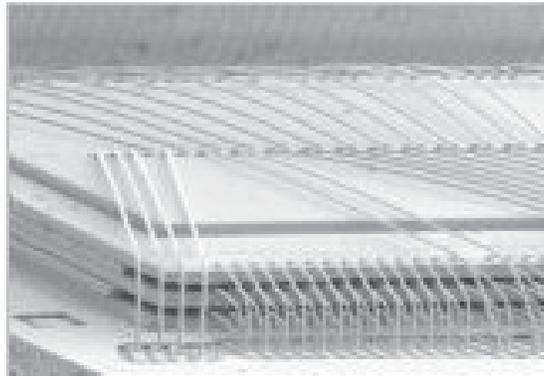


Figure 2.1-1. Stacked wire-bonded die.
Source: STATS ChipPAC

2.2 Package-on-Package (PoP)

Package-on-package (PoP) is a package technology where pre-packaged devices are vertically stacked on top of each other using a lead-frame, printed wiring board, or flex interconnects to integrate different functionalities while still remaining a compact size. For example, combining memory and logic into a single PoP offers advantages in procurement, lower cost, better total system costs, and faster time to produce and integrate into applications. Electrically, PoP offers benefits by minimizing trace lengths between different interoperating parts, yielding better performance, faster signal propagation, and reduced noise and cross-talk. Another benefit is that separate testing (and burn-in) of each package can be conducted before assembly into the integrated structure.

PoP technology has advanced to the point where the JEDEC JC11 committee has developed guidelines and standards related to PoP technology. In March 2007, they released JEDEC Publication 95, Design Guide 4.21A, “Internal Stacking Module, Land Grid Array Packages with External Interconnect Terminals (ISM)” and in January 2009, they released MO-266C, a registration drawing for “Very Thin, Fine-Pitch, Stackable Ball Grid, 0.50 mm Ball Pitch Array Family, VF-XBGA.” Most recently, they released another registration standard in April 2010, MO-302A for “Very Thin, Fine-Pitch, Fully Overmolded, Stackable, Ball Grid Array Family, 0.40 mm Ball Pitch, VF-XBGA.”

PoP technology is not without manufacturing or reliability issues. As the stacked packages may be procured from different suppliers, there is a chance that their expansion coefficients can vary and cause warpage during and after the reflow joining process. Warpage is the result of residual stress induced by non-uniform package shrinkage. Various methods have been implemented to counter these effects. The addition of smaller solder balls on the top pad of the bottom package helps absorb the effect of package warpage, while keeping the total volume of solder paste used to a minimum. In addition, overmolding the assembly can help reduce the effect of these residual stresses.

2.3 Package-in-Package (PiP)

Package-in-package (PiP) technology extends traditional packaging by utilizing a combination or “hybridization” of dissimilar packaging technologies. An example of this technology may contain individual die in flip-chip formats integrated with pre-packaged, pre-tested formats like PoP. Combining wire-bonded die on organic substrates or flex interconnected die may further miniaturize the package. Most challenges are in the construction of the package and include bumping of thin wafers, die cracking, thin die flip-chip attachment, underfilling, substrate and package warpage and parametric shifts in the die. Package integration requires innovative assembly techniques and more rigorous methodologies and assembly design rules for managing chip-package interactions.

2.4 Through Silicon Via (TSV)

Stacked memory die is an ideal choice for using TSV technology as all interconnections of each die align with the corresponding die located above and below. Vertical electrical connections (vias) pass through the silicon wafer or die. This is a high-performance 3D packaging technique compared to PoP technology because via density can be substantially higher and trace lengths are shorter. Most device manufacturers are involved with TSV or variations of TSV technology. Glass interposer technology used in conjunction or in place of TSV technology is also being developed and noted in recent literature.

3.0 EVALUATION APPROACH

3.1 Package Construction

The package selected for this evaluation utilizes PoP technology consisting of 48-lead TSOPs solder stacked (both 2-high and 4-high) and integrated into single dual-flat no-lead (DFN) packages (Figure 3.1-1) Topline dummy packages were used in a daisy chain configuration for interconnect testing (Figure 3.1-2). Lead-free solder was used in the stacking assembly process and 63Sn-37Pb solder was used to mount the package to the test board. Ablestik ABLEFILL[®] UF8828 MRCE underfill was applied after mounting to the board. This particular underfill exhibits high T_g and high-fracture toughness and is engineered to withstand the 260°C peak reflow temperature associated with Pb-free soldering. All material selections and assembly were performed by ISI. An example of the completed assembly is shown in Figure 3.1-3.

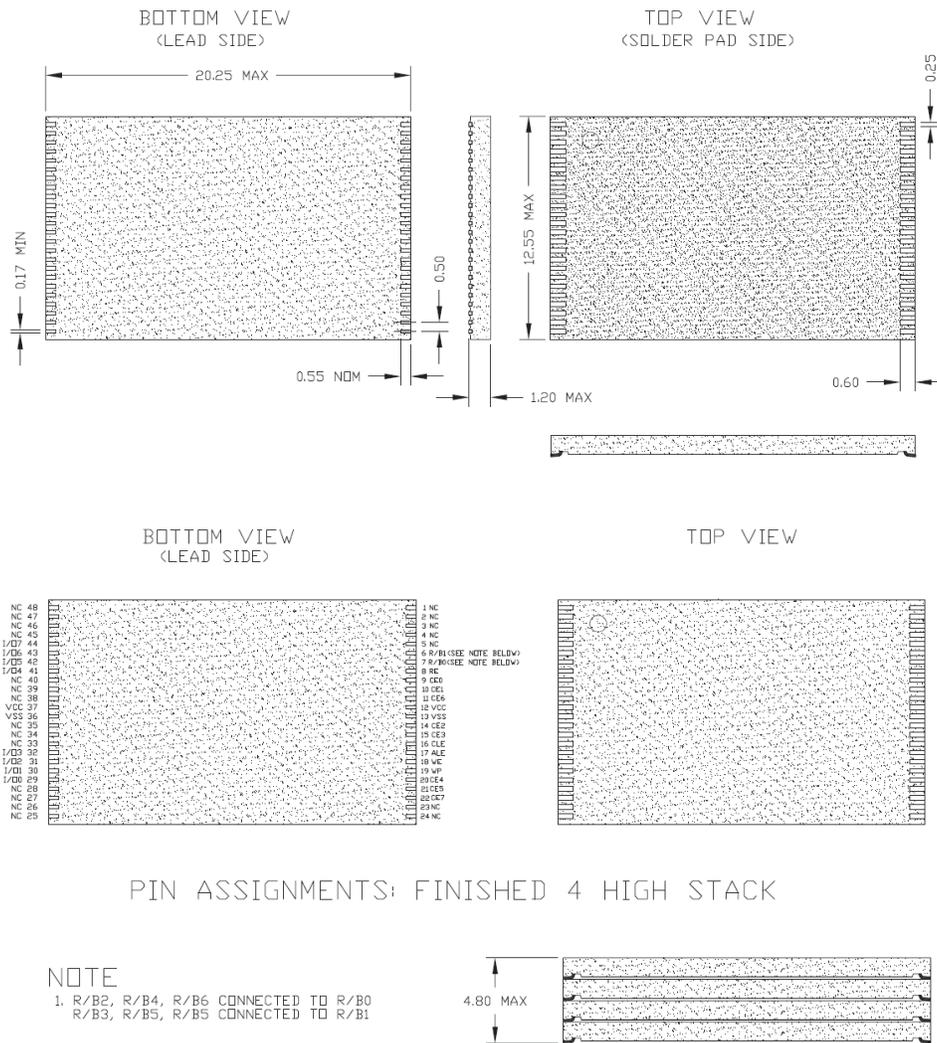


Figure 3.1-1. ISI stacked TSOP package—standard TSOP converted to stackable DFN.

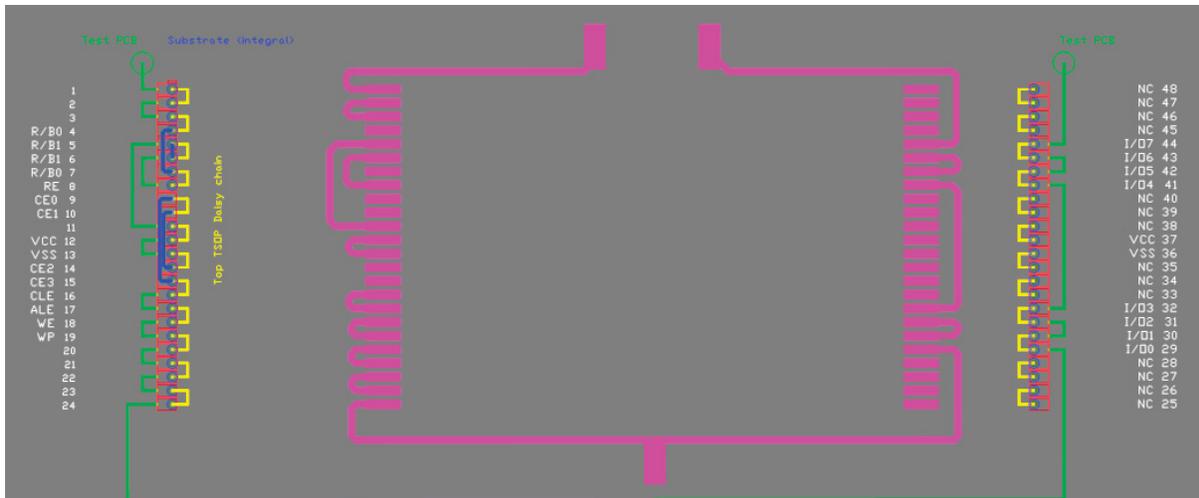


Figure 3.1-2. Daisy chain pattern.

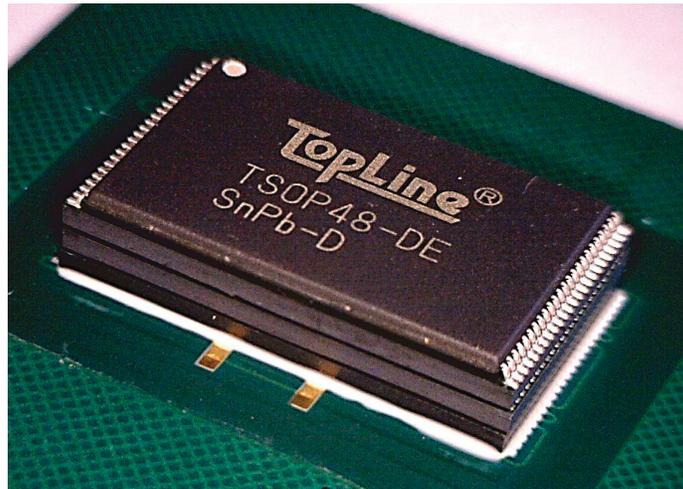


Figure 3.1-3. ISI 4-high TSOP stacked package surface-mounted and epoxy-underfilled.

3.2 Testing

Thermal cycle testing was conducted in accordance with MIL-STD-883, Method 1010, Test Condition B (temperature cycling, -55°C to $+125^{\circ}\text{C}$). See Figure 3.2-1 for typical profile. Series resistance was monitored periodically to 500 cycles and recorded.

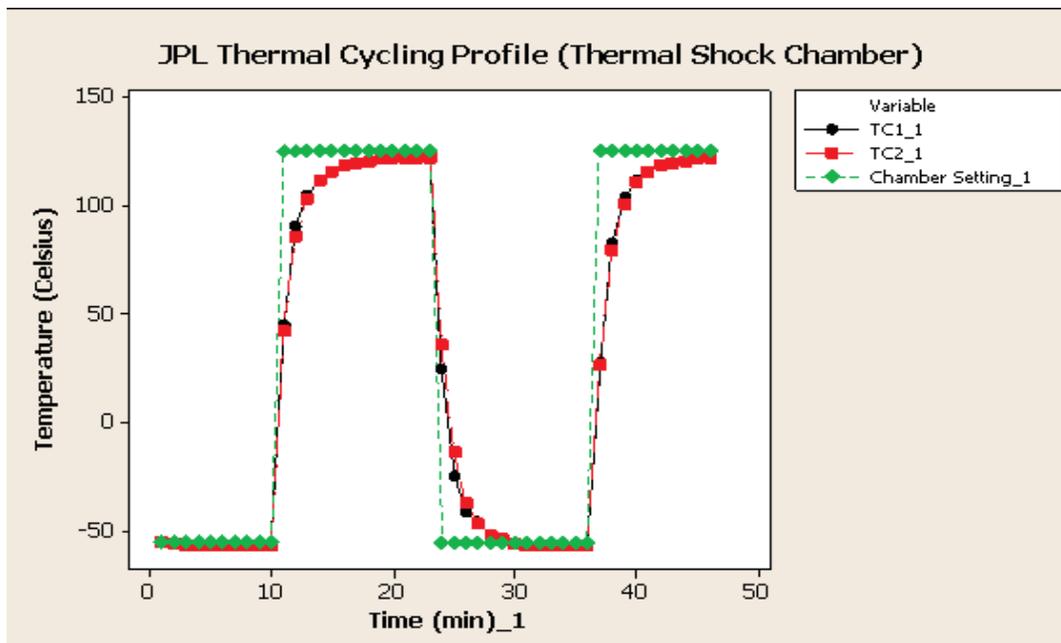


Figure 3.2-1. Temperature cycle profile.

4.0 RESULTS

The daisy chain series resistance is shown in Table 4-1 for the 2-high stack assemblies and in Table 4-2 for the 4-high stack assemblies. Figures 4-1 and 4-2 show corresponding plots of these data.

Table 4-1. 2-high stack daisy chain resistance (Ω).

		# Cycles										
		0	50	100	150	200	250	300	350	400	450	500
Module #	1	1.535	1.586	1.596	1.556	1.554	1.588	1.590	1.521	1.609	1.577	1.562
	2	1.463	1.571	1.512	1.514	1.513	1.571	1.640	1.694	1.886	2.143	10000
	3	1.451	1.486	1.435	1.429	1.493	1.495	1.416	1.405	1.450	1.478	1.483
	4	1.372	1.512	1.493	1.480	1.558	1.663	2.545	3.575	9.459	7.708	11.546
	5	1.471	1.517	1.463	1.502	1.527	1.603	1.575	1.619	1.662	1.734	1.760
	6	1.474	1.630	1.584	1.542	1.505	1.522	1.582	1.536	1.596	1.605	1.710
	7	1.527	1.734	1.547	1.471	1.513	1.592	1.828	10000	10000	10000	10000
	8	1.482	1.561	1.561	1.586	1.689	1.805	1.887	1.995	2.067	2.124	2.211
	9	1.487	1.637	1.572	1.541	1.501	1.592	1.541	1.507	1.575	1.516	1.510
	10	1.537	1.823	1.725	1.629	1.568	1.593	1.574	1.617	1.740	1.850	2.587

Note: $\geq 10000 \Omega$ is considered an open connection

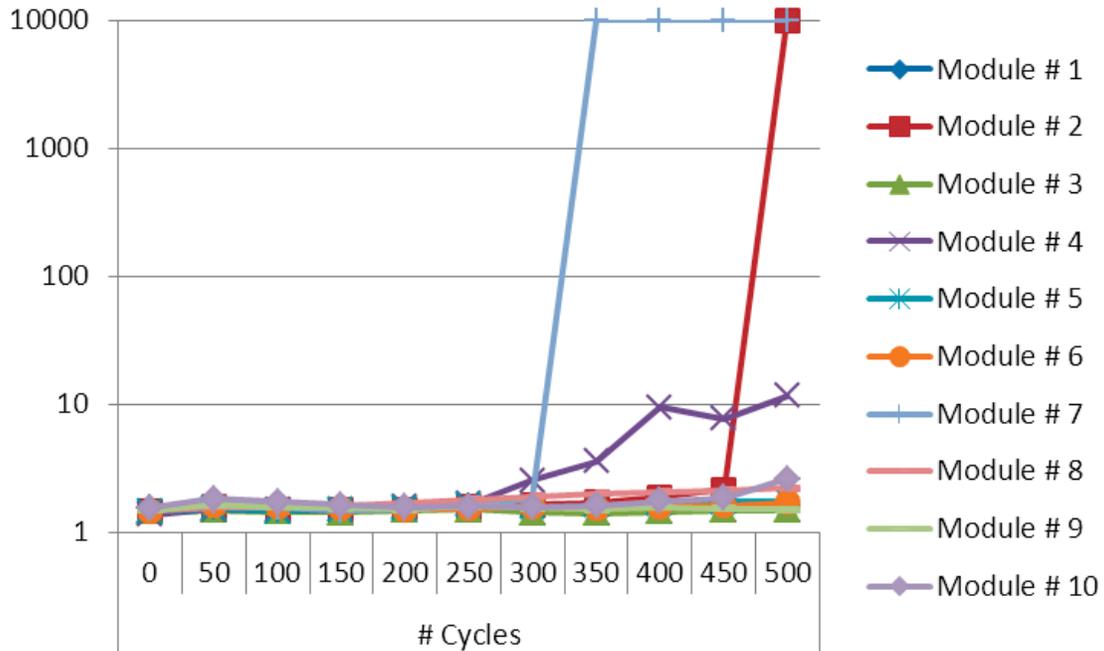


Figure 4-1. Plot of Table 4-1 data.

Table 4-2. 4-high stack daisy chain resistance (Ω).

		# Cycles										
		0	50	100	150	200	250	300	350	400	450	500
Module #	11	1.928	2.161	2.033	2.359	3.301	10000	10000	10000	10000	10000	10000
	12	1.932	2.209	2.111	2.157	2.371	2.528	3.061	10.159	9.671	6.513	6.881
	13	2.011	2.440	3.068	3.567	4.171	5.943	6.166	7.674	11.142	12.798	18.904
	14	1.883	1.980	1.994	2.087	2.151	2.155	2.771	2.657	3.182	12.430	10000
	15	1.812	2.056	2.129	2.233	2.468	2.716	2.920	10000	10000	10000	10000
	16	1.894	2.132	2.187	2.464	4.177	8.288	6.020	5.629	11.807	11.495	14.716
	17	1.902	2.308	2.424	2.855	3.095	3.501	4.168	4.430	5.485	11.739	10000
	18	1.841	2.354	2.529	3.230	4.317	4.668	5.345	5.611	6.424	6.932	8.127
	19	1.908	2.215	2.102	2.298	2.752	13.041	12.247	7.077	21.088	10000	10000
	20	1.912	2.208	2.289	2.454	2.597	2.775	3.077	3.362	3.908	4.134	4.359

Note: $\geq 10000 \Omega$ is considered an open connection

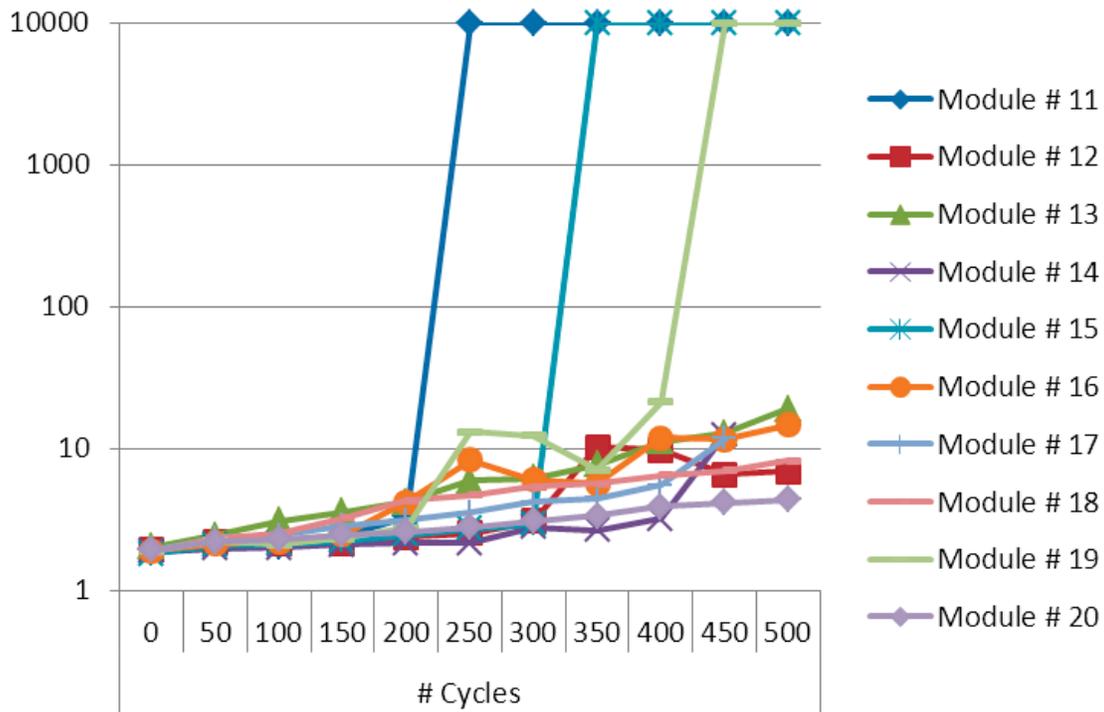


Figure 4-2. Plot of Table 4-2 data.

5.0 DISCUSSION

The change in electrical resistance with the increasing number of temperature cycles is an indication of an imminent interconnection failure. An electrical resistance of greater than or equal to 10,000 ohms (Ω) is considered an electrical open, a clear failure. The 2-high stack package exhibited stability (arbitrarily less than 10% changes in resistance) within 250 cycles of testing, whereas the 4-high stack package became unstable (greater than 10% change in resistance) within 50–100 cycles of testing. Figure 5-1 is a plot of the cumulative percentage failures versus the number of temperature cycles. This figure shows that the 4-high stack has an increased failure rate over the 2-high stack by a factor of 1.43, which is the ratio of the slopes of the two linear fits for the data.

This significant increase in failure rate coupled with the steadily increasing resistance prior to failure means that the 4-high stack PoP approach implemented in this test is not acceptable for NASA applications.

Due to the limited amount of resources available for this task, a complete root cause failure analysis was not performed on any of the failures from the two different package assemblies. A general discussion of the possible failure mechanisms is provided for completeness, however. The location of these interconnection failures is either within the stack package itself, at the package-to-board interface, or at a combination of these two possible locations. Understanding the material aspects of the packaging construction is essential to not only the assembly of such parts, but also to the design of a reliable product. In this particular PoP construction, the package assembler has no control of the geometries or material selection used in the stacked configuration. It is entirely conceivable that the particular multiple materials of construction with varying coefficients of expansion (CTE), elastic moduli, and strengths contributed to the relatively low interconnection life exhibited in these results. In this particular PoP technology, the package assembler can only control the choice of solder and the associated processing, and whether to overmold the assembly (in which case, the assembler has a choice of overmold material). Overmolding can have some major effects on the CTE; however, in this case, no overmolding was conducted on the

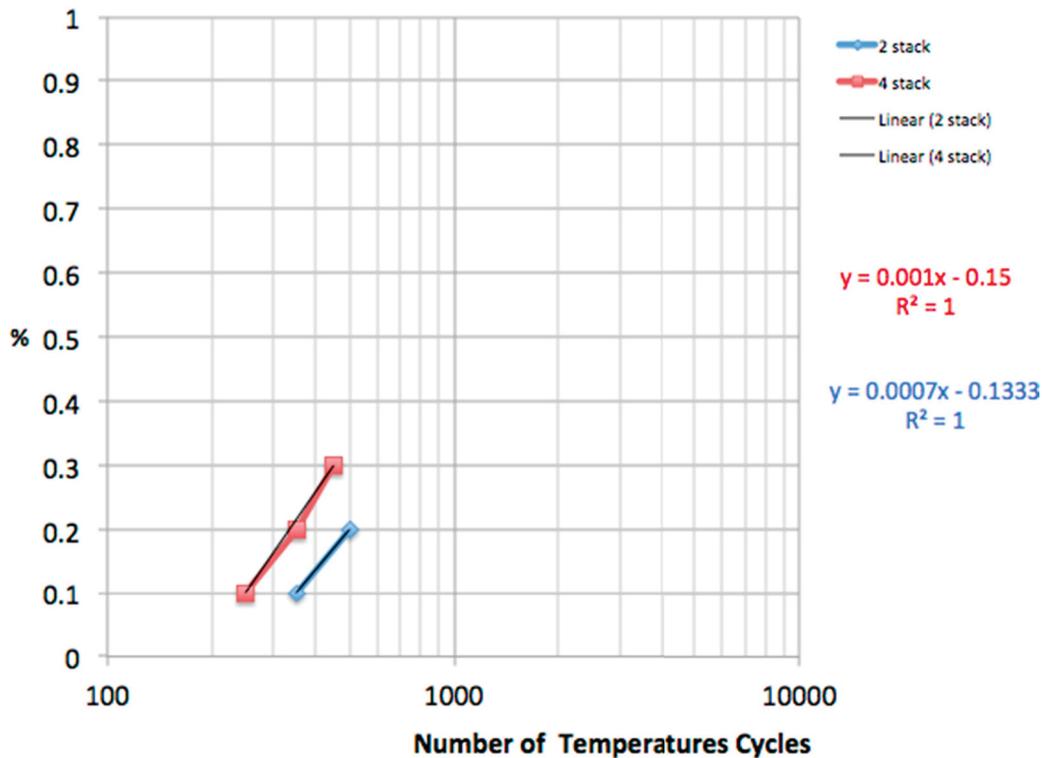


Figure 5-1. Cumulative percentage failure vs. number of temperature cycles.

assemblies. From a board reliability standpoint, the user of these packaged assemblies has some control over the choice of board material, solder, and underfill. ISI had control over all material choices, except the TSOP packages and their geometries. The packages used in this evaluation were procured fully assembled, mounted, and underfilled to the test boards.

Isolation of the interconnection failures was not conducted due to the limited resources in this task. However, computed tomography x-ray was conducted on the parts with open interconnections in an attempt to visually isolate the failure. Figures 5-2 and 5-3 show composite images for the 2-high and 4-high stack assemblies, respectively.

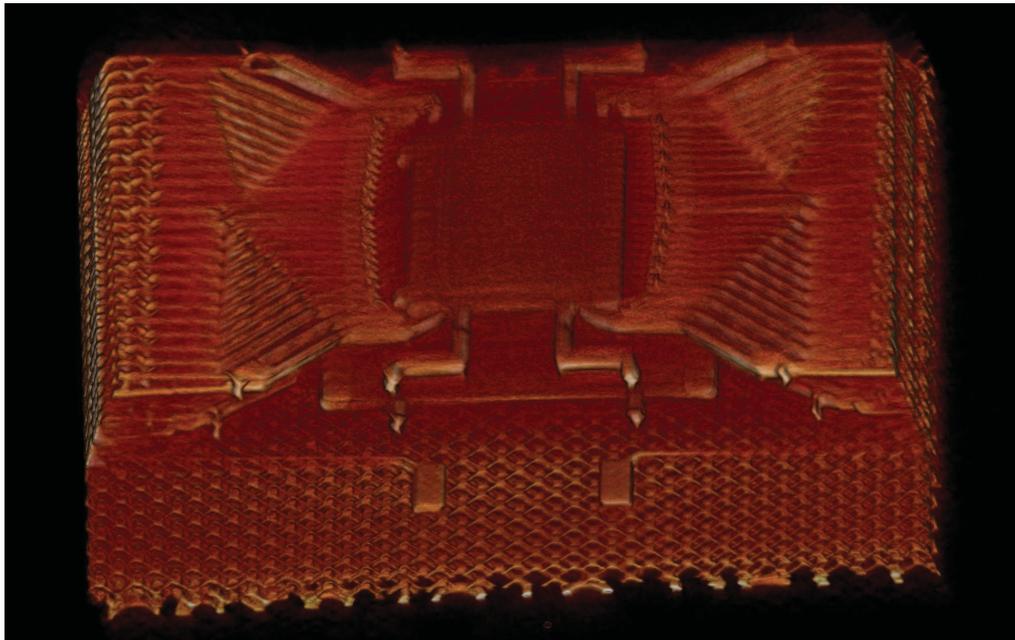


Figure 5-2. Computed tomograph X-ray of the 2-high stack assembly.

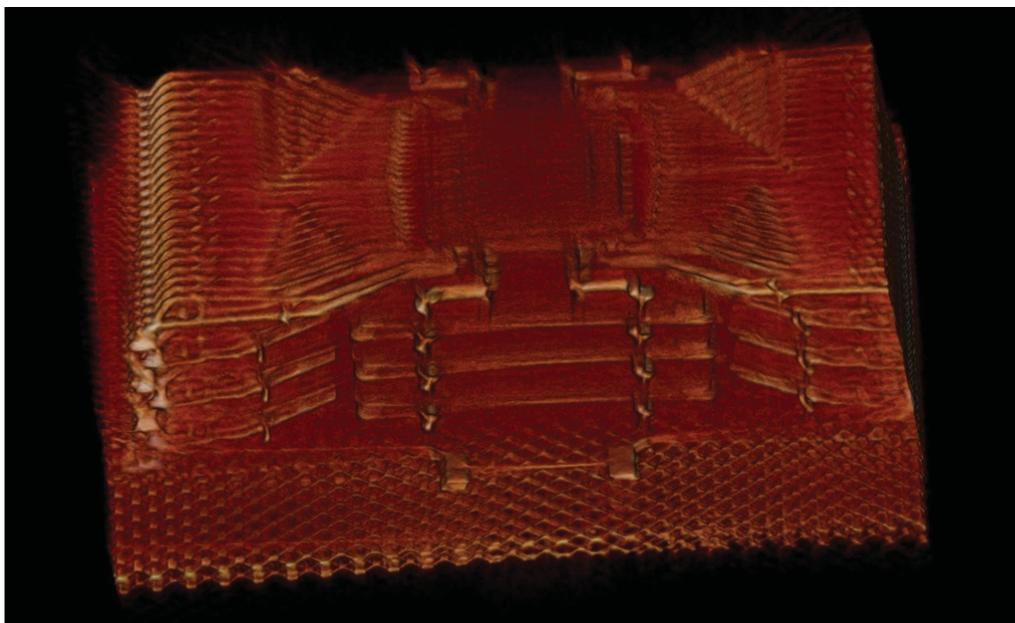


Figure 5-3. Computed tomograph X-ray of the 4-high stack assembly.

6.0 SUMMARY AND RECOMMENDATIONS

Although this particular PoP technology offers advantages in 3D high-density packaging with readily available (TSOP to DFN) technology, it was found that this packaging technology does not meet minimum reliability expectations when evaluated under standard temperature cycling methods typically used in electronics packaging qualification tests for NASA applications.

Isolation of specific open interconnection failures did not occur due to the limited available resources in this task. Specific failed units were sent to ISI for their evaluation. As of the completion of this report, no feedback on that evaluation has been received.

Extremely limited evaluations have been conducted within NASA to characterize reliability and failure behavior of PoP/PiP technologies. At the same time, these technologies offer significant packaging advantages where mass and space are factors in a particular application. Thus, future evaluations are recommended. However, it is also acknowledged that a wide variety of 3D packaging options are currently available from various sources and there is limited reliability information to support their adoption. Because of this, the following short-term recommendations are made:

- Conduct 3D stacked packaging survey of suppliers.
- Secure available reliability data, particularly as a function of materials and construction.
- Review PoP/PiP packages most applicable for high reliability applications.
- Monitor progress of TSV stack technologies

The long-term recommendation is to physically evaluate 3D stacked packages/assemblies based on the results of the above short-term recommendations.