National Aeronautics and Space Administration

Radiation Tests of Highly Scaled, High-Density, Commercial, Nonvolatile NAND Flash Memories—Update 2010

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I. Introduction

The space radiation environment poses a certain radiation risk to all electronic components on the earth-orbiting and planetary mission spacecrafts. In recent years, there has been increased interest in the use of high-density, commercial, nonvolatile flash memories in space because of ever-increasing data volumes and strict power requirements. They are used in a wide variety of spacecraft subsystems. At one end of the spectrum, flash memories are used to store small amounts of mission-critical data such as boot code or configuration files and, at the other end, they are used to construct multi-gigabyte data recorders that record mission data.

Information on floating gates (FGs) is embedded by the presence or absence of trapped charge on an electrically isolated conductor. Nevertheless, flash memories are susceptible to upset and degradation from radiation, and more information is needed on their radiation response before they can be used in space. Flash memories have been the subject of several ionizing radiation effects studies in recent years, regarding both total ionizing dose (TID) [1–3] and single-event effect (SEE) [4–7] experiments. In both cases, the complex control circuitry has been demonstrated to be the most vulnerable part of commercial devices. However, the degradation of the threshold voltage (VTH) of a single cell in the floating gate array after exposure to ionizing radiation is a non-negligible issue, as it may lead to the corruption of the stored data. The functionality of flash memories begins to fail as TID accumulates during a space mission. Older generations of flash memories functionally failed during erase/write modes at approximately 10 krad (SiO_2) [1]. In addition, different functional failures have been detected in some commercial devices depending on the mode of operation during radiation exposure, including reduced speed, higher leakage currents, standby power supply currents, variation in timing parameters, and possible loss of device functionality [6–9]. In addition, direct strikes from galactic cosmic rays (GCRs) and protons from a solar flare can upset internal circuitry associated with structures such as the charge pump, state buffers, cache, or internal microcontrollers, as well as FG arrays. These upsets can result in incorrect read/write operation or even cause the device not to function until it is power cycled, reinitializing all the internal circuitry.

At present, the industry trend is to continue with feature-size scaling. The impact of single-event upset (SEU) on the highly scaled memories, because of their shrinking dimensions and increasing densities, has become a significant reliability concern. In advanced flash memories, one would expect the SEU cross section per bit to become smaller with shrinking feature sizes [2]. Furthermore, the SEU cross section for the FG arrays is becoming comparable to, if not larger, than that of the control logic. The SEU cross section can be dominated by either the FG array or the control logic, depending on the particular application [4]. In addition, because of thinner oxide layers, the total dose response is improved, although the tunnel oxides have not been scaled as aggressively as other oxides because of concerns about retention [2]. The last several generations of NAND flash memories have had only 7–10 nm tunnel oxides.

High-density, commercial, nonvolatile flash memories with NAND architecture are now available from several manufacturers. This report examines SEE effects and TID response in single-level cell (SLC) and multi-level cell (MLC) NAND flash memories manufactured by Micron Technology.

II. Experimental Procedure

II.A Device Descriptions

The part number, date code, and processes feature size of the parts studied in this report are summarized in Table 1. In general, a NAND structure consists of 32 cells. SLC NAND stores two binary states (either a binary 1 or a binary 0) in a single cell, whereas MLC NAND can store four states: 00, 01, 10, and 11. To recognize the four states (11, 10, 01, and 00), special circuitry must be added to allow the amount of charge stored in the FG to be controlled within narrow limits during the writing, and also to detect the different amounts of charge during reading. The programming circuits must deliver precise amounts of electrons to the FG, and the sense amps must distinguish between the four small threshold voltage regimes. There is considerably more design margin with the SLC device, which leads to greater radiation robustness, reliability, and endurance compared to the MLC device.

Table 1. Micron Technology NAND Flash Memories under Study

Part Number	Density (Gb)	Date Code	Feature Size (nm)
MT29F1G08AAC	1 SLC	0912	120
MT29F2G08AAD	2 SLC	0902	90
MT29F4G08AAC	4 SLC	0932	72
MT29F8G08AAA	8 SLC	0834	51
MT29F8G08MAA	8 MLC	0830	51
MT29F16G08AAA	16 MLC	0752	42
MT29F32G08AAA	32 MLC	0942	32

II.B Test Facility and Procedure

II.B.1 SEE Measurements

Heavy ion SEU measurements were performed at three facilities—the SEU Test Facility located at Brookhaven National Laboratory (BNL); the cyclotron facility at Jyväskylä, Finland (RADEF); and the Cyclotron Institute of Texas A&M University (TAMU). All three facilities provide a variety of ion beams over a range of energies for testing. Ion beams used in the measurements are listed in Table 2 for BNL, Table 3 for RADEF, and Table 4 for TAMU. LET and range values are for normal incident ions. At all three facilities, test boards containing the device under test (DUT) were mounted to the facilities' test frames. Tests at BNL were done in vacuum, and tests at RADEF and TAMU were done in air. The beam flux ranged from 3×10^2 to 5×10^5 ions/cm^{2}sec. The radiation measurements for Micron Technology 1-, 2-, 4-, and 8-Gb SLC devices were done at BNL and TAMU, and for Micron Technology 32-Gb MLC devices, at RADEF and TAMU. SEE tests were not performed on the 8- or 16-Gb MLC devices.

The DUTs were etched to remove the plastic packaging and expose them to the ion beam. Removal of the plastic packaging did not affect the DUTs' parameters such as standby current. The SEE data for NAND flash memories at both facilities were taken using a commercial memory tester called the JD Instruments (JDI) tester. The JDI ATV tester uses both custom ASIC and FPGA hardware with a built-in graphical interface. The JDI tester is fully capable of performing high-speed testing on memory systems using algorithmically generated test vectors.

The maximum operating frequency of the JDI is a 50 MHz cycle time. The operating frequency during the measurements was 17 MHz. The DUT was biased only at 3.6 V (3.3 V nominal power supply, plus 10%) during irradiation. No measurements at 3.3 or 3.0 V were performed.

All tests were conducted by first loading the DUT with all "0" pattern and then verifying the pattern by reading it back from the device. The complete Read cycle for the Micron Technology 32-Gb MLC devices is around 20 minutes. During irradiation, the DUT was dynamically operated in Read mode. After irradiation and the completion of the final Read cycle that was started during irradiation, the device's power was cycled, the DUT was read again, checked for errors, and logged. This method ensured that the errors are from bit upsets in the FGs. Then the pattern was erased and rewritten to make the device ready for the next run.

Table 2. Ion Beams Used in SEE Measurements at BNL

Ion	LET (MeV-cm2/mg)	Range (μm)
^{28}Si	8.0	74
^{35}Cl	11.5	64
^{48}Ti	19.8	40
^{80}Br	37.3	36
^{107}Ag	52.9	31

Table 3. Ion Beams Used in SEE Measurements at RADEF

Ion	LET (MeV-cm2/mg)	Range (μm)
^{15}N	1.8	202
^{20}Ne	3.6	146
^{40}Ar	10.1	118
^{56}Fe	18.8	97
^{82}Kr	32.1	94
^{131}Xe	60.5	89

Table 4. Ion Beams Used in SEE Measurements at TAMU

Ion	LET (MeV-cm2/mg)	Range (μm)
^{4}He	0.1	1386
^{14}N	1.3	199
^{20}Ne	2.7	279
^{129}Xe	51.5	120

II.B.2 TID Measurements

Total dose measurements were done using the JPL Co-60 facility at a dose rate of 50 rad (SiO_2) per second at room temperature. In all measurements, the DUTs were under static bias (3.6 V) during irradiation but not actively exercised because this corresponds to the actual operating condition during most of an extended space mission.

The TID data were taken using the JDI tester. All tests were conducted by first loading the DUT with all "0" pattern and then verifying the pattern by reading it back from the device. In all measurements, the standby currents were measured for each dose increment. We also counted bit errors, which were produced because of the shift in the threshold voltage. TID measurements were performed in the following two modes:

1. Refresh mode (Erase/Program/Read):
   a. Erase, write, and read to validate programmed numbers.
   b. Irradiate DUTs with static bias.
   c. Read numbers to ensure data retention.
   d. Repeat steps a to c for each radiation increment.

2. No Refresh mode (Read Only):
   a. Erase, write, and read to validate programmed numbers.
   b. Irradiate DUTs with static bias.
   c. Read numbers to ensure data retention.
   d. Repeat steps b to c for each radiation increment.

III. SEE Test Results

Three types of radiation-induced events were measured while performing read operations during irradiation: SEU, single-event functional interrupt (SEFI), and high-current spikes, which in some cases caused catastrophic device failure that manifested itself as a loss in ability to erase and program the DUT. Three samples were measured.

III.A SEUs

During SEU measurements, the beam flux was set to approximately 2×10^2 ions/cm^2 per second and the DUT was irradiated for 10–12 seconds in order to prevent occurrence of SEFIs. These measurements were performed at RADEF and TAMU. The three samples' measurements showed excellent agreement, indicating that part-to-part variations were not an issue. Therefore, cross sections from three samples of the same device are averaged together in the SEE data reported. Measurements were performed with heavy ions having an LET range of 0.1–60 MeV-cm^2/mg at normal incidence. Tests were done at normal incidence and also at angles. Two types of rotations were used to obtain data at angles. Starting with a normal-incident position, a rotation of the device about the vertical axis of the device will be called a "horizontal rotation." The horizontal rotation angles that were tested are ±30 and ±60 degrees. Going back to the normal-incident position, a rotation of the device about the horizontal axis of the device will be called a "vertical rotation." A vertical rotation angle of +60 degrees was tested.

In all cases, the absolute value of the rotation angle is also the tilt angle (angle between the beam and the device normal), but different types of rotations (plus, minus, horizontal, vertical) describe different ways in which the tilt was obtained. Figure 1 shows the average SEU cross section for three samples of Micron Technology 32-Gb MLC devices. The saturated FG SEU cross section per bit is on the order of 3×10^{-10} cm^2/bit. The error bars are smaller than the size of the plotting symbols. The FG SEU rate is 5.1×10^{-9} per bit per day for the background GCRs environment. The rate for the worst week CREME96 model flare is 2.9×10^{-6} per bit per day, producing an accumulated number over the duration of the flare that is equal to 2.0×10^{-5} per bit per flare. Only data measured at normal incidence are shown in Figure 1. Additional data at

angles using the various types of rotations previously discussed were obtained but not included in Figure 1. These data suggest that SEU susceptibility of the FGs follows the cosine law, but there is some uncertainty because a complete sampling of angles was done for only one ion species (Xe). Because of a lack of FG SEU data for Micron Technology 8- and 16-Gb MLC, we cannot address the scaling effect on MLC devices.

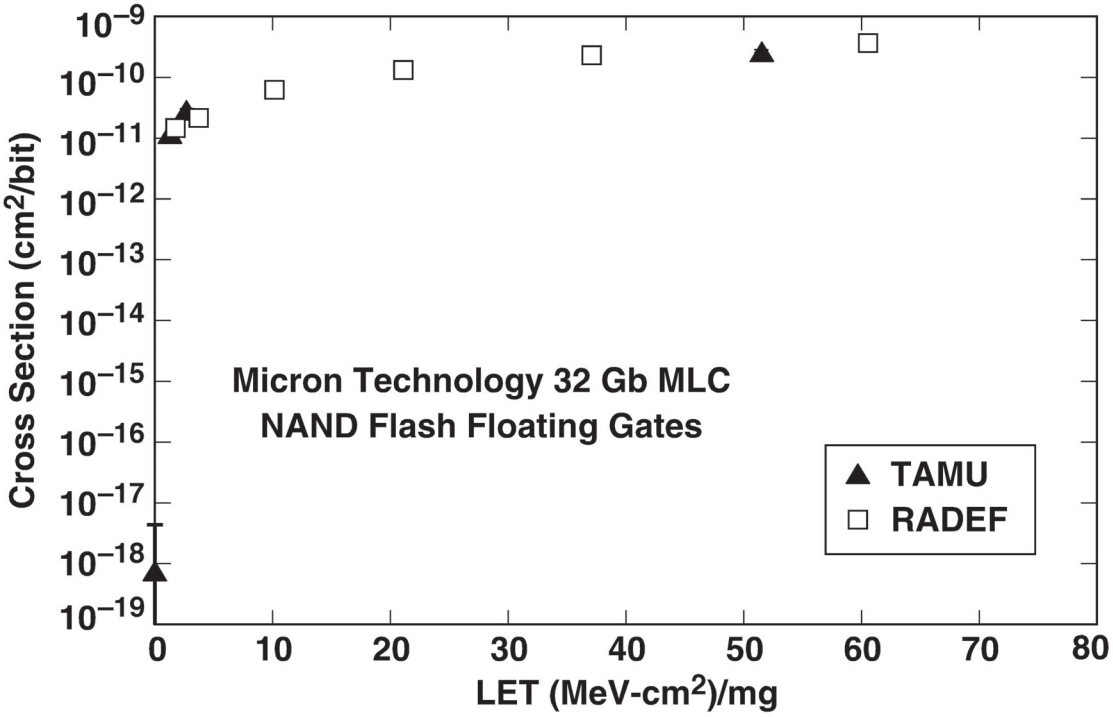

Figure 1. SEU cross section for Micron Technology 32-Gb MLC NAND flash memory. Measurements were performed at RADEF and TAMU.

Figure 2 compares the average FG SEU cross section for three samples of Micron Technology 1-, 2-, 4- and 8-Gb SLC NAND flash memories. All measurements were performed at normal incidence. The error bars are smaller than the size of the plotting symbols. These measurements were performed at BNL and TAMU. The SEU cross section presented in Figure 2 covers feature sizes from 120 to 51 nm. The threshold LET does not change with scaling. At LETs below 7 MeV there are no noticeable differences between SEUs and threshold LETs for the 1-, 2-, 4- and 8-Gb devices. In Figure 3, we display the average FG SEU cross section for three samples of Micron Technology 1-, 2-, 4-, and 8-Gb for LETs above 7 MeV-cm2/mg. The higher resolution of the vertical scale in Figure 3 (compared to Figure 2) gives a clearer comparison between the different devices at the higher LETs. Note that similar to low LET data points (LET below 7 MeV-cm2/mg) there are no noticeable differences in SEUs in the range of 120–72 nm feature size; however, there is a reduction in the SEU cross section at 51-nm feature size. This indicates that scaling effects is effective below a certain feature size, in this case below 72 nm. A similar behavior has been observed in the commercial highly scaled PowerPC processors [9]. As was mentioned in Section II, there is considerably more design margin with SLC, which leads to greater radiation robustness, reliability, and endurance compared to MLC. The differences between SEU susceptibility between SLC and MLC devices are clearly noticeable by comparison of data presented in Figures 1 and 2. The SLC 5-nm part (8 Gb) is less susceptible than is the MLC 32-nm part (32 Gb).

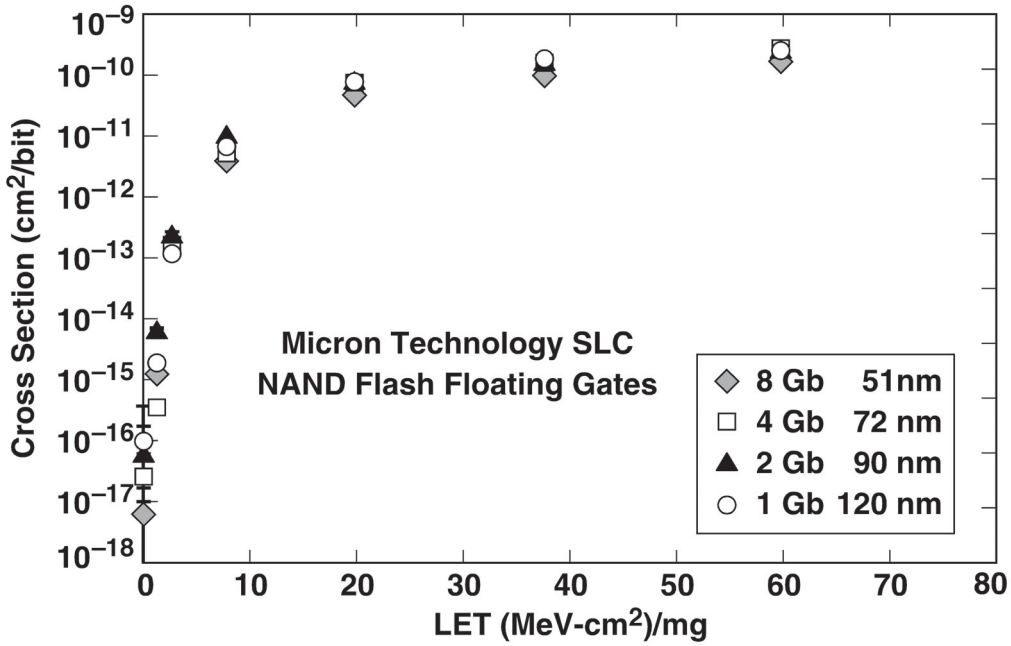

Figure 2. SEU cross sections for Micron Technology SLC NAND flash memories. Measurements were performed at BNL and TAMU.

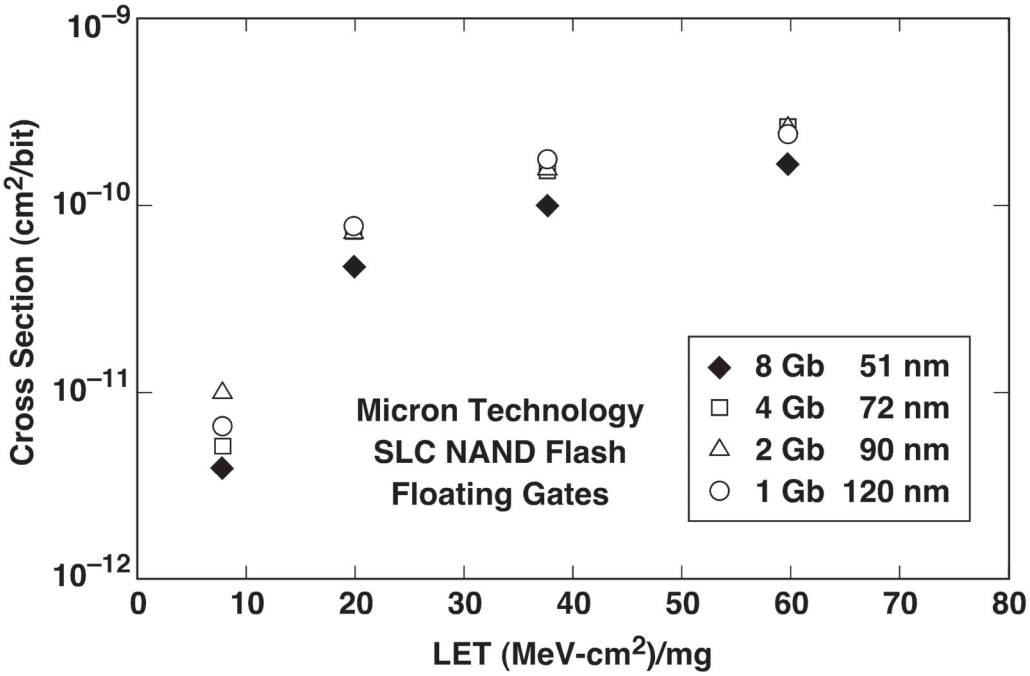

Figure 3. SEU cross sections for Micron Technology SLC NAND flash memories. Measurements were performed at BNL.

III.B SEFIs

During SEFI measurements, the beam flux was set to approximately 5×10^3 ions/cm2 per second and the DUT was irradiated until occurrence of SEFI. After occurrence of SEFI, irradiation was stopped. For each sample, three SEFIs were collected. Figure 4 shows the SEFI cross section for the Micron Technology 32-Gb MLC flash memory. The error bars are approximately 2 sigma (95%) and result from Poisson statistics. SEFIs were observed at a LET of 3.6 MeV-cm^2/mg, but

no SEFIs were observed at a LET of 1.8 MeV-cm^2/mg. The SEFI LET threshold is between 1.8 and 3.6 MeV-cm^2/mg. The SEFI rate is 2.1×10^{-4} per day per device for the background GCRs environment. The rate for the worst week CREME96 model flare is 8.4×10^{-2} per day per device, producing an accumulated number over the duration of the flare that is equal to 0.6 SEFIs per device per flare. An analysis of SEFIs was complicated because the signature, recovery mechanism, and consequence to the device operation varied greatly, depending upon exactly how the device functionality was altered. Typical SEFI events resulted in a large number of errors while trying to read the device. Some events will self-recover once the device is re-read. Other SEFIs require a power cycle and the part to be re-initialized to return to normal operations.

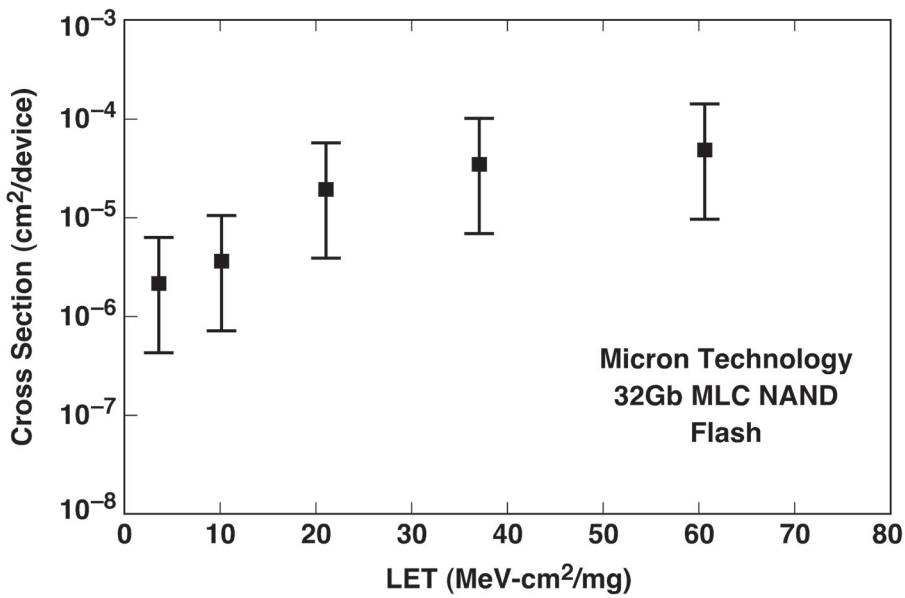

Figure 4. SEFI cross section for Micron Technology 32-Gb MLC NAND flash memory. Measurements were performed at RADEF.

III.C High-Current Spikes

The most surprising and troublesome observation in the measurements was the occurrence of relatively high-current spikes during high LET testing of high-density NAND flashes [6]. It should be noted that the destructive high-current spikes have been reported by others such as the European Space Agency (ESA) group [10], while conflicting results have been presented by others [11, 12]. The high-current spike should not be mistaken with a typical latch-up event because a latch-up is defined as a self-sustaining state. Although radiation causes the current to spike, it cannot stay in a high-current mode, and the measurements show that it lasts for about 400 ms or less. The high-current spikes were not destructive for Micron Technology NAND flash memories tested in this study in Read mode, although our measurements for Micron Technology NAND flash memories in Program mode at high LETs resulted in destructive failure (the loss of ability to erase and program the device). For 32-Gb MLC Micron Technology NAND flash memories, the high currents started at an LET around 8.3 MeV-cm^2/mg; however, high-current spikes lead to a catastrophic failure at a higher LET around 19.6 MeV-cm^2/mg. Even though the spikes themselves are transient, they produce permanent damage.

IV. TID Test Results

TID measurements were performed in Refresh and No Refresh mode. Three samples were measured.

IV.A Refresh Mode

In Refresh mode, three 32-Gb parts were irradiated at 25, 35, 45, 55, 65, 75 and 100 krad (SiO_2). One sample failed post 55 (SiO_2) krad erase; the other two samples failed erase function between 75 and 100 krad (SiO_2). Table 5 summarizes the bit error TID results, and Figure 5 displays the percentage of erroneous bits versus dose.

Table 5. Summary of TID results for Micron Technology 32-Gb MLC NAND flash memory in Refresh mode.

TID (krad)	Errors (Sample #1)	Errors (Sample #2)	Errors (Sample #3)
0	841	826	1,765
25	7,715	1,657	5,130
35	105,041	3,585	12,522
45	8,456,389	14,318	71,282
55	392,707,607	65,367	249,628
65	-	657,800	3,332,897
75	-	8,350,256	37,817,534
100	-	Failed post 100k Erase	Failed post 100k Erase

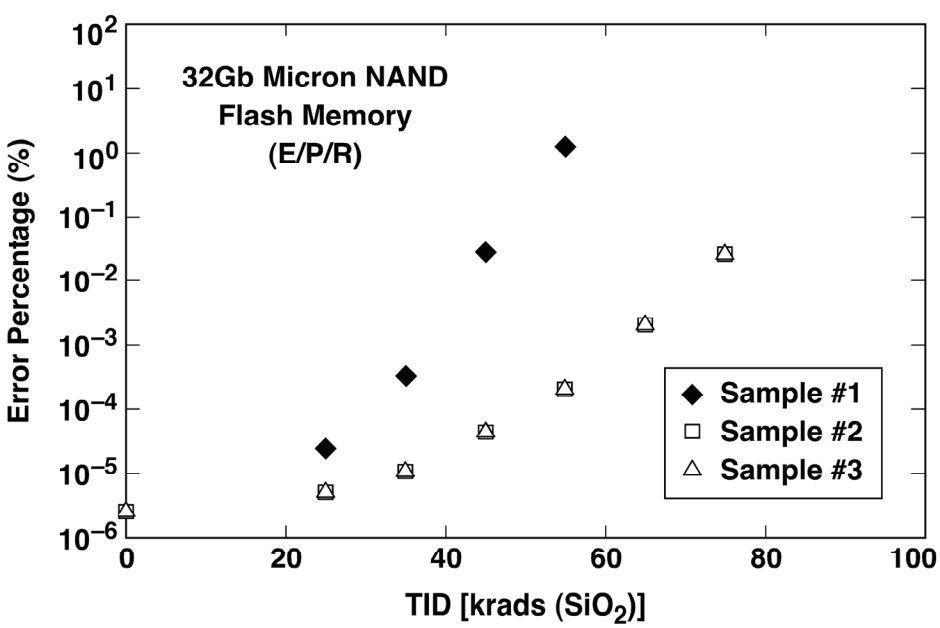

Figure 5. Percentage of bit errors versus dose for Micron Technology 32-Gb MLC NAND flash memory in Refresh mode.

IV.B No Refresh Mode

In No Refresh mode, the DUTs were subjected only to read after irradiation. Three parts were irradiated up to 85 krad (SiO_2). Table 6 summarizes the bit error TID results for three samples of 32-Gb parts. Three measurements show excellent agreement. Figure 6 displays the erroneous bits versus dose for the average of the three samples. Also shown in Figure 6 is erroneous bits versus dose for the average of three samples of Micron Technology MLC 8- and 16-Gb parts.

Table 6. Summary of bit–error TID results for Micron Technology 32-Gb MLC NAND flash memory in No Refresh mode showing separate samples.

TID (krad)	Errors (Sample #4)	Errors (Sample #5)	Errors (Sample #6)
0	704	831	549
25	50,130,130	65,352,888	54,935,938
35	409,942,059	534,208,023	506,120,988
45	1,712,575,647	1,774,942,318	1,752,592,578
55	2,054,249,657	2,218,375,152	2,185,105,314
65	763,554,436	921,808,510	894,469,873
75	77,066,549	104,433,651	113,765,287
85	26,677,830	27,909,498	36,319,728

Figure 6 shows the rapid buildup of bit errors up to approximately 55 krad (SiO_2) for the 32-Gb DUTs that had been programmed to all "0" prior to irradiation. At approximately 55 krad (SiO_2), a large number of the FGs are read as "1" (approximately 2 Gb out of 32 Gb are read as "1"). The remaining cells initially programmed to "0" are partially discharged but still read as "0." After approximately 55 krad (SiO_2), the erased cells gradually change to "0" and error percentage reduces. The rapid buildup of bit errors for 16- and 8-Gb DUTs is around 20 krad (SiO_2). This effect can be attributed to a reduction in the voltage from the charge pump during read operation because of TID damage [13]. In the NAND architecture, a FG cell is read by applying 0 V to its gate and biasing all the other cells that belong to the same series of 32 FGs to a voltage high enough to guarantee that both erased and programmed cells are turned on. This voltage is generated by a charge pump circuit during read operation. If the voltage provided by this element is lower than the design limit, some of the cells in the string will be read as programmed ("0"), regardless of their actual status. This is the likely cause of the drop in apparent number of errors around 55 krad (SiO_2) in Figure 5. Similar behavior has been reported in the x-ray TID measurements of ST Micro 1-Gb SLC NAND flash memory [13].

The standby current measurements for 32-Gb samples used in Refresh mode and No Refresh mode measurements are summarized in Table 7, and the standby current versus the dose for Refresh and No Refresh Modes is displayed in Figure 7. There is excellent agreement between results.

In No Refresh mode, Co-60 irradiations were performed on Micron Technology SLC 1-, 2-, 4- and 8-Gb devices up to 80 krads (SiO_2). Table 8 summarizes the average bit error TID results of three samples for each device. Figure 8 displays the average percentage of erroneous bits versus

dose for three sample measurements for each device. For a particular TID level, the number of errors decreases with increased density.

Figures 9 and 10 compare the results of standby current versus dose for Micron Technology 1-, 2-, and 4-Gb SLC NAND flash memory in No Refresh mode and Refresh mode, respectively. Standby current improves with scaling for both cases.

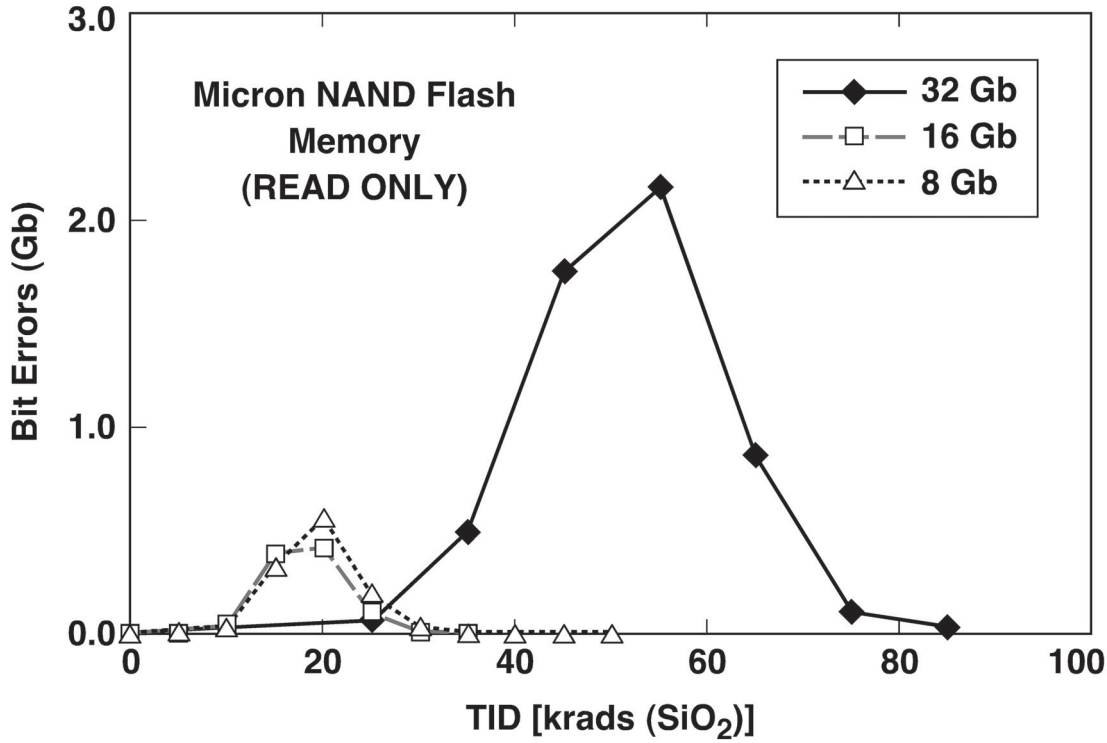

Figure 6. Bit errors versus dose for Micron Technology MLC NAND flash memories in No Refresh mode.

Table 7. Summary of standby current versus dose for Micron Technology 32-Gb MLC NAND flash memory. Samples 1–3 were operated in Refresh mode and samples 4–6 in No Refresh mode.

TID (krad)	Standby Current (μA) (Sample #1)	Standby Current (μA) (Sample #2)	Standby Current (μA) (Sample #3)	Standby Current (μA) (Sample #4)	Standby Current (μA) (Sample #5)	Standby Current (μA) (Sample #6)
0	7.16	7.96	8.07	7.81	7.02	7.25
25	18.64	17.97	16.74	20.11	20.11	19.76
35	23.34	22.04	22.12	23.09	22.18	22.43
45	24.96	25.94	25.94	29.51	24.75	27.59
55	30.04	26.99	29.97	33.17	30.33	29.16
65	38.33	30.68	33.38	37.39	32.75	32.46
75	-	33.12	36.15	38.54	38.43	38.47
85	-	-	-	44.19	39.87	41.98
100	-	53.91	49.67	-	-	-

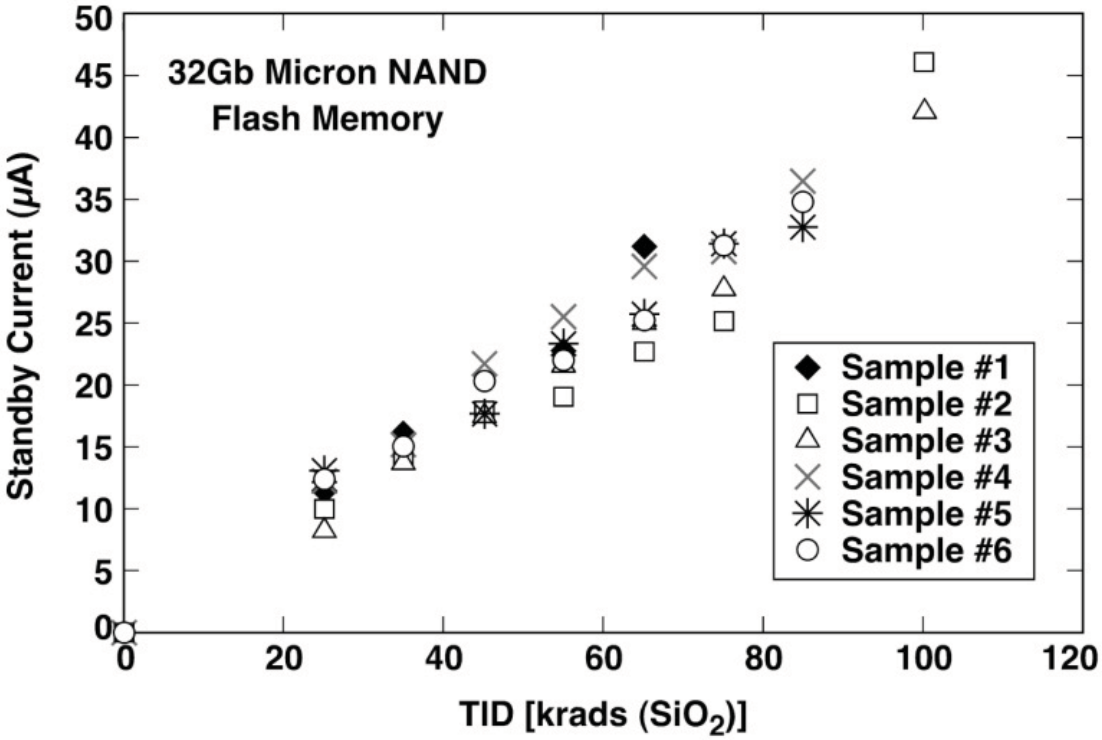

Figure 7. Standby current results versus dose for Micron Technology 32-Gb MLC NAND flash memory in Refresh and No Refresh modes. Samples 1–3 were operated in Refresh mode and samples 4–6 in No Refresh mode.

Table 8. Summary of bit error TID results for Micron Technology 1-, 2-, 4-, and 8-Gb NAND flash memory in No Refresh mode averaged over three samples.

TID (krad)	Errors 1Gb	Errors 2Gb	Errors 4Gb	Errors 8Gb
0	0	0	0	0
10	0	0	0	0
25	-	108	2	43
30	1,063	-	-	137
35	-	-	-	2,844
40	1,498,107	1,048,024	1,102	-
50	145,557,656	528,616,073	113,089	-
60	276,057,030	1,174,465,793	11,458,731	-
65	766,853,454	1,464,210,083	119,384,795	-
70	1,028,052,213	1,284,552,054	-	-

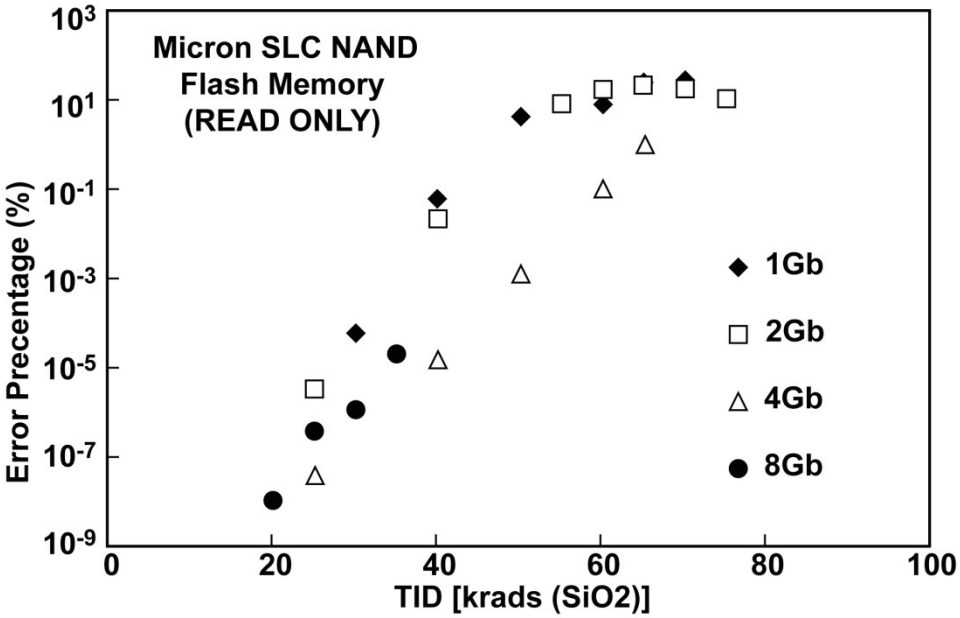

Figure 8. Percentage of data errors versus dose for Micron Technology 1-, 2-, 4- and 8-Gb SLC NAND flash memory in No Refresh mode averaged over three samples.

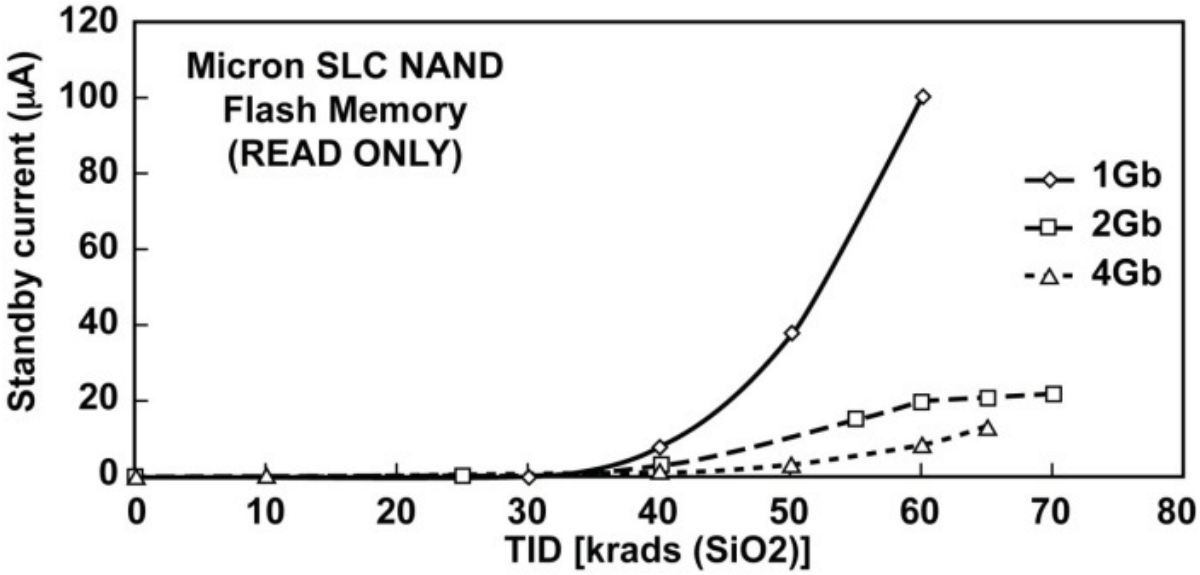

Figure 9. Standby current results versus dose for Micron Technology 1-, 2-, and 4-Gb SLC NAND flash memory in No Refresh mode.

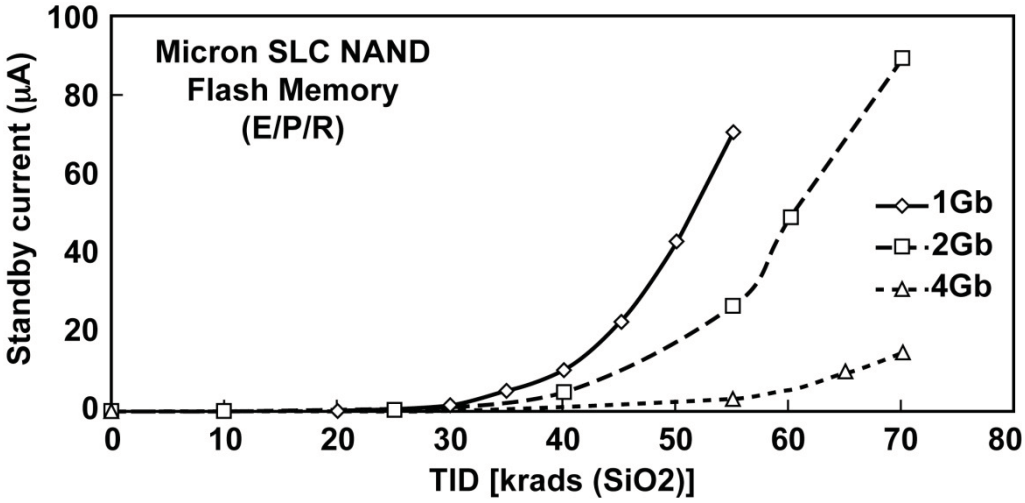

FIGURE 10. Standby current results versus dose for Micron Technology 1-, 2-, and 4-Gb SLC NAND flash memory in Refresh mode.

V. Discussion

Interpretation of radiation tests in the new generation of flash memories is difficult because of the very involved architecture and internal circuitry. In new advanced flash memory technology, the cells are n-channel transistors, where the FG is filled with electrons in the zero state, and empty of electrons in the one state. Since the effect of radiation is to introduce positive charges into the oxide, radiation tends to turn zeros into ones, but not the reverse. In the heavy ion tests, all the single bit errors in the FGs are zero-to-one errors. SEUs in flash memories also occur in the microcontroller, buffer, and register regions, causing complex errors at the block level as well as address errors [1, 4, 5].

The number of induced SEUs experienced by a semiconductor device such as a memory in a given radiation environment depends primarily on its threshold for upsets (usually given by the critical charge Q_c or critical LET) and the total device volume sensitive to ionization. As a heavy ion transits through the sensitive volume of a device, it creates electron-hole pairs along its ionization track. The original charge collection modeling postulated that the charge deposited in a depletion layer of the effected device would be collected rapidly by drift and the remaining charge more slowly by diffusion [14]. An effect not taken into consideration by this model, which made the SEU a more serious problem, is the funneling effect. Taking the funneling phenomenon into consideration, more charge would be collected at the struck node and less at the surrounding nodes. If Q_c is within the indicated range, an upset would occur because of the funneling effect, which increases charge collection at the target node.

Because of the scaling and reduced feature sizes, the advanced high density memories have smaller area capacitors and hence lower critical charges. The critical charge is device dependent and can vary from 0.005 to about 2.5 pC. In general, for unhardened devices, the critical charge decreases with reduced feature sizes and it follows the l^2 scaling rule [15]. Considerable work has been done showing that the critical charge for scaled devices is expected to be lower for more advanced devices [16]. This often leads to the conclusion that SEU will be far more severe for highly scaled devices. However, this has not been observed for high-performance devices such as memory devices [17]. Other factors such as decrease in charge collection depth as well

as by device architecture cause less charge to be collected as devices are scaled to smaller feature size. In the case of commercial processes, the threshold LET has changed very little with scaling. However, the per-bit saturation cross section has steadily decreased with smaller feature size [9].

Similar conclusions have been reported in [18] for scaling effects on SRAMS. The article concluded that error rates would not increase much with scaling. Although the critical charge decreases with scaling, in [18] it is pointed out that the charge has to be deposited in a sensitive volume that has also gotten smaller. To the first order, these effects approximately offset each other, which means that approximately the same LET is required for an upset, even though the charge is less. In turn, this means the error rate will vary only slightly.

Results presented in this paper indicate no noticeable changes in SEU cross sections for the Micron Technology 1-, 2-, 4-, and 8-Gb SLC NAND in the range of 120–72 nm feature size; however, there is a reduction in the SEU cross section at high LETs for 51-nm feature size devices. This indicates that scaling effects is effective below certain feature size, in this case below 72 nm.

The 32 MLC parts were irradiated up to 85 krad (SiO_2), and the charge pump was still functional at high dose levels. This is an improvement compared to the older generation of flash memories in which the charge pump failed at about 10 krad (SiO_2). There is an interesting feature in our No Refresh mode TID measurements of Micron Technology MLC 32-Gb NAND flash memory, which shows a drop in number of bit errors after approximately 55 krad. A drop in the number of bit errors for the Micron Technology MLC 16- and 8-Gb NAND flash memories occurs after approximately 20 krad. These results indicate that the degradation in the VTH follows the scaling trends. Also, in these measurements a standby current improves with scaling.

VI. Conclusion

We tested the advanced, commercial, high-density 1-, 2-, 4- and 8-Gb SLC NAND flash memories from Micron Technology with heavy ions and LET range of 0.1–60 MeV-cm^2/mg. The FG SEU cross section does not scales with feature size, except for SLC 8-Gb devices, which are built with 51 nm feature size, and are about 60% smaller than the FG SEU cross section for 1-Gb devices, built with 120 nm feature size at high LETs. There is no scaling effect in the range of 120–72 nm feature size. No change in threshold LET was noticed in the range of 120–51 nm feature size. TID measurements on 1-, 2-, 4-, and 8-Gb SLC NAND flash memories from Micron Technology indicate that standby current and data error percentage improve with scaling.

We performed heavy ion measurements with LET range of 0.1–60 MeV-cm2/mg on 32-Gb MLC NAND flash memory from Micron Technology with normal incident as well as horizontal rotations of ±30 and ±60 degrees and a vertical rotation of +60 degrees. The measurements at angles indicate that device susceptibility follows the Cosine law, but there is some uncertainty because a complete set of angle tests was done with only one ion species. Also, we studied TID response of 8-, 16- and 32-Gb MLC NAND flash memories from Micron Technology. These parts were irradiated up to 85 krad (SiO_2). For the 32-Gb devices, the charge pump was still functional at high dose levels. This is an improvement compared to the older generation of flash memories in which the charge pump failed at about 10 krad (SiO_2). There is an interesting feature in our No Refresh mode TID measurements of Micron Technology MLC NAND flash memories: It shows a drop in the number of bit errors after a certain dose level, which depends on the feature size. For 32-Gb MLC, the TID level is about 55 krad, and for 8- and 16-Gb devices, it is about 20 krad.

VIII. References

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