



FPGA NEPP FY10 Summary Report

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ABSTRACT

This report documents the activities and results of the fiscal year 2010 (FY10) funding for the NASA Electronic Parts and Packaging (NEPP) program for reprogrammable field programmable gate arrays (FPGA).

The FY10 task was divided into three efforts as listed below:

1. Physics of failure for the Xilinx Virtex-4 Non-Hermetic, Ceramic, Flip-Chip Column Grid Array Package.
2. Continuation and completion of the IDDQ Study of the Actel A54SX FPGA
3. Actel Flash FPGA Technology

The FY10 NEPP FPGA study was organized into these three efforts in recognition of the continued and increasing importance of FPGAs to NASA. FPGAs represent the state of the art in electronic components with millions of transistors integrated into a single device. Modern NASA spacecraft design has dozens of FPGAs implemented onboard. FPGAs are used in a number of areas, including critical command and data handling, instrument control and monitoring, and communications protocols. Therefore, the reliability of FPGAs is fundamental to mission success for NASA.

1.0 PHYSICS OF FAILURE OF THE XILINX VIRTEX-4 NON-HERMETIC, CERAMIC, FLIP-CHIP COLUMN GRID ARRAY PACKAGE

The Virtex-4 from Xilinx uses a new type of non-hermetic package—a ceramic, flip-chip design for column grid array. This unique design was required to accommodate the very large Virtex-4 die (540 mm²). There is no wire bonding and the entire top of the die is contacted via Pb-Sn bumps. Eliminating wire-bond wires improves the inductance and capacitance of the electrical connections. The flip chip also allows the entire die surface to be used for power, input/output (I/O), and ground signals.

The introduction of this new package type for space missions marks a significant technology milestone for NASA missions. Historically, NASA semiconductor technology has remained several generations behind state-of-the-art commercial devices. This mostly has to do with radiation requirements and hermetic packaging requirements. This Virtex-4 device is made with 90 nm complementary-metal-oxide-semiconductor (CMOS) processing, first introduced commercial in around the year 2001.

The Virtex-4 is an example of the size and capability that the 90 nm node provides, however. The Virtex-4 is the most power field programmable gate arrays (FPGAs) have offered for space applications. It has 200,000 logic cells, up to 512 DSP slices, 400 MHz clocking, and 800 Mbps differential I/O. There are three different parts in the Virtex-4 family that are optimized for logic, signal processing, and embedded performance, respectively. Table 1-1 provides a summary of the Virtex-4 capabilities. The use of the flip-chip, non-hermetic, column grid array devices is a fundamental next step in electronic packaging for future space missions. Xilinx Virtex-4 devices will not be the only devices that use this type of packaging. Custom rad hard by design ASICs made from 90 nm commercial foundries will also require this type of packaging, again due to the large and sophisticated nature of the die.

The International Technology Roadmap for Semiconductors (ITRS) report on assembly and packaging trends identifies electronic packages as a convergence of multi-scale, multi-physics, multi-materials, and multi-materials interface systems. The length scale varies from nanometers to centimeters, and a wide range of materials with mechanical properties from stiff and brittle inorganics like silicon, glass, and other dielectrics with property modifications such as micro-pores to achieve low- κ , to softer materials like solders or polymers and polymer composites that have combined non-linear time and temperature-dependent material behaviors.

Table 1-1. Summary of Xilinx Virtex-4

	XQR4VLX200	XQR4VX55	XQR4VFX60	XQR4VFX140
Slices	89,088	24,576	25,280	63,168
Logic cells	200,448	55,296	56,880	142,128
CLB flip flops	178,176	49,152	50,560	126,336
Max distributed RAM (kb)	1,392	384	395	987
Block RAM/FIFO	336	320	232	552
Total block RAM (kb)	6,048	5,760	4,176	9,936
Single-ended I/O	960	640	576	896
Differential I/O	480	320	288	448
DSP slices	96	512	128	192
Configuration memory (Kb)	51.4	22.7	21	47.9
CF1144			576	
CF1140		640		
CF1509	960			768

As scaling is continually reducing transistor size, packaging technologies are being affected. For example, scaling demands are currently driving bump size and pitch. As bump size decreases, the bump becomes less compliant because of the geometry, making it more susceptible to thermal- and mechanical-driven failure modes such as fracture. Bump scaling can also drive the use of new materials, which in turn may introduce a new set of reliability challenges as a result of a change in basic material properties.

These changes in material properties influence interface effects, grain size, and pre-stresses due to process or adjacent materials. Properties of materials such as intermetallics form from solder under-bump metallurgy (UBM) metals interaction, which grow and evolve over time and temperature. Physical failure mechanisms such as electromigration and thermal migration in combination with mechanical stresses will need to be understood and modeled for practical mission life assessment.

The non-hermetic, flip-chip column grid array package is a very complex mechanical / electrical system that will have non-standard failure mechanisms and require additional testing and screening to ensure successful insertion into NASA missions. The remainder of this section discusses the package test data to date and provides additional new data regarding physics of failure for this particular package.

Figure 1-1 shows a cross sectional schematic of the Virtex-4 package. Table 1-2 shows the critical components of the Virtex-4 package, and summarizes the physics-of-failure information for all new portions of the Virtex-4 package. Statistically based life tests that highlight the various failure mechanisms are a fundamental component of any modern technology qualification.

Xilinx has not provided statistical time-to-failure data for all of these possible mechanisms. These data may exist with IBM as they were the original developer of the packaging technology and continue to be the vendor that provides this to Xilinx. Without such experimental data, it is difficult to accurately predict time to fail and hence practical lifetimes. These lifetimes allow mission planner and component engineers the ability to precisely determine the amount of margin for a given environmental and operational set of conditions. This report will approximate these physics-of-failure results based on what testing has been accomplished.

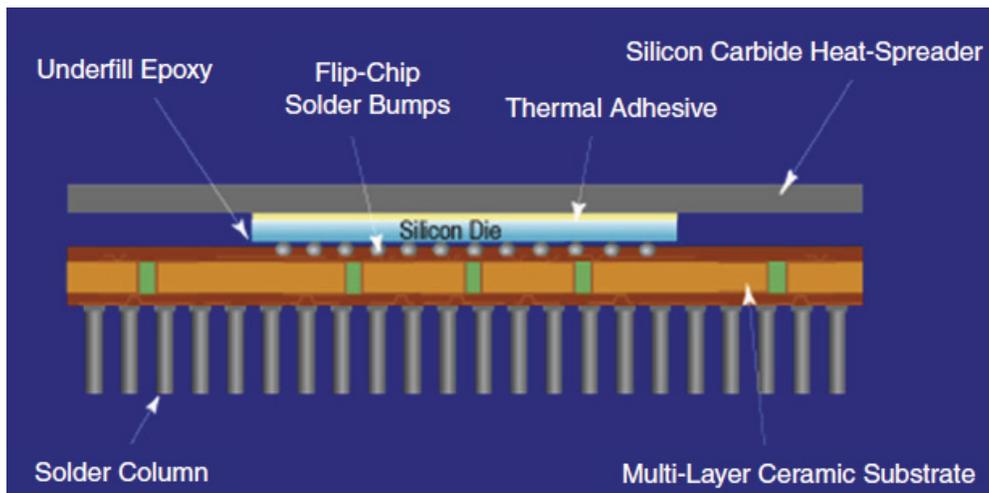


Figure 1-1. Cross sectional drawing of Xilinx V4 package

Table 1-2. Summary of specific new technology assemblies of the Virtex-4 package

Assembly	Failure Mechanisms
Solder bumps	Electromigration, interdiffusion
Underfill epoxy	Moisture penetration
Thermal adhesive	Adhesion
SiC heat spreader	Adhesion
Multi-layer ceramic substrate	Cracking
Solder columns	Metal fatigue

1.1 Historical Review

Literature review shows that development of this packaging technology began around year 2000. It was based on a series of requirements for a family of high availability core routers. Six custom very large scale integration (VLSI) devices using large flip-chip column grid array (FCCGA) packages with large devices were required [1]. The detail of each of these VLSI devices is published and has been graphed in Figure 1.1-1. The number of I/Os for each device is shown on the left hand y-axis while each device's power output in watts is plotted on the right hand y-axis. The devices show a predictable trend of increasing I/O count with increasing die size. As the die size approaches 450 mm², the power begins to range from 40 to 80 watts. This significant amount of power from 180 nm generation ASICs would be a reliability and system concern if these types of devices were in fact used on a NASA mission.

Figure 1.1-1 also shows the die size and I/O values for the Xilinx Virtex-5 (65 nm) single-event, immune-reconfigurable (SIRF) FPGA device to provide an understanding of the I/O requirements and power demands initially placed on the packaging technology. Power requirements are particularly critical because high reliability space missions often require restrictions on junction temperature and final system power. These power values are high in fact when compared to the normal amount of power desired for a space based FPGA. This is an early positive indicator that the technology can "handle" more than NASA may subject it to. This type of condition of course implies a derating margin. However, it remains to be confirmed that such a derating margin actually exists.

Integrated circuit (IC) technology has changed significantly from 180 nm to 90 nm and then on down the current 32 nm process. Of interest to this paper is that the dielectric materials and interconnect metals have changed completely from the ones used on the original IBM process. All of these changes affect the physics of failure. For example, modern low-k materials have lower modulus, lower fracture toughness, and poorer adhesion compared to historical dielectric materials. Thermoelectric failure risk goes up as a result. It is important to comprehend these material changes in detail rather than simply state "IBM has been making these packages for years." The assumption is that as IBM's technology will continue to shrink in feature size down past 90 and 65 nm that this package technology will continue to be modified as well. Most of the data presented to date has shown devices passing all parts tests. However, there is little statistical physics-of-failure information available.

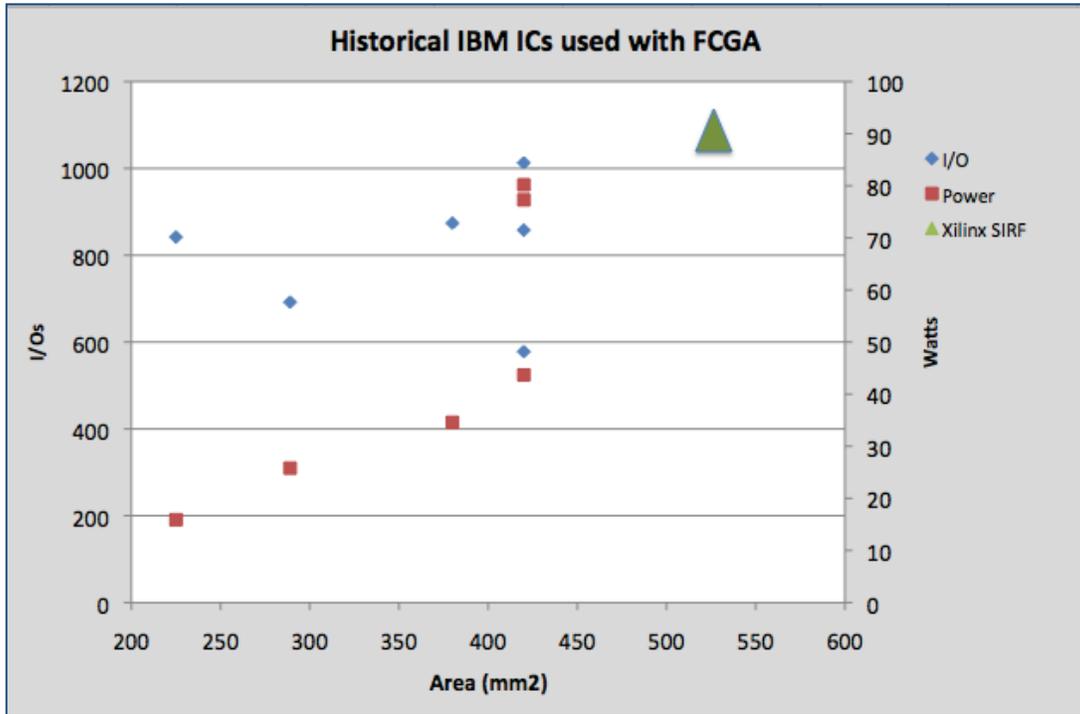


Figure 1.1-1. I/O and power for IBM router ICs using flip-chip CGA packages

1.2 Destructive Physical Analysis

A sample of the CF1144 package from Xilinx was obtained and a destructive physical analysis performed. The analysis focused on optical and scanning electron microscope (SEM) photos and some X-ray elemental analysis with energy dispersive analysis of x-rays (EDAX). The silicon die was a daisy-chain test die. A top view of the package is shown in Figure 1.2-1.

Figure 1.2-2 shows a side view of the package. This picture shows several points of concern. A pin hole in the underfill can be seen in right of the photo near the eighth column from the right. The edges of the die also appear to be visible near the third column from the right and the second column from the left.



Figure 1.2-1. Top view of CF1144 package



Figure 1.2-2. Side photo of CF1144 package



Figure 1.2-3. Top-down view of the CF1144 package with heat spreader removed

These types of visual defects point to manufacturing inconsistencies. This package should be rejected if it were to be part of a normal flight build. Additional concerns with the package can be seen in Figure 1.2-3. This is a top-down view with the silicon carbide heat spreader removed. The die is seen to be placed to the right-hand side of the cavity and not centered in the cavity as it should be. This placement leads to non-uniform epoxy, as there is an excess of epoxy on the left-hand side and almost no epoxy on the right-hand side. The top of void appears near the bottom side of the die at about 7 o'clock.

These preliminary visual inspections reveal poor quality control of die placement and underfill consistency. This occurred on just one random sample that was purchased through a third party (not directly from Xilinx). As a result of these findings, it is strongly recommended that a similar destructive physical analysis (DPA) be performed on a much larger sample size of these daisy-chain parts. The sample should encompass a variety of lots and different assembly dates to determine if there are any systematic errors in the process or if the results obtained from this sample are outliers. A recent audit [2] of the IBM Bromont facility revealed several weaknesses in their statistical process control (SPC) and MIL-PRF-38535 capabilities that required improvement.

Figure 1.2-4 is a transition SEM photo of the die, bumps, and vias to the substrate. This photo is provided to show the change in scale between the optical resolution and SEM resolution.

Figure 1.2-5 is a more detailed photo of the bump and via. There is some misalignment between the via and the interconnect layer as the via appears to be shifted to the left and is not completely parallel to the top of the via opening.

These misaligned via also represent a long-term reliability concern because of the right angle that is formed, which will lead to current narrowing and increased electric fields. Figure 1.2-5 also shows the different layers of the substrate. The bump is surrounded by circular filler material while the via is in a metal layer. Figure 1.2-5 is a close up of the bump itself, where the metal layers of the die can be seen at the top. The die is upside down, the base silicon layer is on top, and the bump connects to the metal layers.

The different spherical sizes of the filler material are readily apparent in this picture with an average size of approximately 10 μm . Some of these filler spheres were embedded into the soft bump material and their round shapes have been transferred to the bump. The round dots seen on the bump are not voids in the bump material.

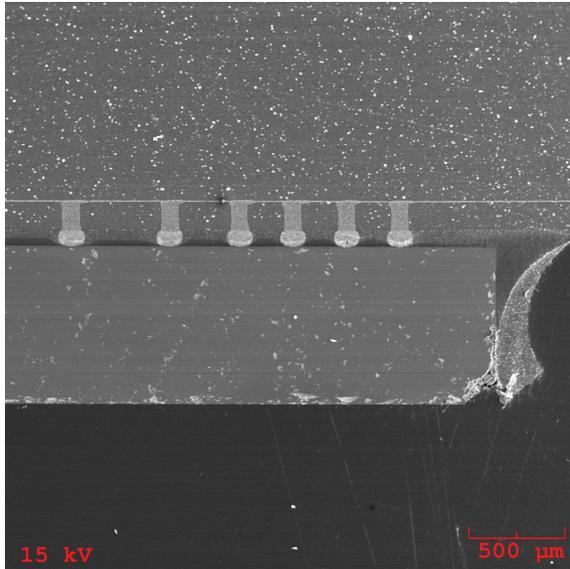


Figure 1.2-4. Long-range view of bump and vias

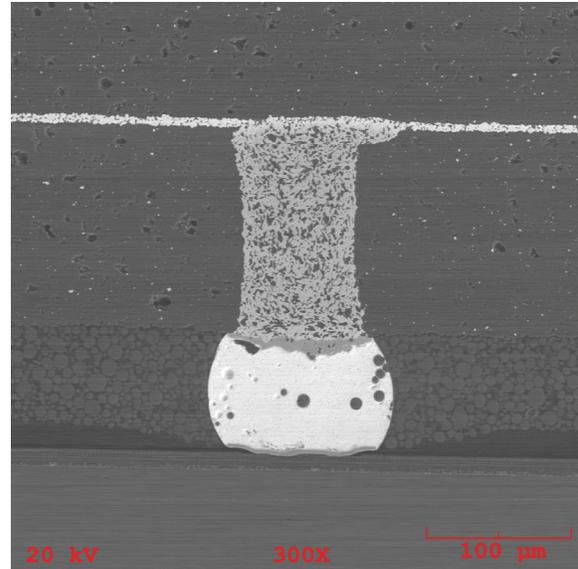


Figure 1.2-5. Bump and misaligned via

Figure 1.2-6 also highlights two important transition layers, one on the top of the bump near the die and the other on the bottom of the bump as it transitions into the via. On the bottom of the bump, an interdiffusion region can be seen forming, connecting the bump to the via. On the top of the bump is an additional intermetallic layer that highlights the UBM layer. The UBM generally consists of successive layers of metal with functions described by their names. The “adhesion layer” must adhere well to both the bond pad metal and the surrounding passivation, providing a strong, low-stress mechanical and electrical connection. The “diffusion barrier” layer limits the diffusion of solder into the underlying material. The “solder wettable” layer offers an easily wettable surface to the molten solder during assembly, for good bonding of the solder to the underlying metal. A “protective layer” may be required to prevent oxidation of the underlying layer.

Figure 1.2-7 shows the results of an X-ray fluorescence (XRF) analysis on this SEM sample. The XRF allows for elemental decomposition. At the bottom of Figure 1.2-7 is the color key for reference. The combined XRF/EDS analysis allows a single SEM image to be split into its constituent elements while the image is reproduced to show only the element selected. The original SEM picture is at the top left. The bright green picture in the third column shows the areas of aluminum (Al), for example. Aluminum appears mostly in substrate. The dark blue is silicon (Si) that appears in the filler material and the silicon substrate of the die. Nickel (Ni) is shown in yellow and is quite prominent at the two bump interfaces. Note, there is no Ni interdiffusion into the main body of the bump.

Lead (Pb) only appears uniformly distributed throughout the bump. The bumps used for the Virtex-4 are high lead bumps (95% Pb/5% Sn). The purple titanium (Ti) layer appears as an adhesive layer between the silicon die and the bump.

The XRF analysis shows the elemental distribution to be as expected. This would form a baseline for temperature-based testing. Once the temperature testing is concluded, a similar bump SEM sample would be prepared and this XRF analysis performed. Any noticeable differences in movement or location of elements could then be identified.

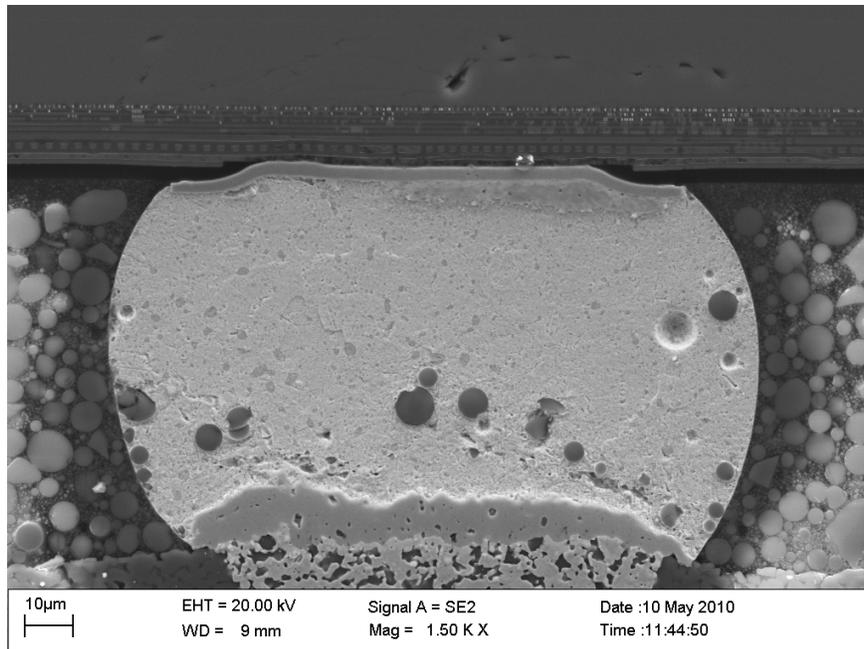


Figure 1.2-6. Close-up of bump; die-level interconnect can be seen at top

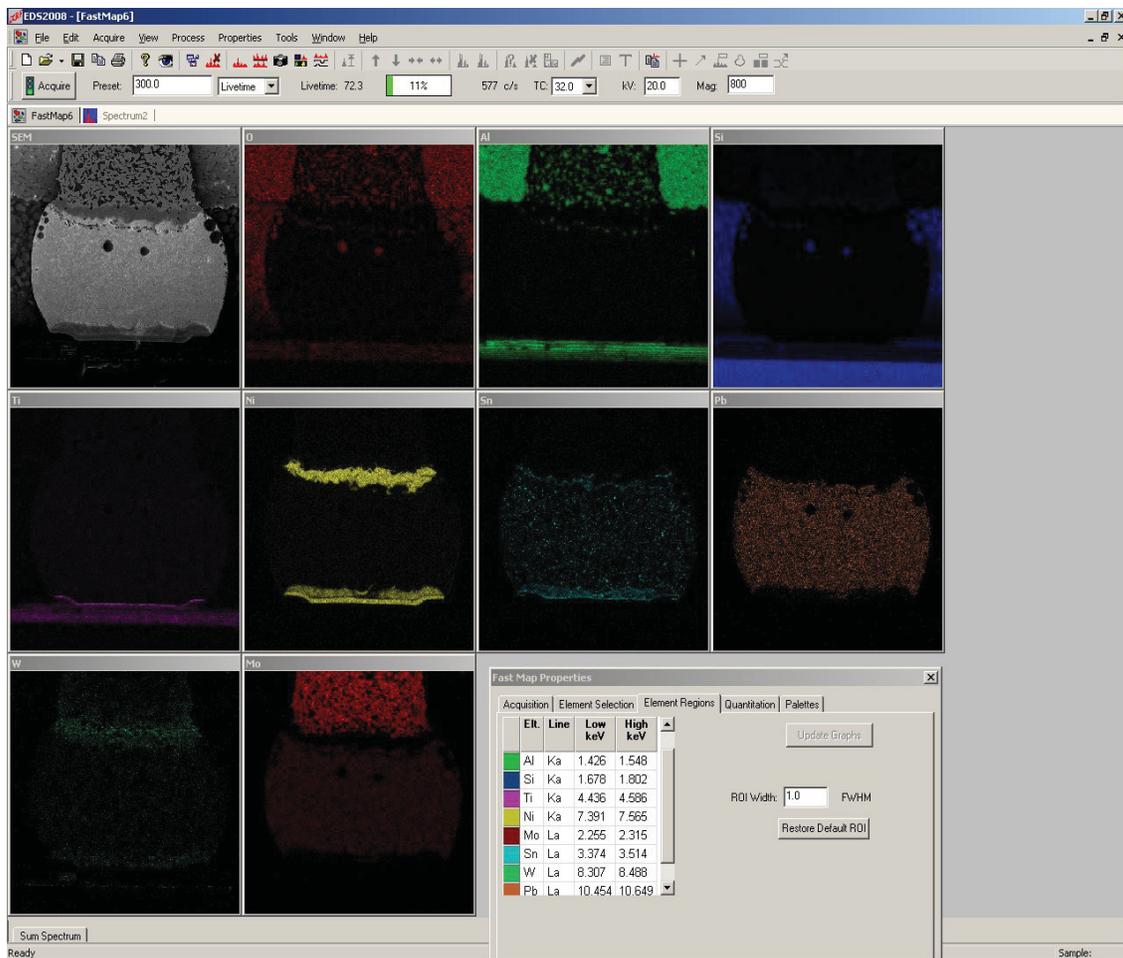


Figure 1.2-7. XRF elemental analysis of bump SEM; note elemental color key on bottom

1.3 Physics of Failure

Because of the limited availability of statistically based physics-of-failure testing, this section only provides a discussion on some of the overall mechanisms. Figure 1.3-1 shows a schematic drawing of the possible failing areas for this flip-chip technology.

Bump electromigration is an important reliability concern for this type of advanced packaging technology. Bump size scales with technology generation. Ball diameters now vary from 40 to 100 μm . A 100 μm ball diameter with 200 mA of current has an approximate 2,500 A/cm^2 current density for example. Although this current density is 1 to 2 orders of magnitude lower than that in the on-chip interconnects, electromigration failure of solder balls can become an important reliability problem for high-density, flip-chip packages, considering that solder alloy has a low melting point and relatively high atomic diffusivity at operating temperature. This is why bump electromigration needs to be addressed as part of an overall package qualification scheme.

Electromigration of solder bumps is a failure mechanism that leads to increased resistance. Bump electromigration can also lead to formation of intermetallic compounds, voids, and cracks that can disrupt the solder joint and the silicon and package metallization leading into the bump. The resistance increase can ultimately lead to an open circuit. The stress drivers for this failure mechanism are current density and elevated temperature. The failure mechanisms for bump electromigration can be varied and depend on the metals present both on the silicon side and the substrate side.

While the on-chip Al or Cu interconnects are usually a single-element system, the solder ball, on the contrary, is a binary or ternary alloy system. The solder material reacts with the ball-jointing metallurgy, which contains by itself thin layers of different metals. This leads to complex metallurgy reactions and intermetallics compound formation, which is further complicated by fast diffusion of certain metals, such as Cu and Au in solder under the driving force of the current. The material reactions and chemical potentials built up in the solder metallization give rise to complicated kinetics and mass transport leading to distinct electromigration failure mechanisms in solders [3].

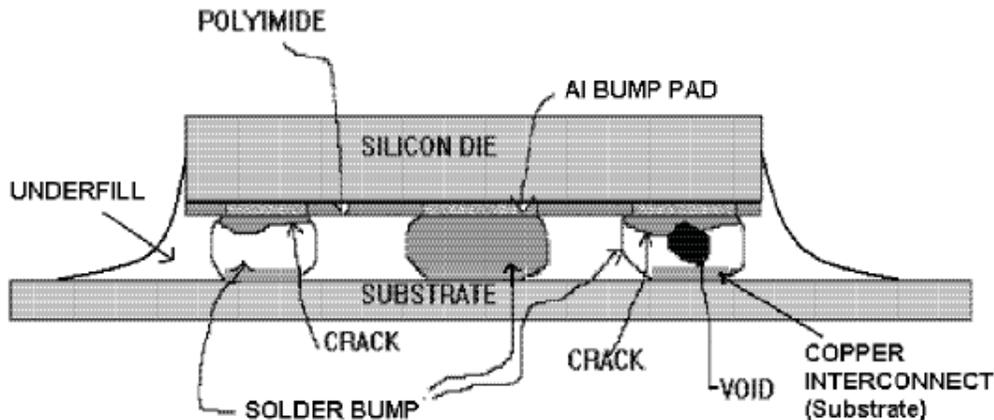


Figure 1.3-1. Failure areas in flip chip [3]

There is a JEDEC specification for electromigration of bump testing, JEP154. Black's equation for electromigration in metal lines is still valid for use in bumps. This equation is shown below:

$$(1) \quad TTF \propto J^{-n} e^{\frac{E_a}{kT}}$$

This equation contains a model parameter relating to temperature (T): the thermal activation energy, E_a . It also contains a model parameter relating to current density (J): the current density exponent, n. Bump electromigration is measured using a constant current source with a constant temperature on a four-point probe test structure. A pre-determined amount of resistance change is considered to be a failure.

As stated in JEP154, bump electromigration is strongly dependent on several factors. These include the following: bump composition, bump fabrication method (e.g., electroplated, printed paste, or evaporated), composition of the UBM on the silicon, the UBM layer thicknesses, and the substrate type. The semiconductor die metallization, passivation or repassivation composition, and test structure details, including via openings and design features, may also have a significant effect on Joule heating and current crowding. Bump geometry and structures can affect bump EM performance based on effects of current crowding.

Figure 1.3-2 shows an example of bump electromigration. This effect of bump material is dramatically evident with the characteristic lifetime of the high lead concentration bump six times longer than the bump made with only 63% lead.

One of the main disadvantages of using bumps is that the connections are quite stiff. This means the thermal expansion of the chip must closely be matched to the connecting material or there is a high risk of cracking. The difference in the coefficient of thermal expansion (CTE) between the chip and the substrate often makes flip-chip configurations vulnerable to thermally induced strains and often results in solder bump failure. Filling the space between the silicon die and substrate with underfill encapsulant mechanically couples the CTE mismatched chip and substrate and provides a significant (at least one order of magnitude) enhancement in solder joints reliability.

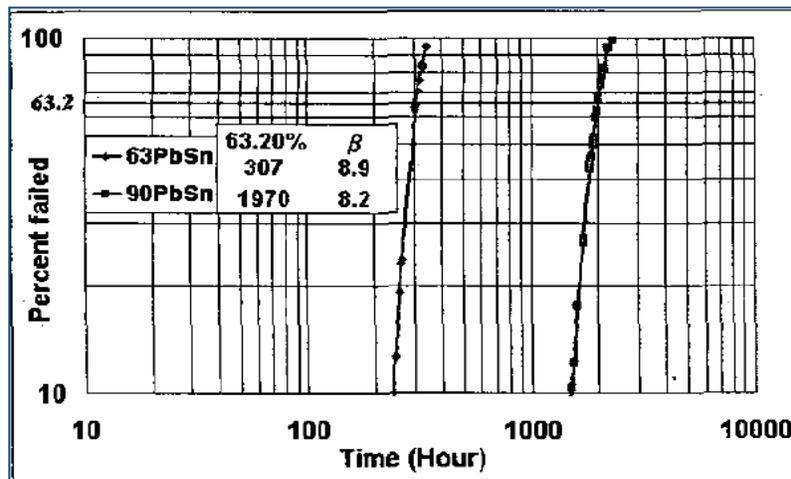


Figure 1.3-2. Bump electromigration 160 mA/160°C [4]

The failure mechanisms of advanced flip-chip interconnects are dependent on the structures and materials of ball-limiting metallurgy associated with the die and top-surface metallurgy. The most predominant failure mechanisms are solder joint fatigue, interdiffusion, creep, underfill delamination, and electrochemical corrosion. Any thermal expansion coefficient mismatches between the silicon die, underfill (with filler and without filler), and the substrate causes shear displacement at each solder joint interconnect, which may lead to thermal fatigue failure during thermal or power cycling.

Underfill was developed as a means to relieve strain in the solder bumps. Underfill is an organic material or a polymeric material that can be mixed or filled with inorganic material (e.g., fused silica, etc.). This underfill encapsulant dispensed by capillary action to fill the gap between the chip and the substrate was a major breakthrough in the early 1990s [5]. The encapsulant served as a compliant buffer reducing the shear strain of the solder balls by coupling the thermal mismatch into bending of the substrate, resulting in a significant improvement of the fatigue life of the solder balls. This provided a breakthrough in packaging development, making it possible to design plastic flip-chip packages to meet the requirements of high I/O counts and large chip size for deep submicron technology.

Although the use of the underfill encapsulant eliminates to a large extent the problem of low-cycle solder fatigue, a number of reliability issues remain. The first is interfacial cracks induced by material reaction during solder reflow between the solder and the top and bottom metallization layers [6]. The second is that the underfill layer shifts the local shear strain from the solder balls to the underfill die and the underfill/substrate interfaces, causing delamination of these interfaces to become a major concern for the structural integrity of the package. Finally, the requirements for the underfill properties become more stringent because of increasing I/O density and decreasing gap height, demanding good flow and thermomechanical matching to the die and the substrate [7].

Fused silica is often a candidate filler material due to its compatibility with silicon die, coefficient of thermal expansion, chemically inert/corrosion resistant, thermally conducting, and also its favorable dielectric properties. The filler provides the strength in the composite polymer, and the resin bonds the die and the substrate. Paralynes, silicones, silica-filled epoxy resins may be used as underfills. These underfills may be tailored to a desired glass transition temperature, elastic modulus, and CTE match to the solder materials.

1.4 Xilinx Qualification

Xilinx has conducted a qualification and analysis of the CF1144 style package. The details of the Xilinx qualification testing have been presented elsewhere [8]. An overview of the qualification approach is shown in Table 1.4-1.

Table 1.4-1 shows that there are five main features to the Xilinx qualification. The five different aspects of the qualification are based on five different standards or organizations. A series of tests has been based on military standards, commercial JEDEC standards, American Society for Testing Materials, Xilinx internal, and finally, a collaboration of Xilinx and Aerospace Corporation. Table 1.4-1 is presented to show that Xilinx has completed testing beyond a simple military standard series of tests.

Figure 1.4-1. Overview of Xilinx CF package series qualification

Test Method	Test
MIL-STD-883	Group A Group B Group C Group D Group E
JEDEC	Moisture Temp cycle
ASTM	Outgassing
Xilinx	Wear out / mask qual
Xilinx & Aerospace	Assembly, bump, die, temp cycle

The first is based on MIL-STD-883 testing and qualification for all the groups, from A to E. Group A and B reflect tests that are done on samples from each delivered lot while Groups C and D are done periodically. Inside the groups there are different levels of testing, depending which level, space, or military standard is desired.

The issue of moisture penetration of the non-hermetic package is a major concern. Xilinx has chosen to address this by performing a JEDEC-based moisture sensitivity test. This testing was done according to JEDEC J-STD-020A. The stated purpose of this document is “to identify the classification level of non-hermetic solid state surface mount devices (SMDs) that are sensitive to moisture-induced stress so that they can be properly packaged, stored, and handled to avoid damage during assembly solder reflow attachment and/or repair operations” [9]. The specification is specifically focused on short timeframe issues of package integrity during solder operations. However, NASA is also concerned about the long-term moisture resistance of this package design. This specification does not address this concern.

The Xilinx package is rated at the highest moisture sensitivity level, MSL 1. This means that the part is considered to have an unlimited floor life and does not require a dry pack for storage. The part has passed a 168 hr 85°C/85% RH test to obtain this level.

This JEDEC standard is practically designed for plastic packages that are the mainstay of the commercial electronics industry. The physics-of-failure driving force behind the standard is the concept of vapor pressure. The vapor pressure of moisture inside a non-hermetic package increases greatly when the package is exposed to the high temperature of solder reflow. Under certain conditions, this pressure can cause internal delamination of the packaging materials from the die and/or lead frame.

Vapor pressure needs to be separated from moisture diffusion, however. The two concepts are not the same. Modeling of flip-chip ball grid array (BGA) devices [10] has shown that vapor pressure saturates much faster than moisture diffusion. For plastic materials such as mold compound, the saturated moisture concentration is a few orders larger than the corresponding saturated ambient water vapor density. The saturated water vapor density is defined by a moisture precondition cycle like 85°C/85% RH. This implies that the moisture absorbed by plastic materials is partially condensed into water in the microvoids or free-volume of the materials.

During the reflow, the moisture vaporizes at high temperature and produces internal vapor pressure. The vapor pressure, however, will maintain at its saturated pressure as long as the moisture in the voids is not fully vaporized. The moisture affects the package reliability at reflow

from two aspects: generation of vapor pressure and degradation of interfacial adhesion. Although the vapor pressure remains at its saturated pressure when more moisture is absorbed, the adhesion strength may continuously deteriorate with additional moisture. When the interfacial adhesion is reduced to the level below the vapor pressure, the delamination will occur. Package cracking is not controlled by the absolute water weight gain; rather it is due to the local moisture concentration at a critical interface. In this case of the CF series package, the underfill material is the package.

The MSL level 1 classification is not designed to provide an accurate estimate of long-term moisture and vapor phase conditions inside the CF series package. Additional finite element modeling would be required to obtain this type of information. Xilinx has also provided collected volatile condensable materials (CVCN) values for the CF series package materials. Both the underfill and the lid adhesive have a value of 0.01%. These numbers and the MSL testing need to be integrated in to a broader “picture” of the overall physics of failure regarding moisture and non-hermeticity.

Xilinx has also conducted board-level reliability tests on the CF1509 package. Using 90/10 Pb/Sn columns attached with the IBM CLASP process, test devices were connected to an eight-layer FR-4 board. The substrate thickness was 2.97 mm using 0.56 mm diameter columns with a 1.0 mm pitch. The parts and board were subjected to a 0°C to 100°C temp cycle stress. The results of the test are plotted in Figure 1.4-1 as the blue line. The data shows a narrow distribution that begins to fail around 3,500 cycles with the entire distribution failing around 5,100 cycles.

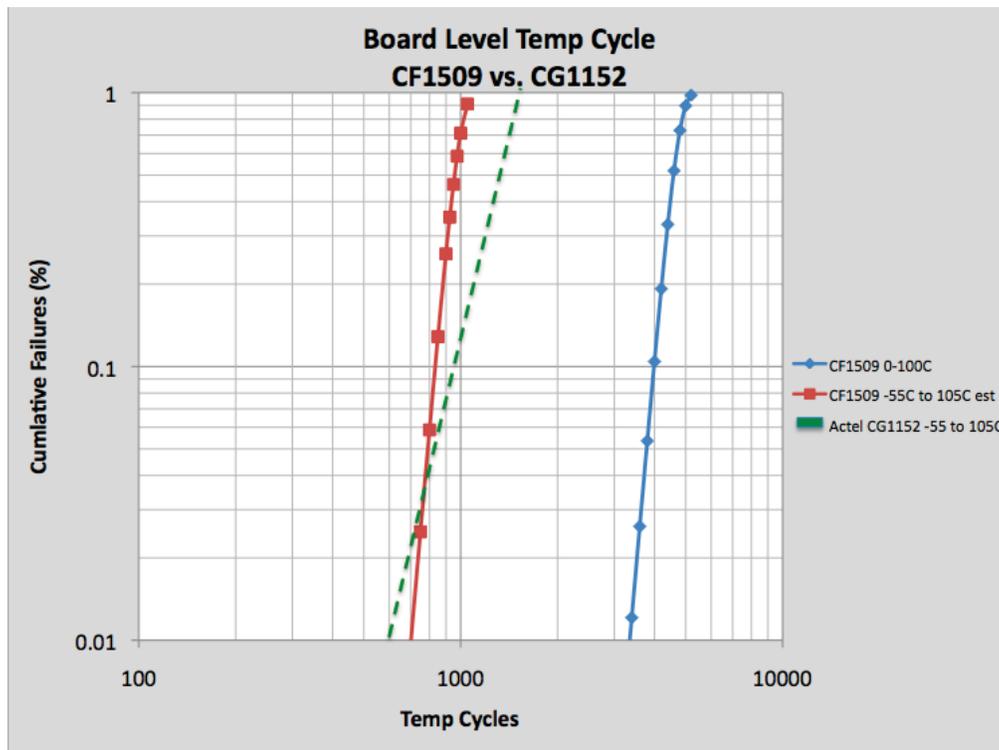


Figure 1.4-1. Xilinx CF1509 package-board level temp cycle versus Actel CG1152

In order to put this result in perspective, it was compared to Actel results for the CG1152 package used for the RTAX2000 FPGAs [11]. The Actel test was conducted from -55°C to 105°C , a much larger temperature delta compared to the Xilinx test. The Actel test used an eight-layer board that was 2.35 mm thick. Using the Norris-Landzberg modification to the Coffin-Manson equation, the results of the 0°C to 100°C Xilinx test can be estimated for a test condition of -55°C to 105°C . Doing this estimation allows us to make a more direct comparison of the Xilinx results to the Actel results.

The red line in Figure 1.4-1 is the calculation of the Xilinx CF1509 being temp-cycled at -55°C to 105°C . The green line in Figure 1.4-1 is the Actel results for -55°C to 105°C temp-cycling for the CG1152 package. Given the approximations used, these two results are considered equivalent. This means the temp-cycle-based reliability of the Xilinx Virtex-4 CF1509 is expected to be similar (no more or no less) than the Actel CG1152.

The Actel results showed a factor of almost $1.4\times$ improvement in temp-cycle performance if the columns were 80/20 Pb/Sn instead of 90/10 Pb/Sn. It is not known if this option for changing the Pb/Sn ratio for the Xilinx parts is available for the IBM Bromont process.

2.0 IDDQ STUDY IN ACTEL A54SX FPGAS

This IDDQ test is a continuation of work done in FY09. Additional IDDQ testing was done at a vendor's site to compare and contrast with JPL data. Inconsistencies first noted in the FY09 data have been resolved in the FY10 data. The inconsistencies had to do with experimental setup.

The original motivation for this test was to investigate the possibility of using IDDQ testing as an alternate to tri-temp testing. Tri-temp testing of antifuse FPGAs remains as a legacy parts/mission requirement. Tri-temp test is a functional test of the FPGA at $-55^{\circ}\text{C}/25^{\circ}\text{C}/125^{\circ}\text{C}$. This is a very expensive test in terms of schedule, effort, and equipment. Also, its correlation to long-term reliability is limited and not rigorously proven.

Antifuse FPGAs remain the vast majority of FPGA technologies used by NASA. The inherent rad hard nature of the antifuse is the main reason for choosing these devices. Passing a high current through a titanium-based metal electrode into a silicon oxide/carbide dielectric layer to another titanium-based metal electrode forms the antifuses. This high current produces a local (~ 10 nm) high temperature that can exceed the melting point of silicon ($>1400^{\circ}\text{C}$). This very high temperature melts the titanium and drives it through the dielectric to form a thin filament of connecting material between the two electrodes. This filament can be used to connect drive signals into FPGA resources or to provide interconnection paths for signal propagation across a chip.

Once the antifuse structure is formed, the FPGA is considered completely "programmed" and ready for operation. Historical generations of antifuse FPGAs have shown reliability failures as a result of the programming process. These programming failures resulted in NASA and other spacecraft providers having to enact multilevel risk mitigation steps. Many of the risk mitigation steps are trying to address the quality and reproducibility of the programming process. The FPGA programmer does not provide quantitative information, only qualitative. The device either "passes" or "fails." The details of how the device passed, whether or not it was near functional current limits, etc. are not available to the user.

This test was designed to address this issue of programming repeatability. By quantifying programming repeatability, we hope to gain insight into the variation of the antifuse resistance values. Being able to measure antifuse resistance at least indirectly will set a stage for an evolution of risk mitigation schemes.

2.1 IDDQ Experimental Results

A single design was chosen for the test. This design was programmed into several different FPGAs and the resulting IDDQ current would be measured. Differences in the IDDQ current can be initially assumed to be due to the variations in the antifuse programming. The design chosen was a finite impulse response (FIR) design. This design can be scaled in terms of the number of logical resources that are implemented. Scaling the design is an important variable in helping to determine variation in antifuse programming.

The basic experimental design is shown below in Table 2.1-1. There are three different variables, each with three different settings. This makes for a total of 27 different combinations of testing/device conditions. Each of the 27 different combinations was reproduced on 15 total separate FPGAs. Five FPGAs were used for each design resource level. Then each of these 5 FPGAs was measured at three different voltages and three different temperatures. This is a total of 135 separate experimental design inputs.

Table 2.1-1. 3³ experimental design for IDDQ testing

Design Resources	Voltage	Temperature
10%	Nominal - 10%	-40°C
50%	Nominal	25°C
80%	Nominal + 10%	85°C

The IDDQ results from all the various experimental combinations are summarized in Figure 2.1-1. Figure 2.1-1 shows three boxplots for each of the three design resource options at which IDDQ data was taken. The temperature and voltage data is combined for each design resource. The median IDDQ value for each of the three splits varies between 1.4 and 1.7 mA. Only the 50% design resource group had three outlier points for the 85°C split. The widths of the boxes are similar in size indicating that the amount of variation between all the splits was relatively constant.

A response surface model (RSM) of the data was also calculated as shown in Figure 2.1-2. A linear model with interaction terms was used for the ANOVA analysis. The confidence levels shown are for 95%.

IDDQ is shown to increase linearly with increasing voltage and temperature as is expected with a measurement of leakage current. Design resources show an inverse correlation between IDDQ current and amount of design resource used. This is a counterintuitive result as increasing resources should increase the amount of leakage. The model shows a large amount of variation in the small design resource group compared to the other two design resource groups. If this variation is reduced to a value similar to the other two groups, a flat to slightly increasing trend would then be obtained. This existence of a large amount of variation in the small design resource group would explain this result.

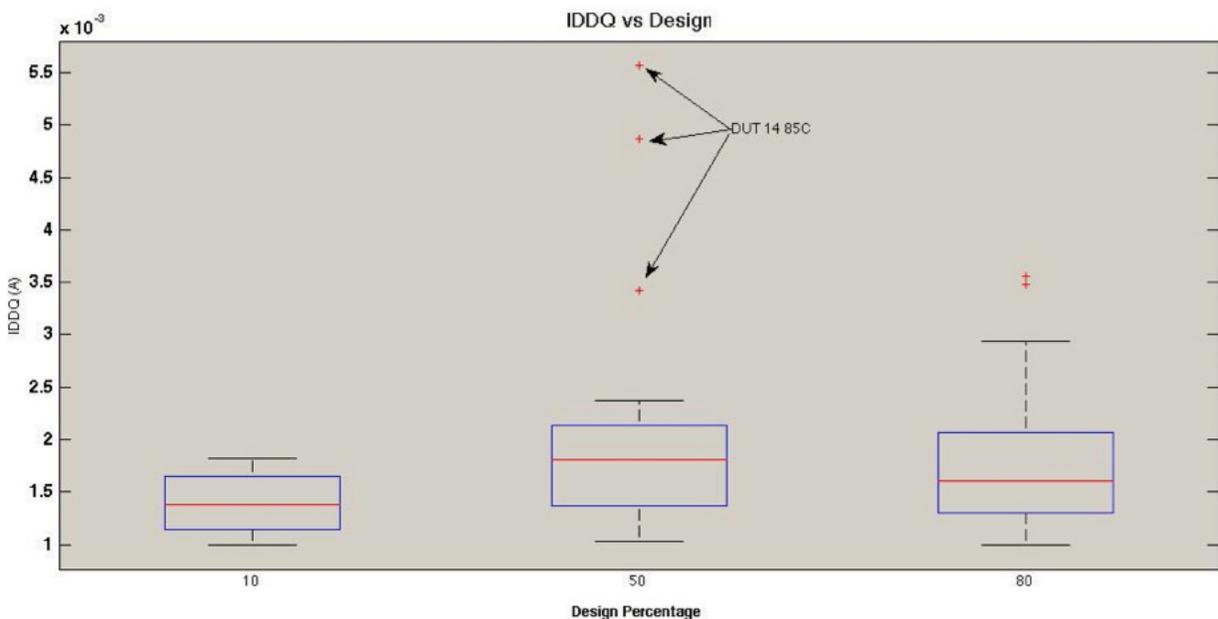


Figure 2.1-1. Boxplot for all IDDQ Data parsed by design percentage

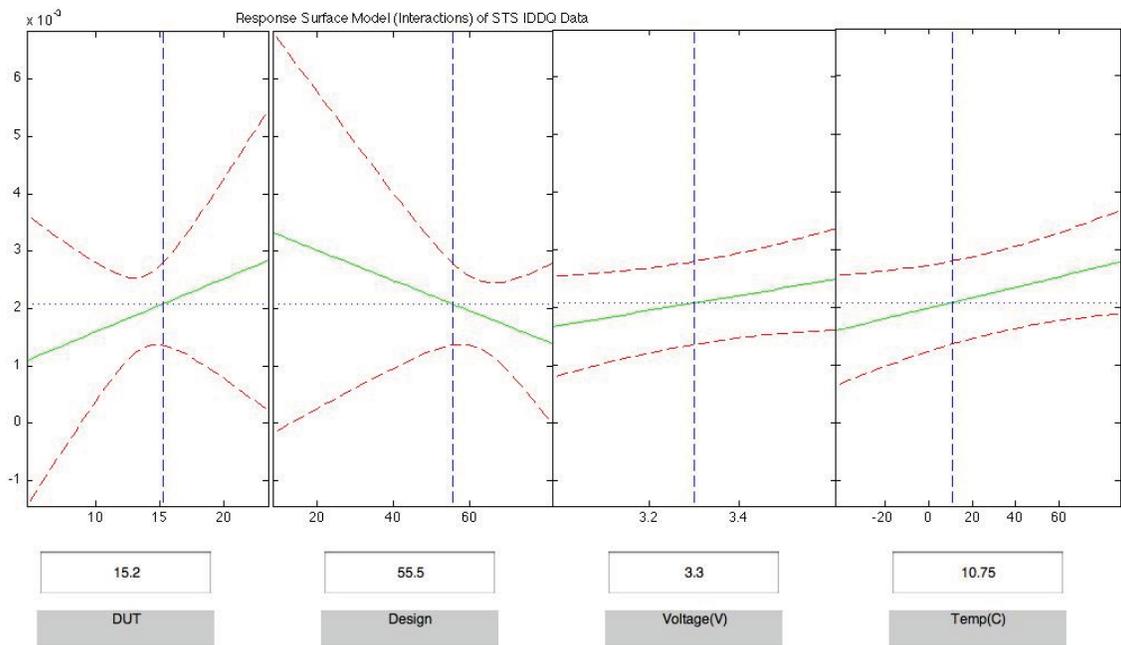


Figure 2.1-2. Response surface model for IDDQ data

3.0 ACTEL FLASH FPGA TECHNOLOGY

Actel offers a series of flash-based FPGAs with their IGLOO and ProASIC lines. These products have been available for several years. The new innovation is that this flash-based FPGA technology is now being applied to radiation-tolerant products. This section will review the technology and reliability data available to date. This review is important, as it will lead to the recommendation that this flash-based FPGA technology is a very important new product line that NASA needs to qualify and implement.

3.1 Flash FPGA Technology

Flash-based FPGA technologies offer several advantages compared to other FPGA technologies. The flash products are based on NOR flash cells that store their data without power being applied. This allows the FPGA to be configured at power-up without the need for external memory devices, helping to reduce cost and power, and improve system reliability.

Mobile devices such as smart phones are now the main growth area for many different IC technologies. A major difference in terms of operation is that mobile devices tend to have a large portion (~50%) of their time either idle or off. This is different than a data/communication-based implementation where the FPGA may be powered on almost 100% of the time. Practically, this means the standby power of the technologies used in these devices must be as low as possible. SRAM-based reconfigurable devices normally have much higher standby power than is acceptable for such mobile devices and therefore are not used. The flash-based FPGAs have substantially less power than the SRAM devices and offer an opportunity for manufacturers to extend their product lines.

FPGAs for portable devices need a very low-power “idle” state. Idle-state power for these applications would need to be measured in tens of μ Watts. Idle refers to a very light activity so that all FPGA flip-flops retain their state without being saved to and restored from a memory. Switching from idle to active must be very quick in a few clock cycles, not thousands. This is a unique advantage flash-based FPGAs can provide.

The overall approach to the flash FPGA is to develop the most low-power technology possible. There are many technology and design steps that can be done to significantly reduce power consumption, including the following:

- Start with a “low power” CMOS technology from a PMOS and NMOS I_{off} value
- Use high-k gate dielectrics
- Use multiple- V_{th} transistors; have the highest V_{th} devices used wherever possible
- Implement multiple V_{dd} processes if possible
- Use long-channel devices
- Implement triple-oxide processing
- Power aware synthesis and place and route software

The Actel flash FPGA is based on the concept of the flash device as a switch. The flash switch cell has a unique layout as shown in Figure 3.1-1.

The layout shows that there is a common gate stack shared between two devices, a sense device used to access the cell in terms of programming and reading, and a switching device used to set the FPGA configuration and route logic signals. Each cell is used directly in the signal path. Figure 3.1-2 shows the architecture for using the sense-switch cell in an FPGA

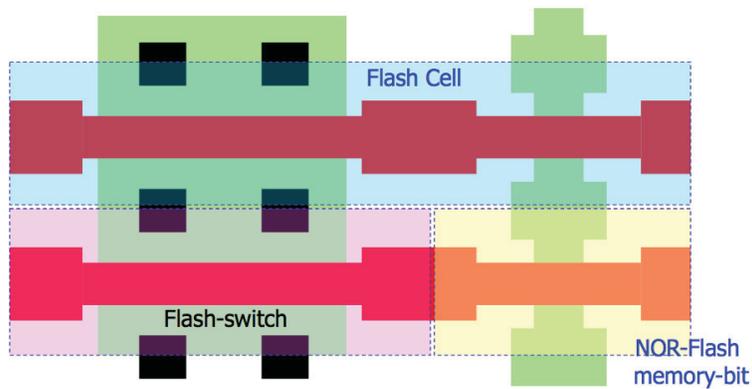


Figure 3.1-1. Flash switch cell layout [12]

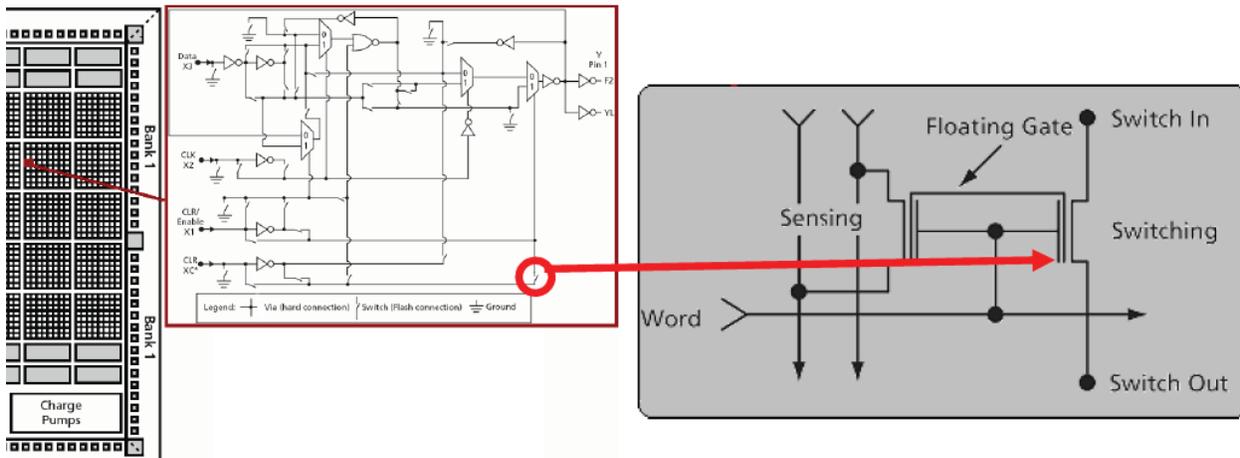


Figure 3.1-2. Sense-switch cell in FPGA architecture

This sense-switch FPGA cell is implemented in a high-voltage, triple-well process with deep trench isolation (DTI), which allows each device to have its own independent P-well. The independent P-well design helps improve coupling and therefore reduces the amount of voltage needed to program the cells. The cell typically operates at 10 V instead of 16.5 V. The cell has been shown to have immunity to gate and column disturb and to have improved programming times by approximately a factor of three over conventional P-well layouts. The memory array begins to show some reduction in the program window margin after 10,000 program/erase cycles as shown in Figure 3.1-3.

Total ionizing dose (TID) tests show similar degradation results when compared to the endurance data. Figure 3.1-4 shows cell window narrowing as a function of dose. The programmed state shows reduction of threshold voltage with increasing dose similar in behavior to the reduction in threshold voltage with increase program/erase cycles. A one volt threshold voltage shift is equivalent to approximately either 50 krad or 10,000 cycles.

In addition to the typical flash memory requirements, the switch also must meet the FPGA operation requirements. This means the switch must be able to isolate the connecting logic elements when programmed and deliver a low resistance path when erased. For use as an FPGA fabric switch, the cell has a very low leakage ($<10^{-11}$ A per cell) with an on-state drive current resistance of approximately 1.5k ohms.

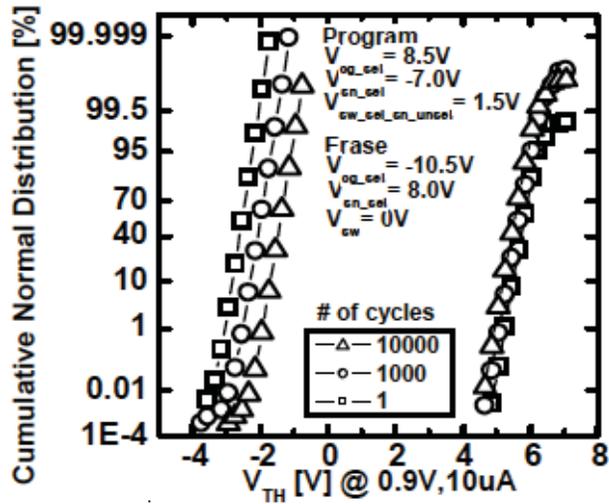


Figure 3.1-3. Program/erase cycle endurance

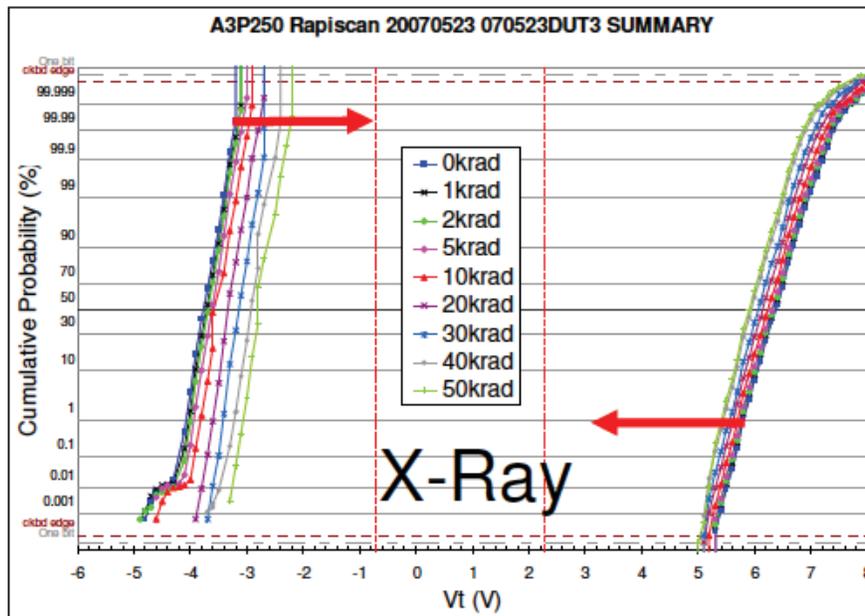


Figure 3.1-4. TID flash cell threshold voltage versus dose

Currently, Actel is specifying the technology at 20 Krad with 40 Krad possible if the cell is refreshed periodically. The refresh rate and conditions are not formally specified. Periodic refreshing will of course degrade the overall cell's lifetime. The tradeoff between radiation performance and cell endurance is critical to determining the safe operating area of this flash-based FPGA technology for future NASA missions. It is recommended that this reliability / radiation interaction be further pursued under the NEPP technology evaluation program. The benefits of ultra-low-power, mixed-signal FPGAs are quite significant to NASA and this technology should continue to be investigated.

4.0 SUMMARY

FPGAs continue to be a mission-critical electronic part. FPGA technology is advancing along with Moore's law and this provides new and more powerful parts for NASA missions. The Xilinx Virtex-4 is an order-of-magnitude improvement in resources and capability in terms of FPGAs for space applications. This large and powerful device requires a complex new packaging scheme that has challenged the historical military standards.

Xilinx has done a multi-tiered qualification to address the issues associated with the long-term quality and reliability of this package. The package has passed this multi-tiered qualification scheme. However, complete statistical physics-of-failure-based analysis and testing remains incomplete. This information may exist at IBM and SPIL, but it has not been made available for review.

Optical and SEM analysis of daisy-chain packages revealed significant misprocessing steps that would cause rejection of devices. These misprocessing steps need to be resolved through a formal action plan by Xilinx and verified by NASA/JPL.

IDDQ (quiescent current) testing of finite impulse response (FIR) filter designs in an antifuse FPGAs did not show a strong correlation to resource utilization, temperature, or voltage. This means IDDQ is not a viable technique to replace tri-temp testing.

Actel flash-based FPGA technology continues to develop and provide the promise of very low-power devices. The technology remains radiation sensitive but Actel is continuing to improve these devices and a rad-tolerant version of the flash device is projected to be available in the next one to two years.

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