National Aeronautics and Space Administration

NASA 2009 Body of Knowledge (BoK): Through-Silicon Via Technology

David Gerke
Jet Propulsion Laboratory
Pasadena, California

Jet Propulsion Laboratory
California Institute of Technology
Pasadena, California

JPL Publication 09-28 11/09

National Aeronautics and Space Administration

NASA 2009 Body of Knowledge (BoK): Through-Silicon Via Technology

NASA Electronic Parts and Packaging (NEPP) Program
Office of Safety and Mission Assurance
(Electronic Packaging Project)

David Gerke
Jet Propulsion Laboratory
Pasadena, California

NASA WBS: 724927.40.43
JPL Project Number: 103982
Task Number: 03.03.15

Jet Propulsion Laboratory
4800 Oak Grove Drive
Pasadena, CA 91109

http://nepp.nasa.gov

This research was carried out at the Jet Propulsion Laboratory, California Institute of Technology, and was sponsored by the National Aeronautics and Space Administration Electronic Parts and Packaging (NEPP) Program.

Reference herein to any specific commercial product, process, or service by trade name, trademark, manufacturer, or otherwise, does not constitute or imply its endorsement by the United States Government or the Jet Propulsion Laboratory, California Institute of Technology.

Copyright 2009. California Institute of Technology. Government sponsorship acknowledged.

ACKNOWLEDGEMENTS

The author would like to acknowledge the NEPP Program, managed by Michael Sampson and Kenneth Label, for funding. The author would also like to thank Chuck Barnes and Phil Zulueta for their contributions to this work.

Table of Contents

1 Executive Summary 1
2 Introduction—What are Through-Silicon Vias? 2
2.1 Why Use TSVs? 4
2.2 Drivers for TSVs 4
2.3 Enabling Technologies for TSVs 6
2.3.1 Wafer Fab/Wafer Foundry Vias 6
2.3.2 Vias First versus Vias Last 7
2.3.3 Laser-Processing TSV 9
2.3.4 Via Fill 10
2.3.4.1 IMP Sputtering for Higher Aspect Ratio via Filling 11
2.3.5 Wafer Thinning 12
2.3.6 Wafer/Chip (Via) Alignment 12
3 Markets that Will Utilize TSVs 14
3.1 Memory and Logic 15
3.1.1 DRAM 15
3.1.2 Flash Memory 17
3.1.3 Logic 18
3.1.3.1 Processors 18
3.1.3.2 FPGA 18
3.2 Image Sensors 19
3.3 Power Devices 20
4 Reliability 21
4.1 Thermal Issues 21
4.2 Various 3D Stacking Technologies 23
5 Conclusions 28
6 Recommendations 31
7 References 32

1 Executive Summary

Through-silicon via (TSV) is the latest in a progression of technologies for stacking silicon devices in three dimensions (3D). Driven by the need for improved performance, methods to use short vertical interconnects to replace the long interconnects found in 2D structures have been developed. The industry is moving past the feasibility (research and development [R&D]) phase for TSV technology into the commercialization phase where economic realities will determine which technologies are adopted. Low-cost fine via hole formation and highly reliable via filling technologies have been demonstrated; process equipment and materials are available. Even though design, thermal, and test issues remain, much progress has been made.

TSV is **not** a "solution looking for a problem," it is **the** solution for many applications such as memory, logic, sensors, and micro-electro-mechanical systems (MEMs). Many companies have TSV as a part of their roadmaps for higher integration. There are approximately 50 organizations identified with 3D TSV activities [1]. Technologically, TSV structures can be fabricated by a variety of methods and progress has been made in the area of thermal management and test issues. Cost/performance trade-offs will be a major factor as to when this technology will be available industry-wide.

Work in this area has already reached "critical mass" such that in the near future there will most likely be products introduced using TSVs because of the advantages this technology offers in the area of 3D integration.

This technology is not mature enough to start new work in the coming fiscal year (FY); therefore, no new National Aeronautics and Space Administration Electronic Parts and Packaging (NEPP) task is recommended for FY2010. However, implementation of this technology is moving quickly and a proposal in FY2011 should be considered.

2 Introduction—What are Through-Silicon Vias?

Vertical chip stacking in a single package increases the amount of silicon that can be put into a given package footprint. In portable and handheld devices, this enables smaller products by conserving valuable real estate on the board. Stacking die inside a package also results in faster signal transmission as a result of the shorter chip-to-chip routing and simplifies board assembly by reducing the number of components to be placed on the board. Placing and wiring devices in the third dimension promises higher clock rates, lower power dissipation, and higher integration density [1].

Through-silicon vias therefore refer to a 3D package that contains two or more chips (integrated circuits) stacked vertically so that they occupy less space on a printed circuit board (PCB) (usually the same footprint as the bottom chip). Through-silicon vias replace edge wiring by creating vertical connections through the body of the chips. The resulting package has no added length or width. Because no interposer is required, a TSV 3D package can also be flatter than an edge-wired 3D package. This TSV technique is sometimes also referred to as through-silicon stacking (or thru-silicon stacking; TSS).

Not all TSVs are the same. There are many variations of this technology. Several examples will be presented in the following paragraphs. Optical photographs of an example of copper-filled TSVs are shown in Figure 2-1.

The interconnection of two or more chips is what makes TSVs so attractive to packaging engineers. Figure 2-2 shows two types of interconnection methods between chips—planar and interlocking. The planar type consists of an electroplated Cu/Sn layer onto the Cu via. In this case, the bonding process between chips was achieved by direct contact of Cu/Sn bump and Cu via (Figure 2-2a). During chip stacking, inter-metallic compounds (IMCs) are formed. These are the same IMCs typically used with other 3D System in a Package (SiP) packages [3, 4]. The interlocking type of TSV consists of a Cu interlocking bump and Sn chip bump in Figure 2-2(b) and (c).

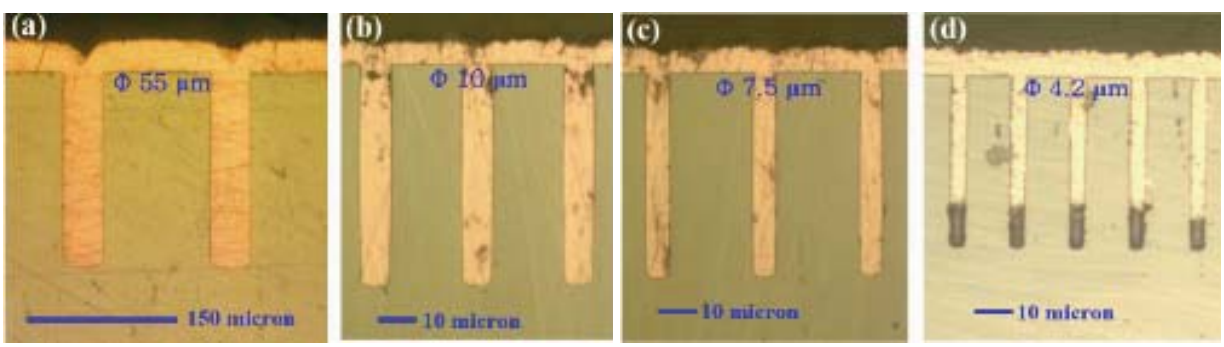

Figure 2-1. Optical images of Cu-filled silicon via holes with a diameter and aspect ratio of (a) 55 μm and 3.1, (b) 10 μm and 6.6, (c) 7.5 μm and 8.0, and (d) 4.2 μm and 11 [2].

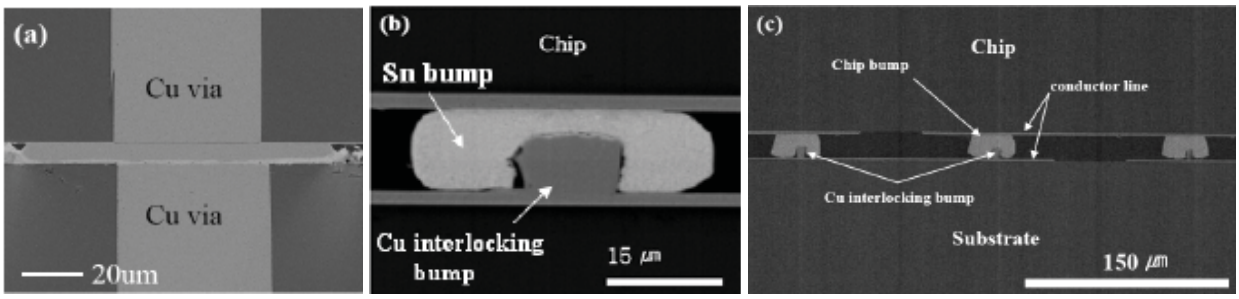

Figure 2-2. SEM images of (a) a planar bump, (b) an interlocked bump, and (c) a daisy-chain structure with interlocked bumps [2].

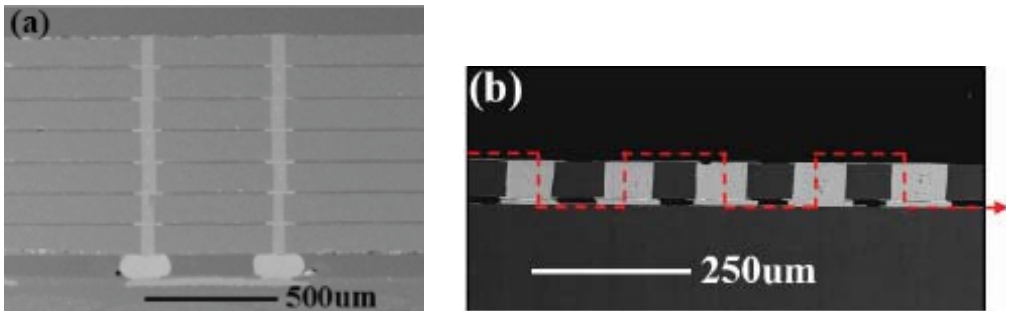

Figure 2-3. a) SEM image of stacked chip on a PCB and b) a daisy-chain configuration used to determine reliability of the stacked joint [5].

The planar bumping system described above is formed by a metallurgical reaction between the Cu via solder bump while the Cu bump process is held together by a mechanical bond during joining. Both interconnections can be achieved without any reflow or flux process required. Flux usually requires a cleaning process to remove residues, which can reduce mechanical reliability. The interlocking interconnection has been shown to achieve higher shear stress and lower contact resistance than the resultant chip stacking process with planar bumps [2]. For interlocking interconnection, the contact resistance per bump was down to approximately 10 mΩ and the shear strength per 252 bumps was 400 g as a function of bump diameter and bonding stress [5].

A cross-sectioned scanning electron microscope (SEM) image of chip stacking with planar type interconnection (seven chips) is shown in Figure 2-3a. During the development of the interconnection of TSVs to a PCB or other board material, daisy-chain test vehicles are used. A simple example of a daisy-chain is shown in Figure 2-3b where a portion of the chain is in the chip (top) and the corresponding portion of the chain is in the package or second chip.

Wafer-level 3D integration is a system-level architecture/technology in which multiple layers of planar devices (also called strata) are stacked and interconnected through the silicon or other semiconductor material in the Z-axis using TSVs. TSVs have also been described as through-wafer vias or through-wafer interconnect.

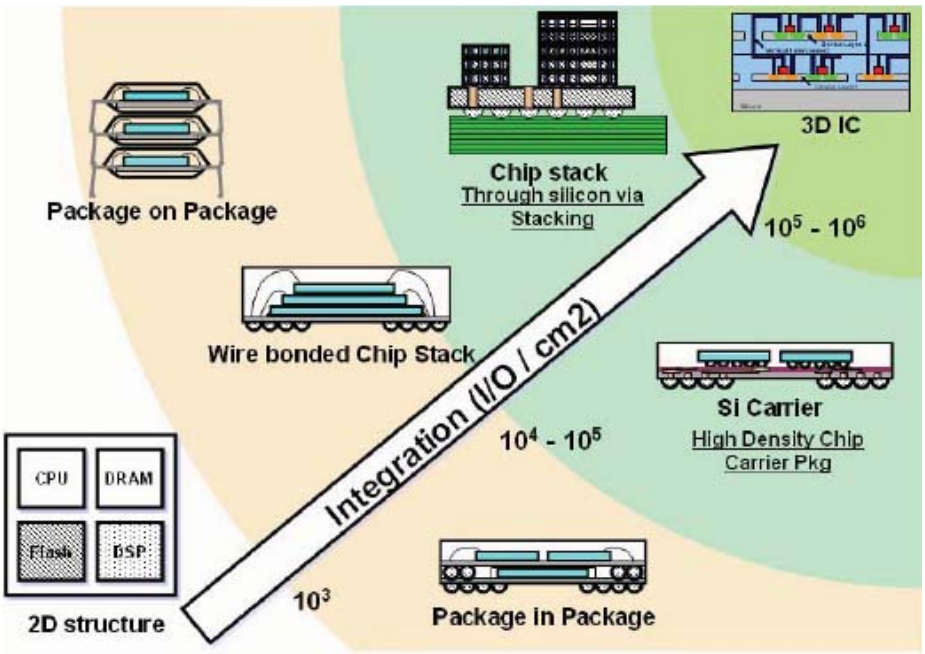

Figure 2-4. Emerging 3D silicon integration [1].

2.1 Why Use TSVs?

As the demands for higher wiring connectivity and shorter distances between chips have increased, so has the development of 3D silicon chip stacks, 3D packaging structures, and system-on-silicon large-scale integration (LSIs) [6-8]. Figure 2-4 shows chip integration approaches with increasing levels of integration. Of the existing 3D package technology options, wire-bonding remains the most popular method for low-density connections of less than 200 input/output (I/O) per chip. In the near future, however, it will become difficult to meet the increasing frequency requirements and demands for wiring connectivity merely by increasing the number of the peripheral wire-bonds. In order to overcome such wiring connectivity issues, 3D chip-stacking TSV technology is attractive because it offers the possibility of solving serious interconnection problems while offering integrated functions for higher performance [9-14].

Some of the key technologies needed to enable chip stacking include through-vias and high-density lead-free interconnects. One approach uses lead-free interconnections, which have either a binary or ternary eutectic composition that gives good bonding yield and later forms a >250°C melting temperature alloy post joining.

2.2 Drivers for TSVs

When is it advantageous to go vertical and when is it not? Stacking two wafers together and integrating them with vertical vias is costly. This cost must be justified through performance gains, functional gains, or cost savings elsewhere in the system. The market for TSV will be established when the benefits justify the cost. There is a growing consensus that several mainstream circumstances exist that justify 3D integration. Table 2-1 shows potential drivers for 3D integration.

Table 2-1. Potential drivers for 3D integration [5].

Driving Issue	Case for TSV	Caveats
Miniaturization	Stacked memories. Sensors, e.g., CMOS cameras, "smart dust"	For many cases, stacking and wire bonding is sufficient
Interconnect Delay	When delay in critical paths can be substantially reduced	Not all applications will have a substantial advantage
Memory Bandwidth	Logic-on-memory can dramatically improve memory bandwidth	While memory bandwidth can be improved dramatically, memory size can only be improved linearly
Power Consumption	In certain cases, a 3D architecture might have substantially lower power over a 2D	Limited domain. In many cases, it does not
Mixed Technology (Heterogeneous) Integration	Tightly integrated mixed technology (e.g., GaAs on silicon, or analog on digital) can bring many system advantages	Will be adopted on a case-by-case basis

The first and most obvious motivation is miniaturization. However, TSV 3D integration is rarely justified by the desire for miniaturization alone. For most circumstances, if volume reduction is the only goal, then it is much more cost-effective to stack and wire bond, or otherwise vertically integrate, at the package level. Such technologies are already in widespread use in cell phones, and continue to grow in sophistication. However, there are several significant exceptions. One exception that is being widely explored for TSV technology is for memory. Wire bonding cannot easily be used to stack identical memory chips, because they are all the same size. In addition, there are system advantages to thinning and stacking multiple memory die such that the aggregate memory has the same end form factor as one memory package. For example, this technology could enable a credit-card-sized video storage and viewing device that contains hundreds of hours of video [1].

Another exception is in imaging arrays, particularly complementary metal oxide semiconductor (CMOS) cameras for mobile applications. Imagers require a high bandwidth between the imaging array and the processor, and because they are separately fabricated, and later integrated, they also benefit from having the smallest possible thickness. Soon, they will also exploit the last driver listed in Table 2-1, mixed technology (heterogeneous integration). By moving all the electronics off the imaging array to a lower die in the chip stack, the imaging array can achieve an almost 100 percent fill factor, improving performance and decreasing area. Two through-vias per pixel are needed to connect to the underlying electronics. An example of such a circuit for a military application can be found in work performed at Lincoln Labs [17].

The most explored advantage of 3D is its reduction of the interconnect distance between chip functions. Many researchers justify 3D from interconnect delay and interconnect power perspectives. From a theoretical viewpoint, the advantages can be substantial. Several studies have presented a Rent's Rule style of analysis supporting this premise [18, 19]. The basic argument relies on the fact that with each additional layer of transistors, there is a similar increase in the number of circuit functions that can be interconnected within a fixed wire length. This leads to a 25 percent or greater decrease in worst-case wire length [20], a similar decrease in interconnect power [21], and a modest decrease in chip area. However, experience shows that many designs do not realize the large theoretical advantages in practice. Fortunately, with careful choice, appropriate design applications can be found. For example, field programmable gate arrays (FPGAs) are very interconnect-bound and can achieve substantial performance and power improvements when recast in 3D [22].

Stacking memory die to create a new "super-memory" chip is not the only 3D application involving memory. An interesting area of application is targeting logic-on-memory, which is creating a high-bandwidth memory interface to the logic. For many end applications, the demand for memory bandwidth is growing rapidly. In many cases, this is due to the increased use of multi-core processors. With the addition of each processor comes a similar requirement for increasing memory bandwidth. It is expected that by 2010, a 32-core CPU will require 1 TBps of off-chip memory bandwidth [1]. Similar bandwidths will be beneficial in other applications, including digital signal processing, graphics processing, and networking. This, by itself, gives a fairly natural case for 3D, one that has been only lightly explored, and then mainly in the context of general-purpose computer micro-architecture. For example, 3D caches can lead to 10 to 50 percent reductions in cache latency, depending on the benchmark used [1].

2.3 Enabling Technologies for TSVs

Processes in a 3D integration sequence include through-wafer via formation, deep reactive ion etching (DRIE) or laser-drilling, via filling by deposition of diffusion barrier and adhesion layers, metallization, wafer thinning and alignment, and bonding [23]. Figure 2-5 shows the major technologies related to 3D TSV.

2.3.1 Wafer Fab/Wafer Foundry Vias

TSVs can be fabricated during the integrated circuit (IC) fabrication process at the wafer fab/wafer foundry. Deep trench capacitor technology is available in foundries supplying embedded memory. The diameters of the 3D TSVs are larger than normal deep trench capacitors and therefore will require a ground rule change for the foundry. Companies developing TSV services include Chartered and TSMC.

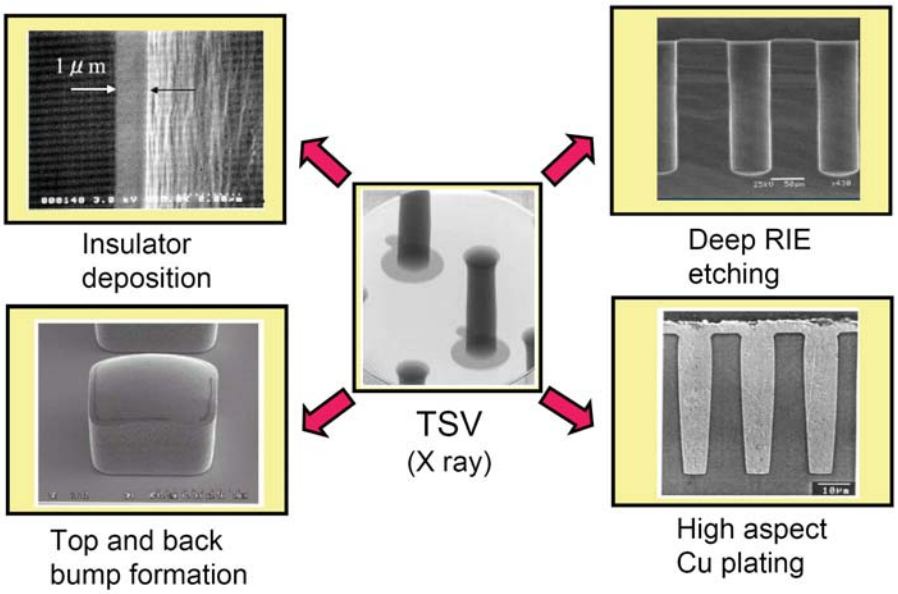

Figure 2-5. 3D TSV technologies [24].

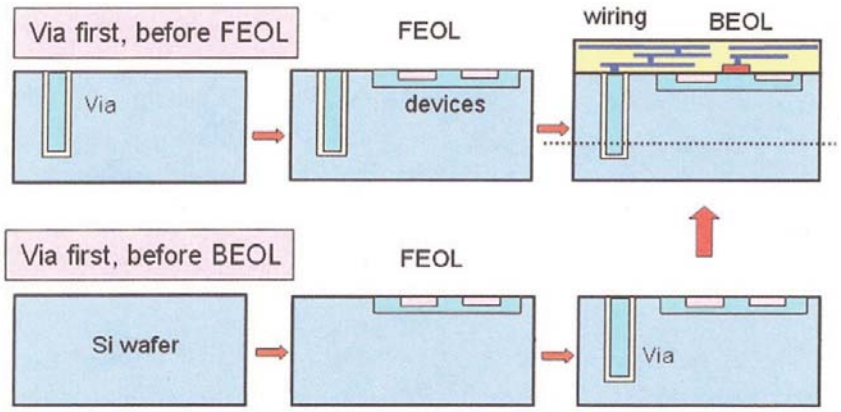

Figure 2-6. Examples of via-first technology [25].

Foundry TSVs can be inserted either just before device fabrication; before the front end of line (FEOL); or just after the devices have been fabricated, but before the fabrication of the on-chip interconnect and before the back end of line (BEOL). If the TSVs are fabricated first, the conductive material selected for the vias is typically doped polysilicon, which can survive subsequent device fabrication process temperatures. This polysilicon deep trench TSV technology has been described in detail in many publications [19]. Although the polysilicon connections are not as conductive as copper connections, they provide sufficient conductivity for many applications. If the TSVs are fabricated after the devices are formed, tungsten or copper can be used. NEC, CEA-LETI, and ZyCube have introduced processes for FEOL polysilicon. IMEC has developed a FEOL copper-based process called "copper nails." These processes are examples of vias-first technologies (see Figure 2-6).

2.3.2 Vias First versus Vias Last

Although definitions differ by group, it is generally accepted that in the vias-first approach, TSVs are fabricated prior to bonding to the stack. In the vias-last approach, TSVs are fabricated after bonding to the stack. TSVs can be formed from the top (face or active side) or from the bottom (backside) of the wafer. These options may be combined in numerous process sequences. Table 2-2 shows the common process sequence options.

Figure 2-7 shows an example of an FEOL TSV vias first or a BEOL TSV vias first in which the first wafer is flipped and face-to-face bonded to the second wafer. The first wafer is then thinned on the stack to reveal the backside vias and the backside processed (isolation layer such as SiO_2 or Si_3N_4 and copper pad formation), readying the structure to bond to the next layer. No handle wafer is needed in this sequence, which is an advantage. However, both wafers are in jeopardy during the thinning and backside processing of the second wafer. Face-to-face bonding can only be done once in a stack because after such bonding, the face of the second wafer is no longer available to bond to the next wafer in the stack.

Figure 2-8 shows the FEOL or BEOL vias first process in which the second wafer is mounted to a handle wafer for thinning. After thinning, backside processing is performed on the handle wafer and then the second wafer is stacked and bonded back-to-face. The handle is subsequently released.

Table 2-2. Process sequences for 3D integrations utilizing TSV [25].

Process				
1	FEOL TSV Vias first	Handle, thin backside process	Back to front bond (metal to metal bonding Cu-Cu, Cu-Sn-Cu, etc.)	
2	BEOL TSV Vias first	Handle, thin backside process	Back to front bond (metal to metal bonding Cu-Cu, Cu-Sn-Cu, etc.)	
3	FEOL TSV Vias first	Front to front bond (metal to metal bonding Cu-Cu, Cu-Sn-Cu, etc.)	Thin backside process	
4	BEOL TSV Vias first	Front to front bond (metal to metal bonding Cu-Cu, Cu-Sn-Cu, etc.)	Thin backside process	
5	Post BEOL Vias last	Front to front bond (metal to metal bonding Cu-Cu, Cu-Sn-Cu, etc.) or SiO_2 bonding, or polymer bonding	Thin	TSV (back) backside process
6	Post BEOL Vias first	Handle, thin	TSV (back) backside process	Back to front (metal to metal bonding Cu-Cu, Cu-Sn-Cu, etc.)
7	Post BEOL Vias last	Handle, thin	Back to front (polymer bonding)	TSV (front) backside process
8	Post BEOL Vias first	TSV (front)	Handle, thin backside process	Back to front (metal to metal bonding Cu-Cu, Cu-Sn-Cu, etc.)
9	Post BEOL Vias first	TSV (front)	Front to front bond (metal to metal bonding Cu-Cu, Cu-Sn-Cu, etc.)	Thin backside process

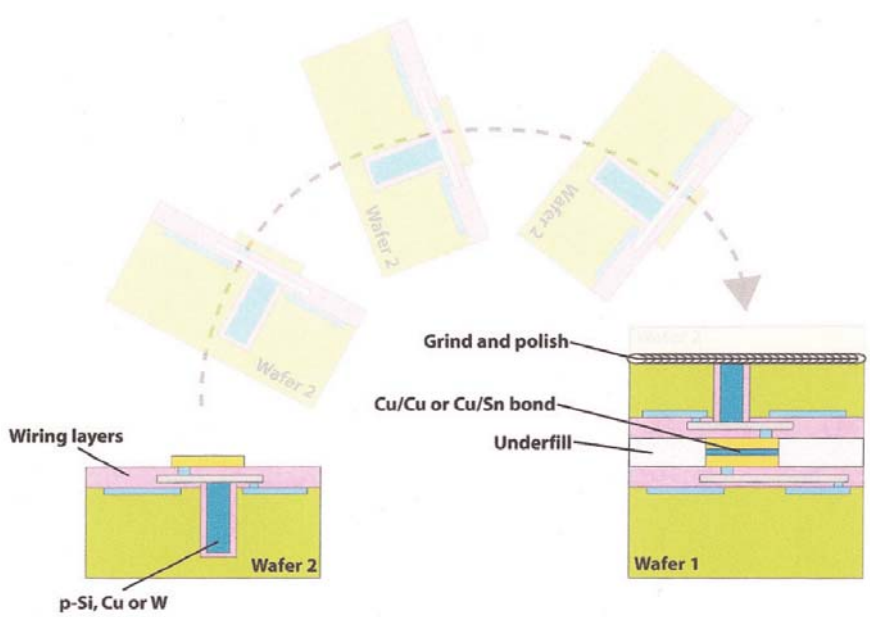

Figure 2-7. Front-to-front, vias last, without a carrier wafer [1].

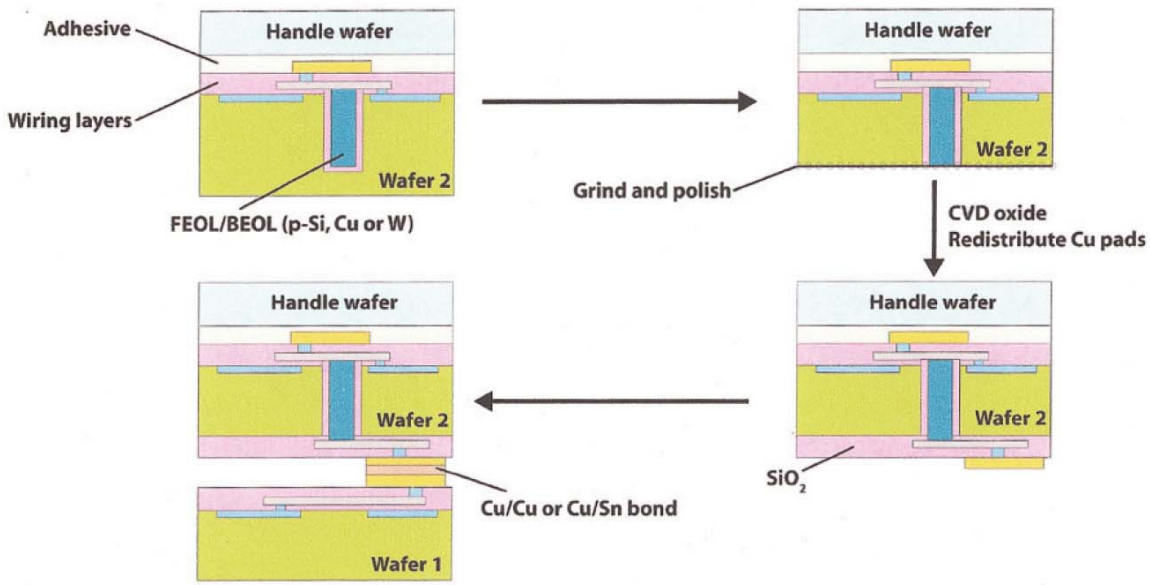

Figure 2-8. FEOL or BEOL vias first with handle wafer [1].

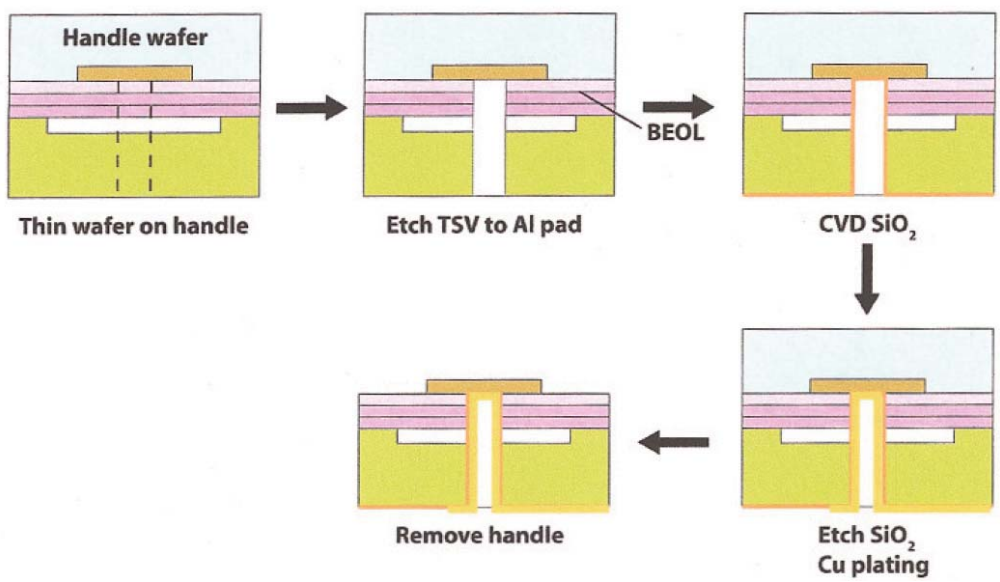

Figure 2-9. Vias from the backside after bonding [1].

2.3.3 Laser-Processing TSV

Ultraviolet (UV) lasers have been shown to produce a much cleaner cut with far less thermal damage than infrared (IR) lasers. Reports indicate that a UV laser-machined feature can be within 2 μm of an active device without producing device degradation [26]. Laser repetition rate, beam scan rate, and pulse play a significant role in determining the throughput and quality of the resulting laser-machined feature.

Major advances in laser via technology have occurred in the past few years. Figure 2-10 shows 10 μm vias that have been drilled to a depth of 70 μm for an aspect ratio of 7 to 1. The natural sidewall taper angle for laser vias is reported to be 85 degrees (Figure 2-11), which makes them suitable for sputter metallization [27, 28].

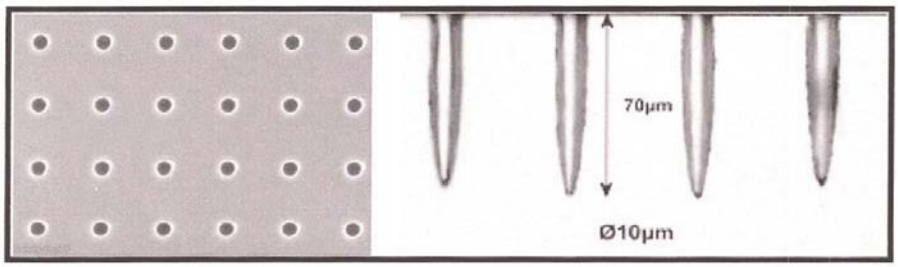

Figure 2-10. Laser vias in silicon (10 × 70 µm) [27, 28].

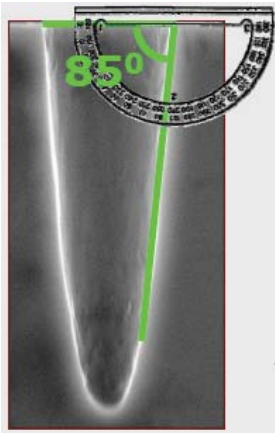

Figure 2-11. Laser vias in silicon illustrating the taper of 85° [27, 28].

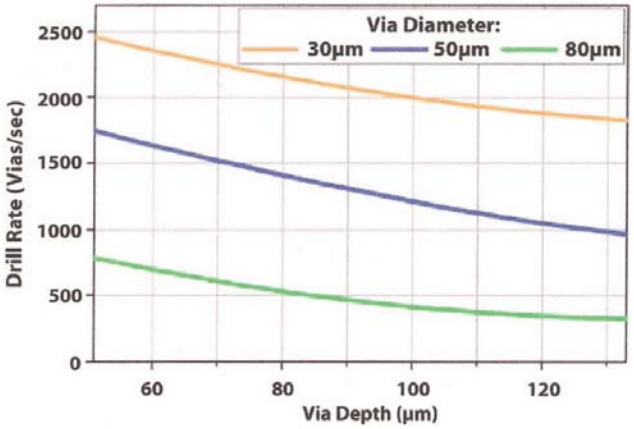

Figure 2-12. Laser vias drill rate in silicon versus via diameter [28].

Surface finish inside the via is a strong function of "drilling" rate. Rapid drilling produces a rougher sidewall. Figure 2-12 shows the drilling speed for various diameter vias in single crystal silicon.

It is likely that 10 µm vias will meet many of today's needs. Laser proponents claim that they can reduce the via diameter down to 1 µm, in which case this technology will move itself to the mainstream of 3D via generation technologies [28].

2.3.4 Via Fill

Difficulties encountered in via filling are directly attributable to via diameter and aspect ratio, which in turn are directly related to the application and thus density of TSV that are required. For example, for memory applications, far fewer TSVs are required to interconnect static random access memory (SRAM) or dynamic random access memory (DRAM) stacks. Thus, memory fabricators have been able to successfully integrate laser via formation in their processes and have no apparent trouble filling 25 to 50 µm vias with traditional seed sputtering and subsequent plating techniques.

IBM recently pointed out that TSV for interconnection of logic functions will require approximately 4 to 5 µm vias to interconnect at the core level and approximately 2 µm vias to interconnect at the unit level as shown in Figure 2-13 [29].

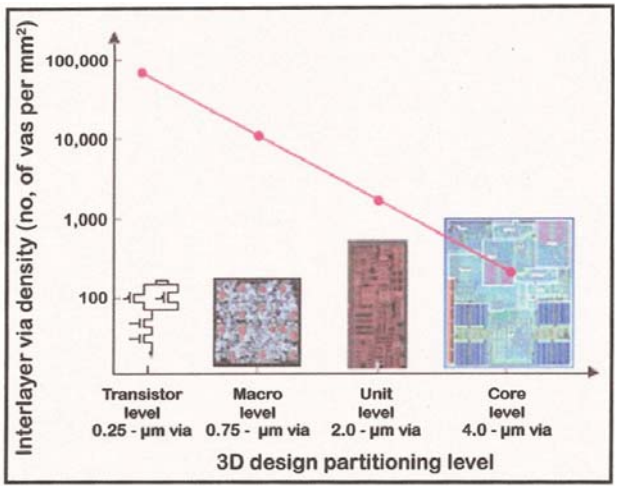

Figure 2-13. Design partitioning for 3D interconnect as described by IBM [29].

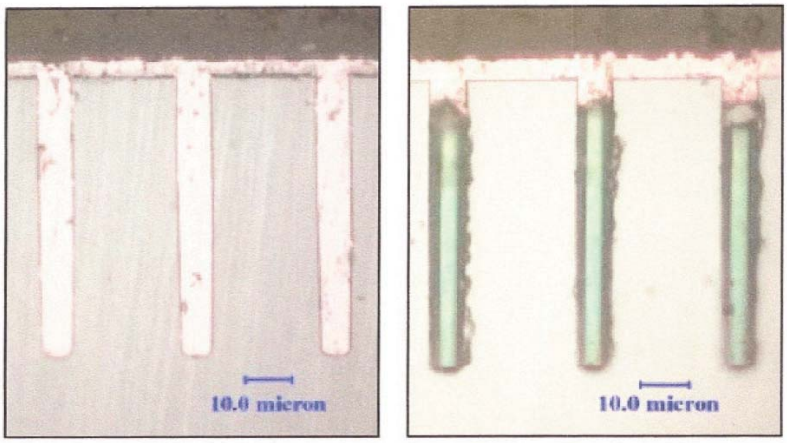

Figure 2-14. Vias plated with Cu after Cu seed deposition by IMP sputtering and normal sputtering [31].

2.3.4.1 IMP Sputtering for Higher Aspect Ratio via Filling

Filling of high aspect ratio vias with electroplated copper requires a smooth and continuous seed layer to prevent copper diffusion into the adjacent dielectric. This process requires conformal/ continuous coverage of a barrier layer along the via sidewalls. Conventional physical vapor deposition (PVD) DC magnetron techniques are inadequate for this application, because of insufficient step coverage of Cu on the sidewalls of the high aspect ratio vias. Ionized metal plasma (IMP)-based PVD technology is known to provide superior step coverage of Ta and Cu because of the directionality of the deposited atoms and utilization of ion bombardment to sputter material from the bottom of the via to the sidewalls, thus yielding continuous and conformal barrier and seed layers [30]. Recently, IMP sputtering has been shown to fill such high aspect ratio 3D vias [31, 32].

IMP sputtering enables more conformal deposition of copper seed layer on the sidewalls as well as the bottom of via holes than conventional sputtering. As shown in Figure 2-14, conventional sputtering deposits a conformal copper seed on the sidewalls of a 7.5 × 60 µm via no more than 10 µm deep, whereas using IMP sputtering results in complete via fill for the same dimension via. Even this technique does have its limits, however, and it fails to completely coat the inside of a via of dimensions 5.7 × 52 µm.

2.3.5 Wafer Thinning

Temporary bonding of 3D wafers to temporary substrates is the accepted method for thinning wafers. If the first two wafers (or die to wafer) are bonded face to face, the bottom wafer serves as the carrier and no temporary carrier is needed. In all other cases, a temporary carrier and temporary adhesive are necessary.

Adhesive layers for temporary bonding can be supplied as liquids (waxes and thick resists) and/or laminable dry-films. Temporary bonding adhesives can allow the release of the device wafer by (a) dissolution of the adhesive in an appropriate solvent, (b) heating above a release temperature, or (3) exposure to UV light. There are a number of commercial products on the market in all of these categories [33].

Properties that must be examined for temporary mounting adhesives include:

1. Maximum temperature exposure capability—This must match the processing expected to be done on the backside of the wafer.
2. Chemical resistance to the chemicals used during the processing of the back side (backgrinding, coating and developing, etching, etc.).
3. Ease of application (i.e., spin coating in the case of wax/resists, and lamination in the case of dry-film tape).
4. Ease of debonding process (i.e., heat, UV, or solvent release) and its degree of achievable automation, as well as the ease of cleaning the device wafer after debonding—The debond process must ensure that all adhesive is removed quickly with no residual material left behind.
5. Optical transparency—If backside alignment is required to align the photomask alignment pattern to the fiducials on the device wafer's front side, the fiducials (alignment keys) must be visible.
6. Thickness control—To keep the device wafer within the required thickness uniformity after back thinning, it is imperative that the intermediate layer and the carrier wafer have comparable or even lower thickness variation. Waxes and resist applications are usually applied with spin coating, where the achieved uniformity is well below 1 percent.

The choice of temporary adhesive is dependent on temperature and mechanical requirements for backside processing subsequent to wafer thinning.

2.3.6 Wafer/Chip (Via) Alignment

One of the last important steps required in this 3D technology is the alignment prior to bonding. Alignment accuracy determines the pad size and, by consequence, the maximum vertical interconnect density. It depends on [16]:

1. Bonding technique (face-to-face or face to back),
2. Type of attachment (direct bonding SiO_2, “glue,” or metallic—Cu Sn-Cu alloy)
3. Die-to-die, die-to-wafer, or wafer-to-wafer
4. Wafer flatness
5. Wafer co-planarity
6. Uniformity and mechanical noise during alignment and bonding

A flip-chip bonder can place known good die (KGD) on the 300 mm base wafer with an alignment accuracy of 10 μm (3 sigma), then attach the die/wafer combination with a temporary polymer adhesive at an effective rate of approximately 4,000 units per hour. A wafer bonder can then permanently bond the chips at 270°C and pressure for one to two hours. The Cu/Sn forms a eutectic alloy that is heat resistant up to 600°C, allowing additional chips to be added on top of the first bonded pair by the same process [1].

An alignment of ±1 μm is possible using commercial pick-and-place tools. A moderate (i.e., 350°C for 2 hours) post-oxide bond anneal is then initiated to form a monolithic conductor contact. From daisy-chain structures, the average direct bond interconnect (DBI) resistance is estimated to be less than 0.1 Ohm [34]. Figure 2-15 shows an example of a 10 μm pitch DBI bond.

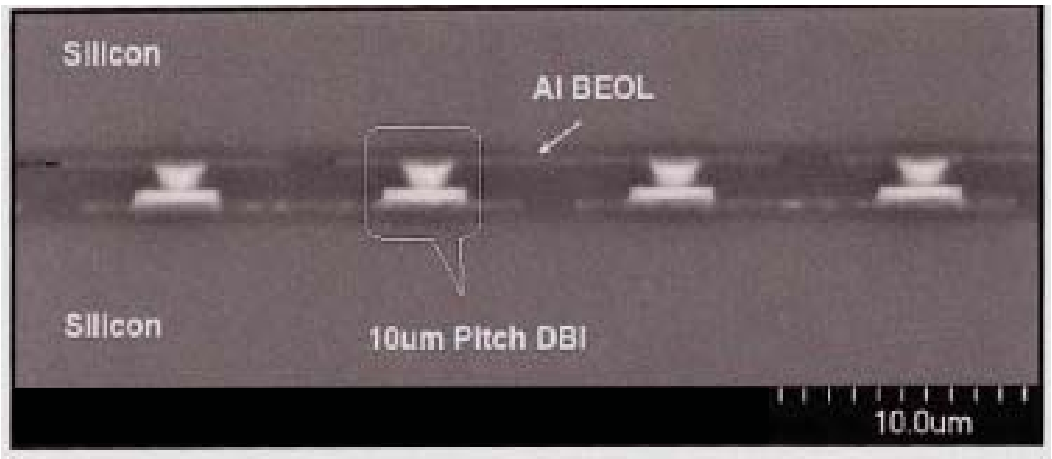

Figure 2-15. 10 μm pitch DBI bond [34].

3 Markets that Will Utilize TSVs

The 3D TSV market can be divided into two distinct markets (see Figure 3-1). The first applications are for low-density 3D vias and typically focus on chip-to-chip or chip-to-wafer bonding. High-density 3D vias and wafer-to-wafer bonding are anticipated in future applications [15].

Applications for 3D TSV include image sensors, flash, DRAM, processors, FPGAs, and power amplifiers. Table 3-1 provides examples of company announcements. The timing for mass production depends on how the TSV compares in terms of cost with existing technologies. In many cases, this means wire-bonded die stacking. While performance is a driver, cost is a limiting factor.

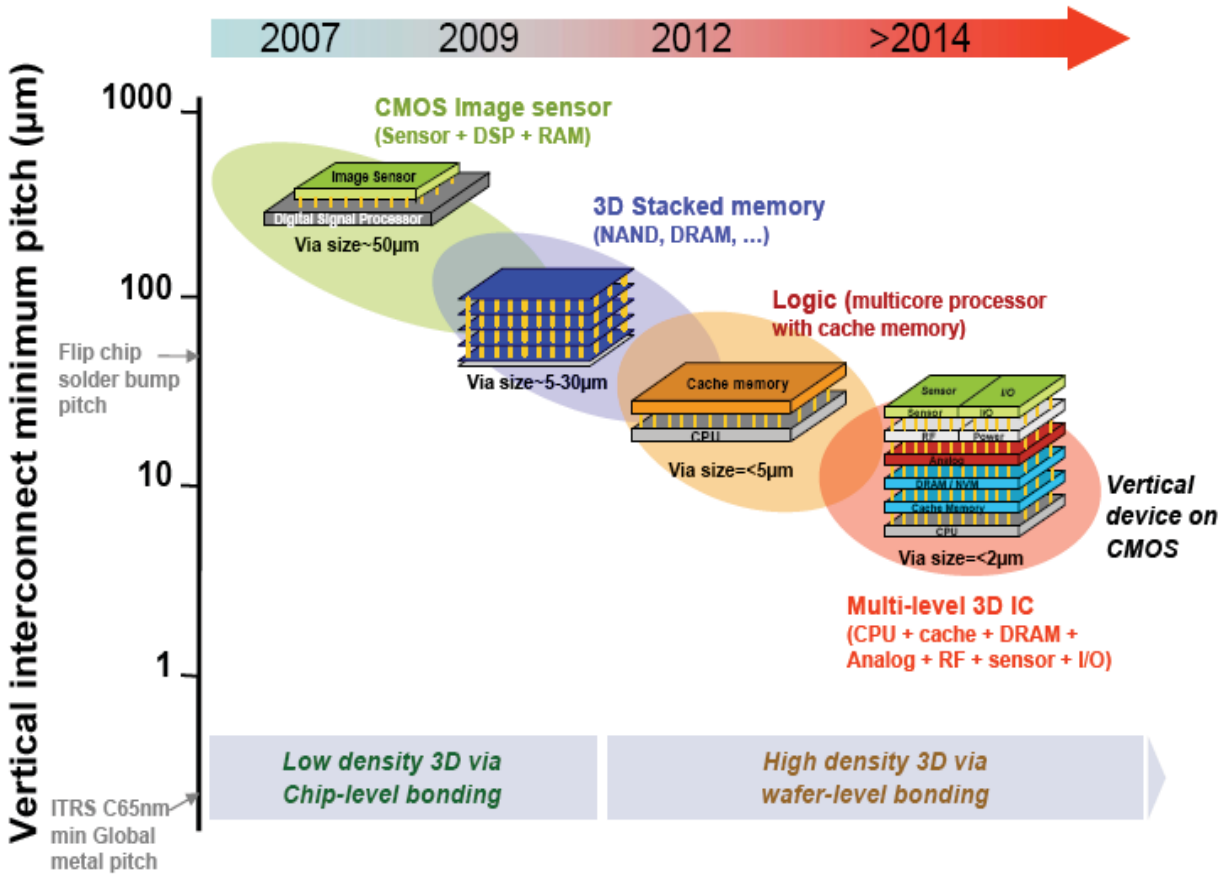

Figure 3-1. 3D applications and required via diameter [16].

Table 3-1. 3D TSV products slated to be manufactured in the near future [1].

Company	Memory and Logic	RAM	Flash	Image Sensor	Power Amplifier	FPGA
Chartered Semiconductor		X				
Fujikura				X		
IBM	X				X	
Intel	X					
Micron		X	X	X		
NEC / Elpida	X	X				
Samsung		X	X			
Sanyo				X		
Sony	X					
Tezzaron		X				
Tessera				X		
Toshiba				X		
Xilinx						X
ZyCube				X		

3.1 Memory and Logic

Chip-on-chip (CoC) is the first step in moving to 3D at the wafer level. In this technology, the chips are thinned and face-to-face bonded without TSVs. Researchers at AT&T Bell Labs proposed one of the first concepts [35].

The microcontroller for Sony's PlayStation had initially been fabricated using 90 nm embedded DRAM process technology. In 2005, Sony introduced a microcontroller and memory CoC for the PlayStation. One of the drivers for the adoption was that Sony was unable to find a way to make the die cheaper by scaling embedded DRAM process technology from 90 nm to 65 nm. Sony noted that even with the adoption of a single-chip DRAM and logic, each with a different manufacturing process, it would take a long time to obtain acceptable yield levels [36].

It is possible to achieve high-speed data transfer with CoC technology because the memory chip is interconnected directly to the logic IC with microbumps. Individual memory chips are used, essentially eliminating the memory capacity limitations of embedded DRAM. The higher data transfer rate is made possible by the greater bit width, achieved by a larger quantity of microbumps. The microbumps provide more interconnects than wire bonding and offer lower parasitic capacitance, resistance, and inductance because they are only several dozen microns in diameter. This makes it easier to increase the operating frequency.

Customers are demanding increasing amounts of memory for applications such as HDTV that previously used 64 Mbit or less memory. Systems supporting 1080i imagery now come with 128 Mbit to 256 Mbit memory. As equipment performance and function continue to improve, memory capacity will continue to increase and eventually embedded DRAM will be unable to handle the requirements [1]. It is only natural for TSV to provide the interconnect densities required in the future.

3.1.1 DRAM

Today's DRAMs are constructed around 50 and 40 nm processes. Issues include concerns that high-speed memory such as DDR3 will suffer performance limitations when connected in a

stacked package using wire bond technology. 3D technologies developed by Samsung, Micron, NEC, and Tezzaron are targeted at mobile phones and other portable devices with sufficient memory to run high-definition video and other 3D graphics applications in the near future.

Samsung Electronics has announced the first all-DRAM stacked memory packaging using TSV technology. Prototypes using the company's wafer-level-processed stacked package (WSP) consist of four 512 Mb DDR2 DRAMs for a combined 2 GB of high density memory and a 4 GB DIMM stack made up of TSV-processed 2 GB DRAMs. Samsung stated that it was developing the process for next-generation computer systems in 2010 and beyond [37].

Elpida has developed stacking technology with polysilicon FEOL technology with NEC and Oki in the joint NEDO project that is expected to be commercialized in 2010 [37]. The motivation for adoption of DRAM is provided in Figure 3-2. It is predicted that at the 32 nm node in 2010, a 3X memory density can be achieved using TSV technology [38].

Micron has pointed out that thermo-mechanical stresses need to be determined vs. TSV diameter Aspect Ratio (AR) and pitch. In addition, Micron has been one of the only companies pointing out that via capacitance varies linearly with die thickness and inversely with via pitch. For fixed via size, tighter pitches can be achieved with thicker insulator dielectrics; however, deposited SiO_2 layers have a very limited thickness range [~1–1.5 um] before they crack. Table 3-2 shows Micron's estimation for the timeline of DRAM development with TSV.

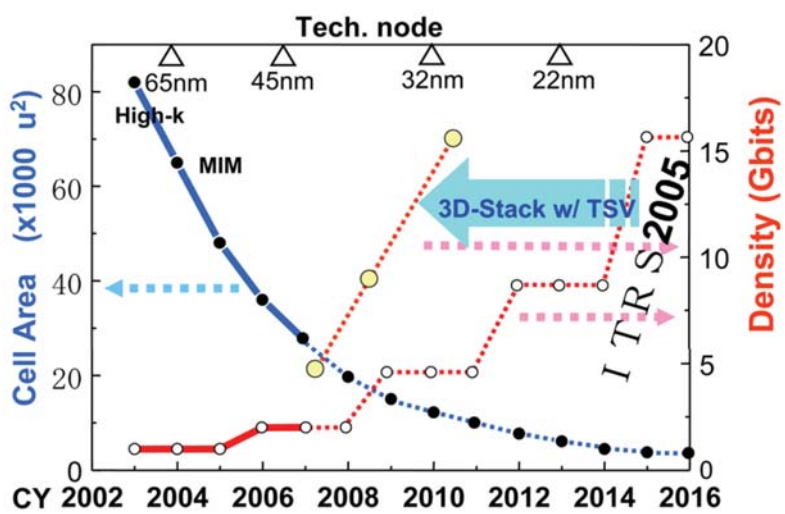

Figure 3-2. Drivers for DRAM TSV development [38].

Table 3-2. TSV for DRAM memory [39].

	Today	Tomorrow	Future
Via Diameter	10–30 µm	5–10 µm	1–5 µm
Via Depth	50–100 µm	25–50 µm	15–25 µm
Wafer Thickness	50–100 µm	25–50 µm	15–25 µm
Aspect Ratio	3:1–5:1	5:1–10:1	10:1 & greater
Pitch	75–100 µm	50–75 µm	20–50 µm
TSV Density	~100 I/O	~500 I/O	~1000 I/O
Package Type	DDP	QDP	8DP

3.1.2 Flash Memory

Examples of flash memory applications include memory storage cards, USB drives, MP3 players, digital cameras, and portable gaming machines. Flash memory is considered a potential replacement for hard disk drives. Flash memory does not have the mechanical limitations of hard disk drives and shows performance advantages in terms of speed, noise, power consumption, and reliability.

Samsung has noted that the demand for smaller and smaller NAND flash card form factors is increasing at a rapid rate. Samsung believes that in the future, flash applications will require TSV to meet performance / form factor requirements [40].

Many memory manufacturers are proceeding with pushing the wafer fab technology toward 32 nm geometries and beyond while many experts think that the memory cells will be so small that the operation will be unstable. The largest part of the perceived problem is not related to the smaller transistor sizes but rather in the signal delay [41].

Figure 3-3 shows Samsung's projections for NAND cost in the future. Samsung believes that 3D IC technology would make it possible to maintain the current pace of cost reductions.

While Samsung has made an argument for the adoption of TSV for flash, other companies argue that the cost of TSV cannot be justified and the required density can be obtained by thinning die and wire bonding the stack. TSV technology is not expected to be used for flash in high volume until 2012 [1].

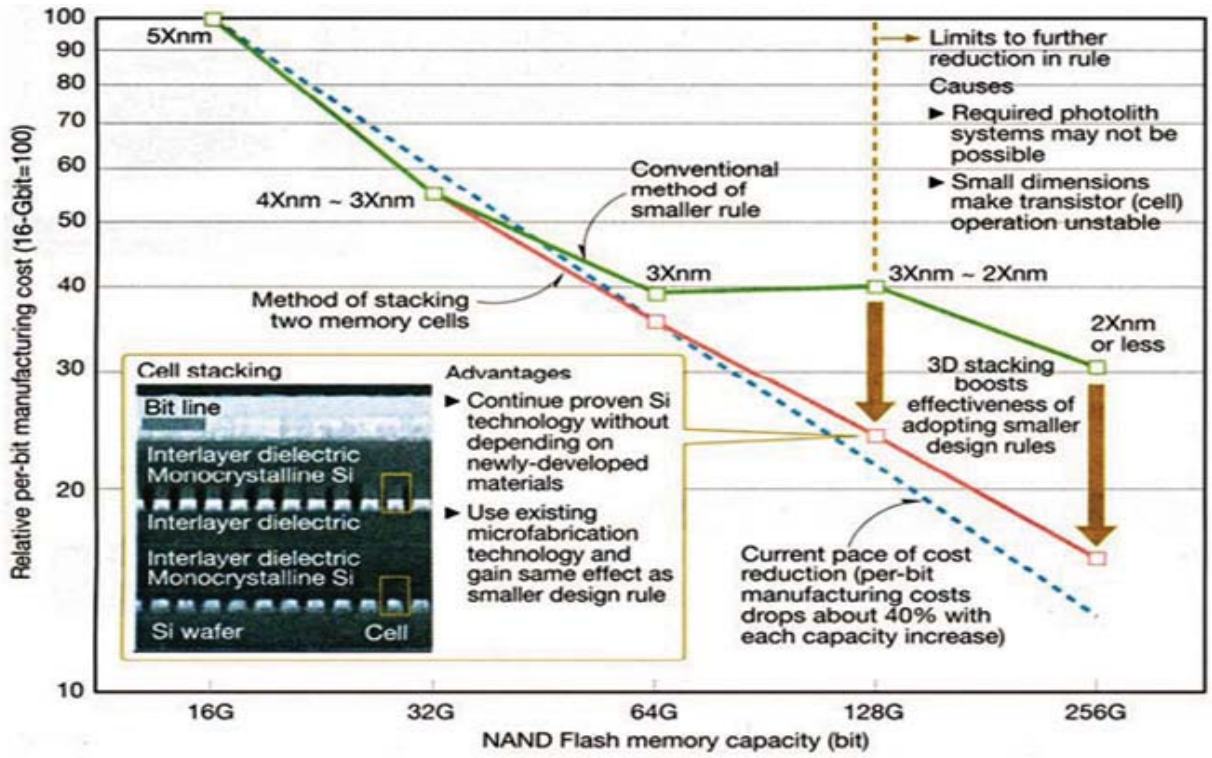

Figure 3-3. Cost of TSV versus the next silicon technology node [41].

3.1.3 Logic

3.1.3.1 Processors

The large bandwidth required to avoid latency issues in the multi-core processor systems of the future can only be addressed by TSV technology. The first application is expected to be cache memory bonded to a processor. A full repartitioning of processors to take advantage of the complete potential of 3D stacking, including low-power consumption and less noise, in the future, requires advances in 3D design tools for repartitioning.

The decision to use die-to-wafer or wafer-to-wafer bonding depends on whether memory-to-logic or logic-to-logic stacking is adopted. Die-level stacking is probably the best choice for logic-plus-memory applications because die stacking enables the stacking of different size die (i.e., SRAM or DRAM and a microprocessor). This type of memory stacking does not require tight-pitch TSV and therefore alignment is less of an issue. Pre-testing both the microprocessor and the memory die is assumed to be relatively straightforward, allowing the advantages of KGD.

In contrast, wafer stacking may be a better choice for logic-plus-logic applications because of its throughput advantages, especially when very precise alignment (tight via pitch) is required, as in the case of repartitioning. Repartitioning for wafer stacking allows die to be made the same size; when the logic is partitioned, it may not be as straightforward to test the individual pieces and select them based on KGD for yield improvement. In this case, die stacking is a less compelling driver.

The first application with TSV technology is expected to start in 2010 at the 32 nm technology node in servers. The die size is assumed to be approximately 9 mm × 9 mm. Stacked processors on DRAM with TSV are not expected until after 2014 [1].

3.1.3.2 FPGA

The benefits of using 3D architecture in logic devices are especially evident in FPGAs. FPGAs consist of large arrays of simple, programmable logic elements with a hierarchy of programmable interconnects that allow the logic blocks to be connected as desired by the system designer. The performance of FPGAs is limited by the configurable interconnect which takes up 90 percent of the chip real estate and accounts for 40 to 80 percent of the device delay.

FPGAs have always had problems with interconnect delays (see Figure 3-4). 3D integration can improve FPGA performance by removing the programmable interconnect from the logic block layer and placing it on another tier in the stack, thus reducing the interconnect delay [42]. FPGAs are one of the early potential applications for 3D TSV, but the availability of design tools at the foundries is critical. Conceptually, memory could also be added as part of the 3D tiers [1].

FPGAs are expected to use TSVs starting as early as 2011, but perhaps as late as 2013, depending on resolving the issues with KGD, cost, and yield [1].

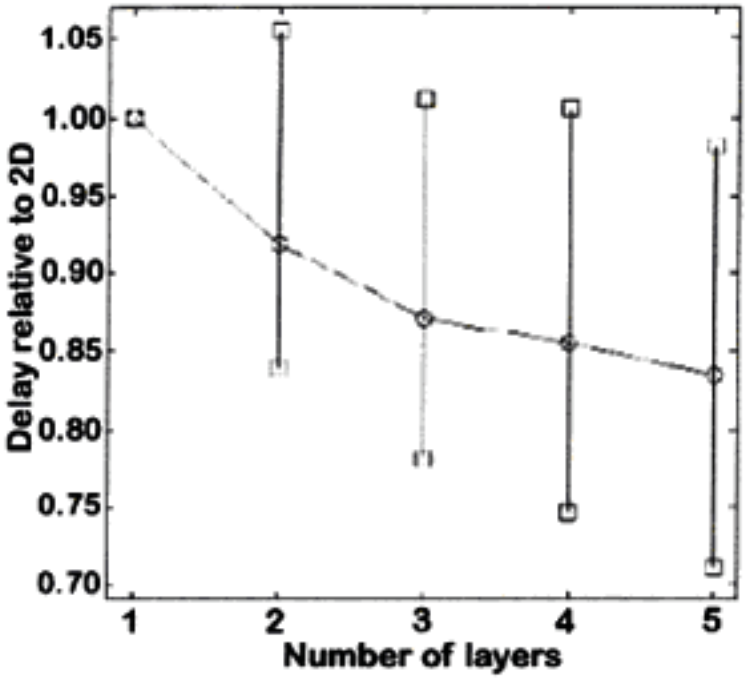

Figure 3-4. Proposed FPGA 3D versus 2D delay [42].

3.2 Image Sensors

Image sensors are one of the first applications to use TSV technology, with production lines already installed at Toshiba and other packaging companies such as Tessera. In general, sensors have not been able to take advantage of the size, weight, and cost advantages of wafer-level packaging (WLP) because sensors need to be connected to the subassembly face up (sensing device). Traditional WLP creates the area array of interconnects over the surface of the IC devices and, therefore, it is mounted face down [43 = 81].

Drivers for assembling sensors in the TSV technology include [39]:

- Small form factor
  - 4.15 × 4.15 × 2.5 mm
- Integrated reflowable module
- Sensor and lens calibration during design avoids costly delays due to sensor mask redesign
  - Time to market
  - Cost savings

Applications include [39]:

- Consumer applications
  - Camera module for mobile phone
  - Form factor driven
- Medical applications
- Military and aerospace applications
  - Performance driven
  - Lower volume

CMOS image sensors are moving into production with TSV technology. The active area of the sensor faces up and the interconnection on the backside of the device is easily obtained by backside formation of the TSV. The SHELLCASE technology, now owned by Tessera (see Figure 3-5), was the first to produce a device with the backside via technology in its optoCSP. SHELLCASE licensees include Xintec in Taiwan, Sanyo in Japan, and China Wafer Level CSP, Ltd., in Suzhou, China [1]. The SHELLCASE wafer-level chip-scale packaging (CSP) technology has shipped in more than one billion image sensors. The innovative technology enables low-cost, highly reliable, small form factor image sensors, making it an ideal solution for camera-enabled mobile devices such as cell phones and PDAs [44].

When connecting and packaging CMOS image sensors, extra care is required to minimize contamination. As pixels in the imaging chips become smaller, particle control in camera module assembly is increasingly challenging. After the devices are coated and packaged, trapped debris is permanently present as flawed (dark) pixels. It is estimated that more than 90 percent of defects are related to particles [46]. Ideally, all manufacturing steps from silicon wafer processing to packaging and assembly would occur in the same clean room to minimize exposure and handling.

3.3 Power Devices

Researchers at Philips (now NXP) have developed a TSV technology for power devices such as vertical trench metal-oxide semiconductor field-effect transistor (MOSFETs) that have active interconnect on the front and backside of the die. In the Philips technology, TSVs are formed in the dicing street and are patterned and plated on only two edges of the slot-shaped vias. This process has not yet been commercialized [1].

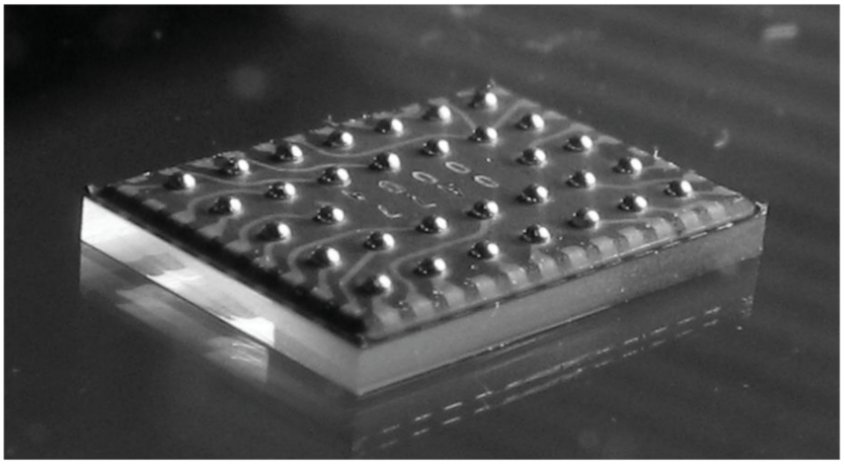

Figure 3-5. Image sensor packaged at the wafer level and provided with a ball grid array (BGA) interface to simplify and cheapen attachment to a printed circuit board. Connection between the die bond pads and the wiring trace attached to the BGA is achieved by a novel through-silicon via (TSV) solution based on via through-pad technology [45].

4 Reliability

4.1 Thermal Issues

Heat dissipation is an extremely important issue in 3D TSV technology. Most of the heat generated in ICs arises from transistor switching and resistance in interconnect. This heat is typically conducted through the silicon substrate to the package and then to the ambient by a heat sink. In multi-tiered 3D device designs, the layers will be insulated from each other by layers of dielectrics (SiO_2, porous SiO_2) that have much lower thermal conductivity than silicon. Thus, the heat dissipation issue becomes even worse for 3D devices and can cause degradation in device performance and reduction in chip reliability due to increased junction leakage, electromigration failures, and acceleration of other temperature-sensitive failure mechanisms.

Chip-cooling techniques can be divided into two categories. One of these is heat sink optimization, which attempts to cool the heat sink through packaging-level cooling techniques such as fans and micro-channels. The other method is thermal conduction to a heat sink. However, in 3D designs, the poor thermal-conducting inner layer dielectric (ILD) layers of the stacked chips impede internal heat dissipation from the heat sources to the heat sink.

Optimizing the internal heat dissipation paths is one of the best thermal dissipation techniques for 3D. This includes temperature-aware physical design tools, thermal via insertion, and 3D IC micro channel techniques [47].

Thermal effects are exacerbated in 3D ICs due to higher power density and greater thermal resistance of the insulating dielectric. This can cause degradation in device performance and chip reliability. It is, therefore, essential to develop 3D-specific design tools that take a thermal co-design approach to address the thermal effects and generate reliable and high performance designs.

A major concern in the adoption of 3D architecture is the increased power densities that can result from placing one computation block over another in the multilayered 3D stack. Because power densities are already a major bottleneck in 2D architectures, the move to 3D architectures could accentuate the thermal problem. Even though 3D chips could offer some respite due to reduced interconnect power consumption (as a result of the shortening of many long wires), it is imperative to develop thermally aware physical design tools. For example, partition design may place highly-loaded, active gates in a layer close to the heat sink.

Thermal issues are more important in application-specific integrated circuit (ASIC) designs than in FPGA architectures because the power densities in ASICs are higher. This is because both the operating clock frequencies and the density of the logic used are much higher in ASICs than in FPGAs [48].

A first-level approach to this problem has been presented as a thermally driven 3D routing algorithm with the planning of thermal vias to reduce temperature, but this does not fully address the issues between thermal vias and routing resources [49]. Thermal vias use valuable routing space, so, algorithms are needed to minimize their usage while placing them in areas where they would make the greatest impact.

Researchers have proposed a temperature-aware 3D global routing algorithm with the insertion of thermal vias and thermal wires to lower the effective thermal resistance of the material, thereby reducing chip temperature [50]. Thermal wires conduct heat laterally within the same layer. Thermal vias perform the bulk of the conduction to the heat sink, while thermal wires help distribute the heat paths over multiple thermal vias.

Efficient thermal via placement may also help to overcome thermal issues produced in the design of 3D ICs. The resulting placements have lower temperatures and thermal gradients, with the use of thermal vias kept to a minimum. Thermal via placement uses 50.3 percent fewer thermal vias to obtain the same 47.1 percent reduction in maximum temperatures that was obtained using the simpler method in which all regions were blindly given the same thermal via densities. The iterative method modifies the thermal conductivities of thermal via regions in order to satisfy a maximum temperature requirement. There is obviously a tradeoff between reducing thermal effects and the percentage of thermal vias used. There is also a tradeoff between routing space and thermal via space that results in a tradeoff between thermal problems and routability. An important observation is that placing thermal vias in areas of high temperature, such as on the uppermost layer, has little impact in reducing thermal issues. This algorithm places thermal vias where they will have the most impact using the thermal gradient as a guide. High temperature can only be reduced by alleviating the high thermal gradients leading up to it.

Since thermal vias and thermal wires take up lateral routing space, the algorithm utilizes sensitivity analysis to allocate their usage judiciously, and resolve the contention between routing and thermal vias and thermal wires. Experimental results show that the routing algorithm can effectively reduce the peak temperature and alleviate routing congestion. Figure 4-1 shows a thermal profile before (a) and after (b) thermal via placement [50].

Thermal design is more complex in 3D ICs than in 2D ICs, as the heat flux might increase proportionally to the number of active layers. Without adequate care, this can lead to elevated temperatures, which can lead to reliability failures such as electromigration, or to timing failures as logic cells might be hotter and slower than assumed. Particular care has to be taken with clock distribution to ensure that the clock buffer temperatures are well known. Because clock buffers are operating all the time, they can easily be hotter than the surrounding logic, and many thermal evaluation tools will not accurately predict the temperature of this relative handful of transistors. Thermal design is particularly difficult in silicon-on-insulator (SOI) design due to the absence of a heat-spreading substrate. Additional TSVs can sometimes be used in the power and ground grids to aid in local heat spreading.

Figure 4-2 shows an example of a detailed temperature map for one layer of a 3D IC. The “tent poles” in this map coincide with locations of the clock buffers. A coarser thermal tool would not resolve these higher temperature points [51].

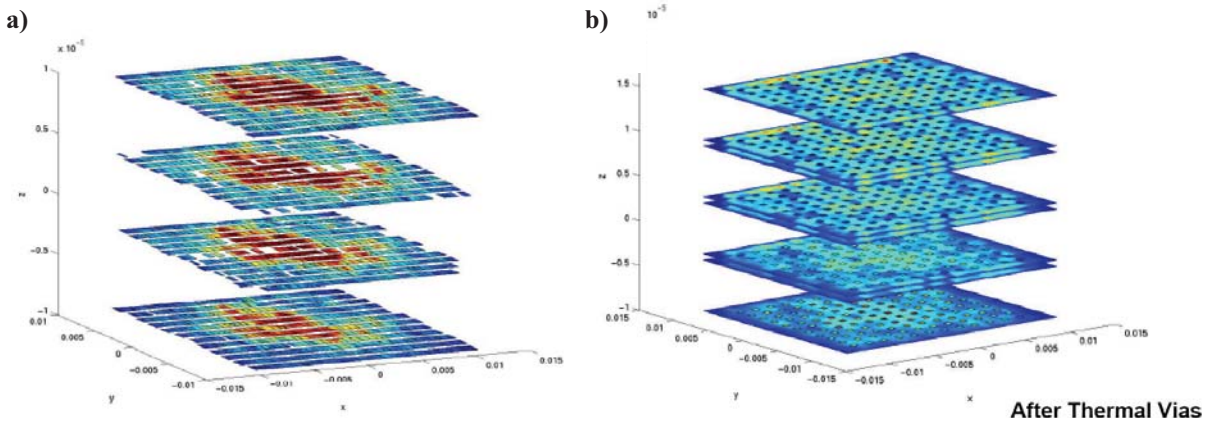

Figure 4-1. Thermal profiles a) without and b) with thermal via placement [50].

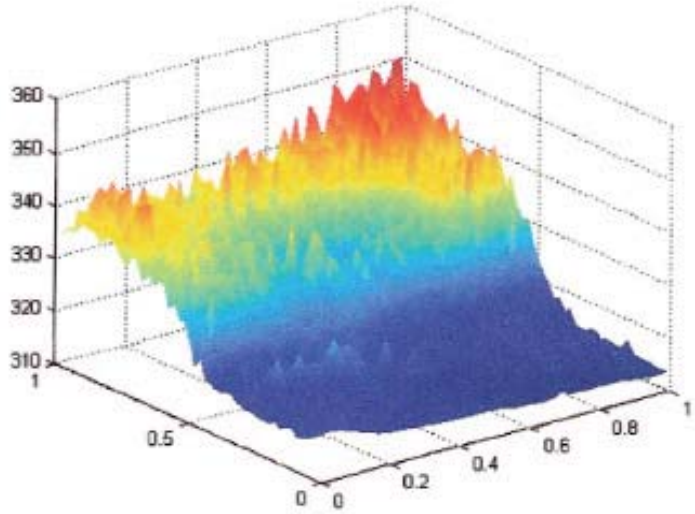

Figure 4-2. Temperature profile of one chip within a 3D stack [51].

I/O planning is also more complicated in 3D design than in 2D design. Usually the most power-hungry chip in the stack is placed near the heat sink. Thus, the I/O solder bumps or wire bonds will be placed on a chip further down in the stack that draws less power. The current needed by the most power-hungry chip has to be delivered through the rest of the stack, and high-speed I/O must also be provided. Careful design of the delivery via structures will be needed to ensure high quality power and signal integrity.

4.2 Various 3D Stacking Technologies

Ziptronix, based in Morrisville, NC, near Research Triangle Park, is a spin-off of Research Triangle Institute (RTI). The company's patented DBI™ technology is a direct oxide bond technology in which formation of electrical interconnects is integrated into the bonding process.

Direct oxide bonding typically consists of joining two surfaces that have been activated to form hydroxyl bonds (OH groups) on their surfaces. The Ziptronix technology activates the surfaces with amine groups. Ziptronix reports that this allows for the formation of stronger bonds at lower

temperatures while eliminating the formation of water (steam) that can cause voids at the interface during normal thermal annealing (ammonia is eliminated at room temperature).

In an initial reliability study using temperature cycling and HAST testing of a 72,500 daisy chain on 25 μm pitch, no failures were observed as determined by change in resistance (see Table 4-1).

Raytheon Vision Systems has reported that the Ziptronix DBI technology is compatible with multilayer CMOS IC processes. Demonstration of the compatibility involved the 3D integration of a five-layer metal, 0.5 μm CMOS high-performance imaging device for applications, including focal plane imagers and high-performance sensor arrays. Parts were fabricated in a die-to-wafer format. Demonstration of 100 percent focal plane pixel operability was accomplished [52].

NEC Electronics, Oki Electric Industry, and Elpida Memory developed a general-purpose 3D-LSI platform technology for a high-capacity stacked memory integrated on a logic device [53-57]. To accomplish this, they developed a TSV daisy chain test vehicle with 8-strata as shown in Figure 4-3 [58].

As shown in Figure 4-3, the stacked sample was mounted onto a ceramic carrier, gold wires were bonded onto it, and the sample was sealed. Electrical tests were carried out using a ceramic carrier package. Measured electrical resistances of daisy-chain circuits are shown in Figure 4-4. From these results, the estimated resistance of individual poly-Si TSVs was shown to be approximately 4.1Ω.

Table 4-1. Ziptronix DBI interconnect reliability data [52].

Test Part	50 μm Pitch	25 μm Pitch	10 μm Pitch
Test Part	9,950 Serial Connections	72,500 Serial Connections	460,000 Serial Connections
Typical Resistivity	<20 mΩ (<1.5 Ω/μm$^{2)}$	<50 mΩ (<0.5 Ω/μm$^{2)}$	<50 mΩ (<0.5 Ω/μm$^{2)}$
Thermal Cycling –65°C to 175°C	1,000 Cycles, 18/18 Pass 10,000 Cycles, 9/9 Pass	1,000 Cycles, 5/5 Pass 10,000 Cycles, 4/4 Pass	1,000 Cycles, 10/10 Pass
HAST (130°C, 85% RH, 333 psi)	96 Hours, 12/12 Pass	288 Hours, 6/6 Pass	

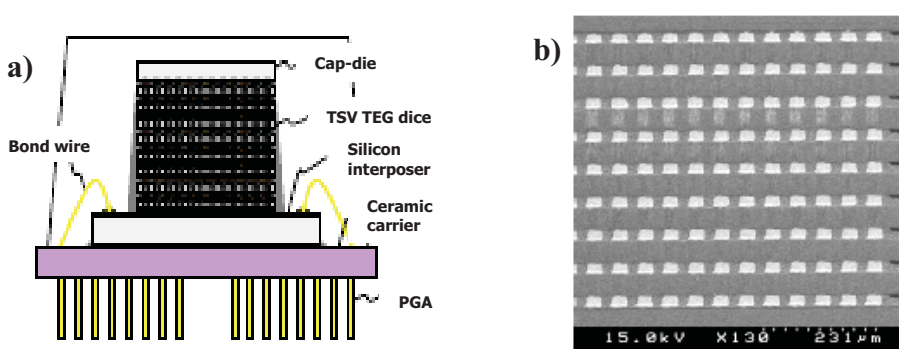

Figure 4-3. a) Electrical test sample structure of stacked dice with TSV; b) Cross-sectional SEM image of complete stack of 8-strata TSV-TEG dice and cap-die on silicon interposer [58].

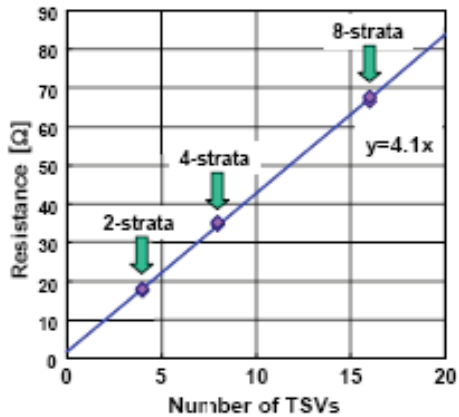

Figure 4-4. Electrical test result of daisy-chain circuit illustrating TSV resistance [58].

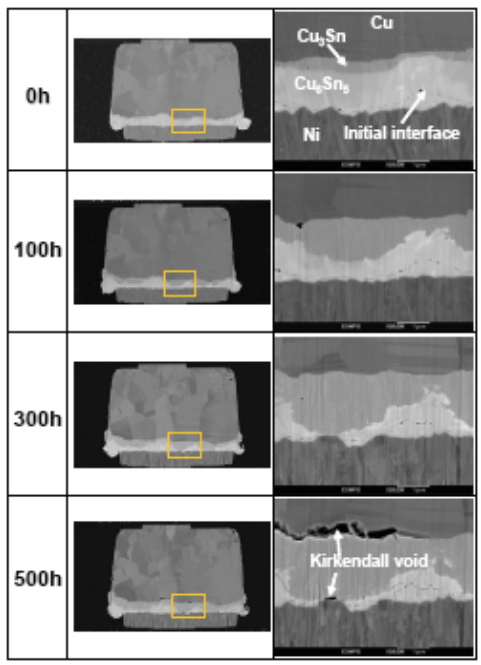

Figure 4-5. Fixed-point cross-sectional observation of the aging behavior of micro-bump interconnection during thermal aging at 150ºC [58].

A high-temperature storage test of micro-bump interconnections was carried out using a stacked TSV test vehicle sample. The baked sample was treated with a focused ion beam (FIB) technique and SEM observation was repeated. These processes were repeated at 0 (initial condition), 100, 300, and 500 hours of aging. The SEM observation results are shown in Figure 4-5. Soon after bond forming, Cu_6Sn_5 showed as the dominant intermetallic layer and tin oxide involving small voids was observed at the initial interface near the Ni surface. A Cu_3Sn layer of approximately 0.4 μm was formed on the Cu interface. As the aging progressed, the Cu_3Sn intermetallic layer grew from the Cu pillar bump side to the Ni bump side, and reached the Ni surface at 300 hours. At 500 hours, Kirkendall voids were observed at the interface of the Cu/Cu_3Sn and Cu_3Sn/Ni layers. During this aging process, the growth of the Ni-Sn intermetallic layer was not observed. This indicates that Cu supplied from pillar bumps in Sn solder may have suppressed Ni diffusion into solder [58], and could prevent the degradation of the thin backside bumps.

Wafer-level 3D packaging for optical image sensor devices developed by Schott Advanced Packaging utilizes TSV technology by contacting the bond pads of the image sensors from the backside. Direct contact of the bond pads from the back side of the chip offers much shorter transmission paths to the board assemblies, thus providing faster signal speed, lower ohmic contact, and efficient thermal conduction [59, 60].

Via shape and a controlled spray coating process are the key to achieve good quality and reliable product [61]. In the very first process steps, a wafer, comprised of the optical sensor area and the bond pads, is bonded to a glass wafer using a clear optical adhesive. Then the wafer is thinned down to thicknesses between 85 µm to 125 µm to be prepared for plasma etching. Figure 4-6a illustrates the bonded and thinned wafer of this process step. It should be noted that above the bond pads, there is always an inter-layer dielectric of silicon oxide. The next step is to create vias that are needed to contact the bond pads through the silicon and thus enable an electrical connection. Depending on the process parameters of the plasma process, a variety of via shapes can be generated. Figure 4-6b shows the wafer after plasma etching.

Polymer material is then spray coated onto the wafer, which serves as an interlayer dielectric to prevent shorts when the redistribution is done (Figure 4-7).

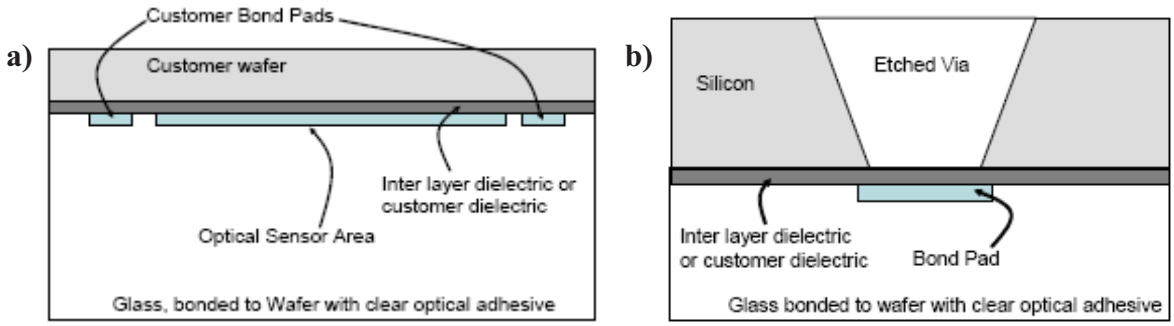

Figure 4-6. a) Bonded and thinned wafer and b) wafer with etched vias [61].

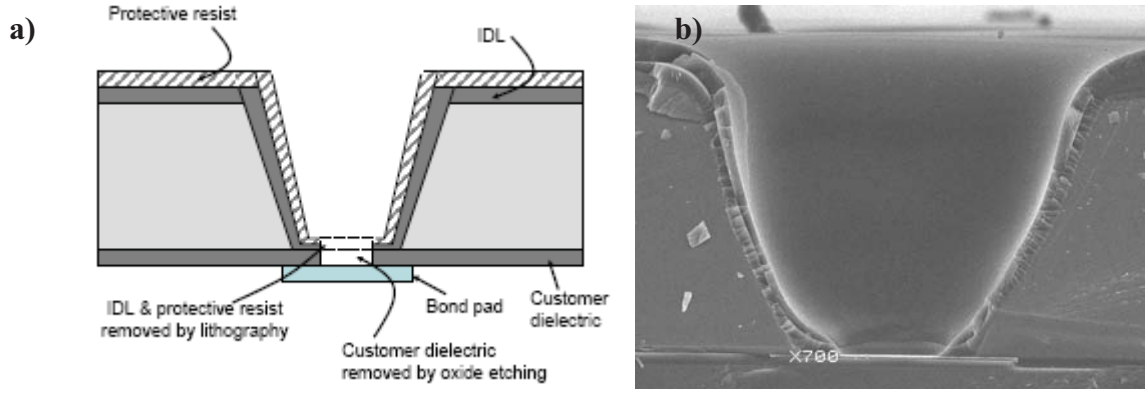

Figure 4-7. a) Illustration of a wafer with IDL, protective resist, and opened dielectric layer; b) SEM photomicrograph of a) [61].

In order to establish an electrical contact of the solder bumps to the bond pads, the dielectric layer (particularly above the bond pads) is removed by a highly selective oxide etch process.

Reliability results are related to the electrical testing of the devices. For each device, there are 74 I/Os. If any one or more of these I/Os shows an electrical failure due to open circuit or short circuit, that particular chip is considered a fail. Schott's electrical yield varies from 92% to 96% from lot to lot. Apart from electrical tests, the chips are also subjected to reliability tests according to JEDEC standards.

These tests include:

1. Pre-conditioning test:
   a. Bake out: Bake the device for 24 hours at 125° C (+ 5 / –0°C) (Std - JESD22-A113E and JEDEC J-STD-020C)
   b. Moisture Soak: Soak the device for 72 hours at 30°C / 60% RH (Std - JEDEC J-STD-020C, Table 5-1, Level 4)
   c. Reflow: Subject the device to three cycles of 260°C for 20 seconds (Std - JEDEC J-STD-020C, Table 5-2, Pb-Free Assembly)
2. Temperature humidity storage (THS) test: 85°C at 85% RH (JESD22-A101). The chips are subjected to 168, 500, and 1000 hours.
3. Temperature cycling test (TCT): –40°C / +85°C (JESD22-A104). The chips are subjected to 100, 200, 300, 500 and 1000 cycles.

After each cycle, the chips go for electrical test to check for any abnormalities that can cause electrical failures. Tables 4-2 and 4-3 show the result of THS and TCT tests, respectively.

The data shows that this version of TSV survived up to THS 1000 hours and TCT 1000 cycles.

Table 4-2. Result after THS for 30 chips [61].

Reliability Test Description	Test Condition	Wafer ID	Sample Size	Number of Hours		
				168 hours	500 hours	1000 hours
				Electrical Test	Electrical Test	Electrical Test
Temperature Humidity Storage Test (THS)	85°C / 85% RH (JESD22-A101)	6697-20	12	0/12	0/12	0/12
		6697-23	7	0/7	0/7	0/7
		6697-25	11	0/11	0/11	0/11

Table 4-3. Result after TCT for 30 chips [61].

Reliability Test Description	Test Condition	Wafer ID	Sample Size	Number of Hours				
				100 Cycles	200 Cycles	300 Cycles	500 Cycles	1000 Cycles
				Electrical Test	Electrical Test	Electrical Test	Electrical Test	Electric al Test
Temperature Cycling Test (TCT)	–40°C / +85°C (JESD22-A104, Condition N with Soak Mode 3)	6697-20	12	0/12	0/12	0/12	0/12	0/12
		6697-23	7	0/7	0/7	0/7	0/7	0/7
		6697-25	11	0/11	0/11	0/11	0/11	0/11

5 Conclusions

Through-silicon via is the latest in a progression of technologies for stacking silicon devices in 3D. Driven by the need for improved performance, methods to use short vertical interconnects to replace the long interconnects found in 2D structures have been developed. The industry is moving past the feasibility (R&D) phase for TSV technology into the commercialization phase where economic realities will determine when the technology will be adopted.

Even with the advantages of 3D ICs, there are several challenges to the adoption of 3D architectures:

- Commercial availability of electronic design automation (EDA) tools and design methodologies
- Thermal concerns due to the increased power densities
- Test, especially for repartitioned logic

3D integration technology will not become commercially viable without the support of EDA tools and methodologies that will allow circuit designers to use the technology. Design tools remain a weak link in the 3D infrastructure, with better thermal modeling, finite-element analysis, floor planning, and layout tools all required for a smooth 3D design flow. Because of this, 3D integration has been limited to applications such as image sensors, and has not been easily applied to the design of complex 3D microprocessors and ASICs where it could have the most pronounced impact.

Several companies and organizations are designing 3D memory stacks that can be used to replace individual memory die in many applications requiring more capacity than can be provided by one die. Examples include increased flash and DRAM capacity. Stacking memory die like this requires little redesign, except for the need to include space for the TSVs. Through clever design, it is possible to use identical die at every portion in the stack. Table 5-1 shows examples of different styles of 3D designs.

The next level of complexity is needed when memory is stacked on top of logic. Such integration is desirable for many reasons, as discussed in the previous sections. Though design complexity is increased over that of a 3D memory stack, the clear functional partitioning makes it an easier design target than logic-on-logic. Fortunately, the required via density between the memory and logic layers is relatively modest, though higher than in the pure memory stack.

Table 5-1. Different styles of 3D design [51].

Style	Main Characteristics	Comments
3D Memory Stack	Stacked identical memories designed only for the purpose of increasing capacity, by making a "super-chip."	Simple redesign of existing memories. Requires only coarse vias.
Memory-on-logic	Custom memory, e.g., DRAM or cache integrated on top of a logic die, for a CPU or ASIC application.	Requires finer vias. Logic power delivery usually through the memory stack.
Logic-on-logic	Redesign logic function to benefit from interconnect advantages of stacked 3D ICs.	Benefits most from smaller vias on a narrower pitch.
Logic-on-analog	Optimized logic process wafer on top of optimized analog process wafer. Provides optimal cost/technology mix and can improve noise isolation.	Coarse via pitch OK. Have to demonstrate advantage over packaging option.
Mixed Technology (Heterogeneous) Integration	Tightly integrated mixed technology (e.g., MEMS, GaAs or InP on silicon, or imaging array layer on silicon) can bring many system advantages.	Via needs are very application specific. Could enable silicon photonics and a broad range of other applications.

The highest level of complexity, for an all-silicon system, would be to design a pure logic-on-logic system. This has been heavily explored by both industry and academia for CPUs, FPGAs, and some DSP functions. It has the highest complexity because it benefits greatly from very fine, micron-scale through-vias, and requires intensive study of possible partitioning options. Other complexities introduced include test and debug, and larger process variations.

In comparison to logic-on-logic, logic-on-analog (or RF) has not been explored very much. Part of the reason for this is that most mixed signal applications have low interconnect requirements between the digital and analog functions, and these requirements can usually be met with a packaging approach. Nonetheless, some applications are being explored in this realm, including mm-wave circuits and tight digital control of RF power amplifiers.

The primary points of difference between 2D and 3D IC design are summarized in Table 5-2. This table focuses mainly on memory-on-logic and logic-on-logic designs. One obvious issue that has to be dealt with is partitioning. For memory-on-logic, the functional partitioning is clear. However, careful floor planning is desirable so as to best align the memory bandwidth with the logic functions that require it. Emerging physical standards for memory stack integration via locations will ease this issue somewhat. Such standards will also be needed to ensure multiple sourcing.

For logic-on-logic 3D ICs, partitioning is much more complex. It can be done at the floor plan, standard cell, or even circuit (transistor) level, depending on the sophistication of the tools and designer. Issues to consider during partitioning include area minimization, power minimization, interconnect circuit performance, heat flux density, clock distribution, yield and test. If die are to be tested to ensure KGD before a die-on-wafer integration, the partitioning options are limited by the available test points. On the other hand, if wafer-on-wafer integration is planned, testing before integration has relatively little value, as there are few options available to not using the bad die. In this situation, the 3D die could be treated as one integrated structure for design purposes (and for yield prediction). Another complication would be the added inter-transistor variation that will be present between transistors in different source wafers. Another difficult issue with logic-on-logic 3D ICs is the added mask, etc., costs of designing two wafers at once. In contrast, memory-on-logic parts will most likely reuse standard 3D memory parts.

Table 5-2. Differences between 2D and 3D design [43].

Design Issue	Main Difference(s) in 3D	Comments
Partitioning	Have to decide on partitioning of functions between die in the stack. Lack of standards for integratable memory functions to enable multi-sourcing.	Relatively easy for memory-on-logic but can be hard for logic-on-logic. Issues include performance, process variations, yield, test and debug.
Yield and Test	Have to decide if parts are to be tested before or after integration.	If using die-on-wafer integration, pre-testing is possible and potentially worth the effort for larger die.
Debug	How to debug when functions are partitioned and observability is difficult?	None
Thermal Design	Total heat flux is higher. It can be difficult to cool interior functions.	None
Power and I.O Provisioning	Power and ground current delivery and I/O might have to be built through complex via stacks.	None

Even with design tool shortcomings, TSVs have numerous end uses (memory, logic, power and sensors) that are pulling the technology. In other words, it is not a technology looking for a problem to solve—there are plenty of problems that need solving. There are numerous companies that have TSVs on their technology roadmaps, which will make this a technology NASA will need to evaluate.

6 Recommendations

TSV is the type of technology that requires close watch for commercial applications that could be of interest to NEPP and NASA flight projects. There are a number of companies that are extremely active in this field.

Work in this area has already reached “critical mass” such that in the near future there will most likely be products introduced using TSVs because of the advantages this technology offers in the area of 3D integration.

This technology is not mature enough to start new work in the coming FY; therefore, no new NEPP task is recommended for FY2010. However, implementation of this technology is moving quickly and a proposal in FY2011 should be considered.

7 References

[1] P. E. Garrou, E.J. Vardaman. and P.D. Franzon, "Through Silicon Via Technology: The Ultimate Market for 3D Interconnect," *Tech Search International*, January 2008.

[2] D. M. Jang, C. Ryu1, K. Y. Lee, B. H. Cho1, J. Kim, T. S. Oh, W. J. Lee. and J. Yu, "Development and Evaluation of 3-D SiP with Vertically Interconnected Through Silicon Vias (TSV)," *Proceedings of the Fifty-Seventh Electronic Components and Technology Conference*, May 29–June 1, 2007, pp. 847–852.

[3] Y. Tomita et al., "Advanced Packaging Technologies on 3D Stacked LSI utilizing the Micro Interconnections and the Layered Microthin Encapsulation," *Proceedings of the Fifty-Seventh Electronic Components and Technology Conf*, Orlando, FL, May 2001, pp 353–360.

[4] K. Hara et al., "The Optimization of Terminal Structure for Interconnections in 3D Packaging Technology with Through-Silicon Vias," International Conference on Electronics Packaging, Tokyo, Japan, 2005, pp. 161–166.

[5] K. Y. Lee et al., "New Chip-on-glass and Flip-chip Processes Using Interlocking Bump Structure Fabricated by Electrodeposition," 208th ECS Meeting, Los Angeles, California, 2005, abs# 683.

[6] J. U. Knickerbocker et al., "Development of next generation systeom-on-package (SOP) technology based on silicon carriers with fine-pitch interconnection," *IBM J. Res. & Dev.* 49(4/5), pp. 725–754, 2005.

[7] Y. Akasaka, "Three-dimensional IC trends," *Proc. IEEE* 74(12), pp. 1703–1714, Dec. 1986.

[8] K. Sakuma et al., "A New Wafer-Scale Chip-on-Chip (WCOC) Packaging Technology Using Adhesive Injection Method," *Proceedings of the 1998 International Conf. on Solid State Device and Materials*, pp. 286–287

[9] M. Koyanagi et al, "Future System-on-Silicon LSI chips," *IEEE MICRO* 18(4), pp. 17–22, Jul/Aug. 1998.

[10] A. Klumpp et al, "Chip-to-Wafer Stacking Technology for 3D System Integration," *Proceedings of the 53th Electronic Components and Technology Conference*, San Diego, CA, pp. 1080–1083, 2003.

[11] K. W. Lee et al., "Development of three-dimensional integration technology for highly parallel image processing chip," *Jpn. J. Appl. Phys.* 39(4B), pp. 2473–2477, Apr. 2000.

[12] K. Takahashi et al., "Development of Advanced 3-D Chip Stacking Technology with Ultra-Fine Interconnection," *Proceedings of the 51st Electronic Components and Technology Conference*, p. 541, 2001.

[13] K. Hara et al., "Optimization for Chip Stack in 3-D Packaging," *IEEE Transactions on Advanced Packaging* 28(3), pp. 367–376, Aug. 2005.

[14] K Sakuma, P.S. Andry, B. Dang, J. Maria*, C.K. Tsang, C. Patel, S.L. Wright, B. Webb, E. Sprogis**, S.K. Kang, R. Polastre, R. Horton, and J.U. Knickerbocker, "3D Chip Stacking Technology with Low-Volume Lead-Free Interconnections," *Proceedings of the* 57th *Electronic Components and Technology Conference*, p. 627, 2007.

[15] P. Ludec, "What is 3D Integration and What Metrology is Needed," *Conference on Frontiers of Characterization and Metrology for Nanoelectronics,* NIST, March 2007.

[16] M. Scannell, "CEA CEA-Leti 3D Activities and Roadmap," presented at EMC-3D "European Technical Symposium Minatec," June 29, 2007.

[17] B. Ault, J. Bums, C. Chen, B. Felton, H. Hanson, C. Keast, J. Knecht, A. Loomis, M. Renzi, A. Soares, V. Suntharalingam, K. Warner, D. Yost, and D. Young, "Laser Radar Imager Based on 3D Integration of Geiger-Mode Avalanche Photodiodes and Two 501 Timing Circuit Laters," *IEEE ISSSC Proceedings,* pp.1179–1188, February 2006.

[18] K. Banerjee, S. Souri, P. Kapur, and K. Saraswat, "3-D les: A Novel Chip Design For Improving Deep-Submicrometer Interconnect Performance and Systems-on-Chip Integration," *IEEE Proceedings* 89(5), 2001.

[19] A. Rahman, Fan, R. Reif, "Comparison of Key Performance Metrics in Two and Three Dimensional Intergrated Circuits," *International Interconnect Technology Conference Proceedings,* 2000, pp. 18–20.

[20] S. Das, A. Chandrakasan, and R. Rei£, "Timign, Energy and Tehrmal Performance of Three Dimensional Integrated Circuits," *Proceedings Great Lakes Symposium on VLS,* 2004, pp. 338–343.

[21] H.P. Hofstee, "Future Microprocessors and Off-chip SOP Interconnect," *IEEE Transactions Advanced Packaging* 27(2), May 2004, pp. 301–303.

[22] A. Rahman, S. Das, A. Chandrakasan, and R. Rei£, "Wiring Requirement and Three-Dimensional Integration Technology for Field Programmable Gate Arrays," *IEEE Transactions VLSI* 11(1), pp. 44–54, February 2003.

[23] J. Vardaman, "3-D Through-Silicon Vias Become a Reality," *Semiconductor International,* pp. 37–40, June 2007.

[24] S. Denda, "New Concepts in Flipchip Bump Technology (Session Invite)," ICEP2008, International Conference on Electronics Packaging, Tokyo, Japan, June 10–12, 2008.

[25] P. Garrou, "Wafer Level 3D Integration," presented at Peaks in Packaging Whitefish Montana, Sept. 5–7, 2007.

[26] R. Toftness et al., "Laser Technology for Wafer Dicing and Microvia Drilling for Next Generation Wafers," *Proceedings SPIE* 5713, p. 54, 2005.

[27] A. Rodin, "High Throughput Laser Via and Dicing Process," *Peaks in Packaging Proceedings,* Whitefish, Montana, September 2007.

[28] N. Brennan, J. Callaghan, M. Hannon, and A. Rodin, "High-Throughput Laser Percussion Interconnect Microvia Process," presented at 'Be-Flexible' in Munich, Germany, December 5–6, 2007.

[29] A. Topol et al., "3D Integrated Circuits," *IBM Journal of Research and Development* 50, p. 491, July/Sept 2006.

[30] L. Hashim, V. Pavate, P. Ding, B. Chin, D. Brown, and T. Nogami, "IMP Ta/Cu Seed Layer Technology for High Aspect Ratio Via Fill," *SPIE* 3508, Multilevel Interconnect Technology II, M. Graf, D. Patel Editors.

[31] B. Cho, and W. Lee, "Filling of Very Fine Via Holes for 3D SiP by using Ionized Metal Plasma Sputtering and Electroplating," *International Conference Electronic Packaging,* Tokyo Japan, pp. 384–385, 2007.

[32] D. M. Jang et al., "Development and Evaluation of 3D SiP with Vertically Interconnected TSV," *2007 ECTC Proceedings,* p. 847.

[33] R. Puligadda et al., "High Performance Temporary Adhesives for Wafer Bonding Applications," MRS Proceed. V. 970, Enabling Technologies for 3D Integration. C. Bower, P. Garrou, P. Ramm, K. Takahashi Editors, 2007, p. 239.

[34] P. Enquist, "Direct Bond Interconnect for Advanced Packaging Applications," *SMT A 3D/SiP Advanced Packaging Symposium,* May 2007.

[35] Y. Los, R. Frye, and K. O'Connor, "Design Methodology for Chip-on-Chip Applications," *IEEE Transactions CPMT, Part B,* Volume 21, p. 298, 1998.
[36] M. Uno, "Chip-on-Chip Offers Higher Memory Capacity, Speed," *Nikkei Electronics Asia,* pp. 28–32, February 2007.
[37] "Samsung Develops New, Highly Efficient Stacking Process for DRAM," *Semiconductor International,* April 22, 2007.
[38] H. Ikeda, "3D Stacked DRAM Using TSV," Plenary Session, *ECTC,* May 2007.
[39] J. Vardaman, "Applications for TSV and Issues for Adoption," presented at workshop, entitled "Manufacturing and Reliability Challenges for 3D ICs using TSVs," at the Advanced Metallization Conference (Sematech), San Diego, CA, September 23–25.
[40] K. Lee, "Next Generation Package Technology for Higher Performance and Smaller Systems," 3D *Architectures for Semiconductor Integration and Packaging Conference, B*urlingame, CA, 2006.
[41] M. Ooishi, "Vertical Stacking to Redefine Chip Design," *Nikkei Electronics Asia,* April 2007, pp. 20–26.
[42] C. Ababei and K. Bazargan, "Exploring Potential Benefits of 3D FPGA Integration," Book Series Lecture Notes in Computer Science, Field Programmable Logic and Application, Springer Berlin, pp. 874–880, 2004.
[43] M. Toepper and P. Garrou, "The Wafer Level Packaging Evolution," *Semiconductor International,* p. SP-l3, October 2004.
[44] "Tessera's SHELLCASE Technology Shipped in One Billion Image Sensors," Reuters (on-line), Jan. 26, 2009, http://www.reuters.com/article/pressRelease/idUS82857+26-Jan-2009+BW20090126
[45] G. Humpston, "Novel and Low Cost Through Silicon Via Solution for Wafer Scale Packaging of Image Sensors," *Proceedings of Electrical Design of Advanced Packaging and Systems (EDAPS 2008)*, Seoul, Korea, December 10–12, 2008.
[46] A. Chowdury, Camera Module Assembly and Test Challenges, *Semiconductor International,* February 2006.
[47] J. Cong et al., "An Automated Design Flow for 3D Microarchitecture Evaluation," *Proceedings IEEE Asia and South Pacific Conference on Design Automation,* p. 384, 2006.
[48] C. Ababei et al., "Placement and Routing in 3D ICs," *IEEE Design and Test of Computers,* p. 520, 2005.
[49] J. Cong and Y. Zhang, "Thermal Driven Multilevel Routing for 3D ICs," *Proceedings ASPDAC,* pp. 121–126, 2005.
[50] T. Zhang, Y. Zhan, and S. Saptnekar, "Temperature Aware Routing in 3D les," *IEEE Asia and South Pacific Design Automation Conference,* p. 309, 2006.
[51] Paul D. Franzon, W. Rhett Davis, Michael B. Steer, Steve Lipa, Eun Chu Oh, Thor Thorolfsson, Samson Melamed, Sonali Luniya, Tad Doxsee, Stephen Berkeley, Ben Shani, Kurt Obermiller, "Design and CAD for 3D Integrated Circuits," *Proceedings of the 45th Annual Conference on Design Automation Table of Contents*, Anaheim, California, p. 668.
[52] L. Peters, "Ziptronix, Raytheon Prove 3-D Integration of O.5~m CMOS Device," *Semiconductor International,* April 6, 2007.
[53] Y. Kurita, K. Soejima, K. Kikuchi, M. Takahashi, M. Tago, M. Koike, Y. Morishita, S. Yamamichi, and M. Kawano, "Development of High-Density Inter-Chip-Connection

Structure Package," *Proc. of 15th Micro Electronics Symposium (MES 2005)*, Osaka, Japan, p. 189, Oct. 2005.

[54] M. Takahashi, M. Tago, Y. Kurita, K. Soejima, M. Kawano, K. Kikuchi, S. Yamamichi, and T. Murakami, "Inter-chip Connection Structure through an Interposer with High Density Via," *Proc. of 12th Symposium on Microjoining and Assembly Technology in Electronics (Mate 2006)*, Yokohama, Japan, p. 423, Feb. 2006.

[55] Y. Kurita, K. Soejima, K. Kikuchi, M Takahashi, M. Tago, M Koike, K. Shibuya, S. Yamamichi, and M. Kawano, "A Novel 'SMAFTI' Package for Inter-Chip Wide-Band Data Transfer," *Proc. of 56th Electric Components and Technology Conference*, San Diego, CA, p. 289, May/June 2006.

[56] K. Nanba, M. Tago, Y. Kurita, K. Soejima, M. Kawano, K. Kikuchi, S. Yamamichi, and T. Murakami, "Development of CoW (Chip on Wafer) bonding process with high density SiP (System in Package) technology 'SMAFTI,'" *Proc. of 16th Micro Electronics Symposium (MES 2006)*, Osaka, Japan, p. 35, Oct. 2006.

[57] F. Kawashiro, K. Abe, K. Shibuya, M. Koike, M. Ujiie, T. Kawashima, Y. Kurita, Y. Soejima, and M. Kawano, "Development of BGA attach process with high density Sip technology "SMAFTI," *Proc. of 13th Symposium on Microjoining and Assembly Technology in Electronics* (Mate 2007), Yokohama, Japan, p. 49, Feb. 2007.

[58] Y. Kurita, S. Matsui, N. Takahashi, K. Soejima, M. Komuro, M. Itou, C. Kakegawa1, M. Kawano, Y. Egawa, Y. Saeki, H. Kikuchi, O. Kato, A. Yanagisawa, T. Mitsuhashi, M. Ishino, K. Shibata, S. Uchiyama, J. Yamada, and H. Ikeda, "A 3D Stacked Memory Integrated on a Logic Device Using SMAFTI Technology," *Proc. of 2007 Electronic Components and Technology Conference*, Reno, NV, p. 821, May 2007.

[59] J. Leib and M. Topper, "New Wafer-Level Packaging Technology Using Silicon-Via-Contacts for Optical And Other Sensor Applications," Proceedings of the *54th Electronic Components and Technology Conf*, Las Vegas, 2004.

[60] G. Viswanadam, F. Bieck and N. Suthiwongsunthorn, "Novel Wafer Level Package Technology Studies for Image Sensor Devices," *Electronic Packaging and Technology Conf, Singapore*, 2005.

[61] D. Shariff, N. Suthiwongsunthorn, F. Bieck, J. Leib, "Via Interconnections for Wafer Level Packaging: Impact of Tapered Via Shape and Via Geometry on Product Yield and Reliability," Proceedings of the *57th Electronic Components and Technology Conf*, Reno, NV, p. 858, 2007.