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Reliability of Low-Pitch, High-I/O Area Array Packages

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Objectives and Products

Commercial-off-the-shelf area array packaging (COTS AAP) technologies in high reliability versions are now being considered for use in a number of National Aeronautics and Space Administration (NASA) electronic systems. Understanding the process and quality assurance (QA) indicators for reliability are important for low-risk insertion of these newly available packages. This report first summarizes the body of knowledge (BoK) on high-input/output (I/O) plastic ball grid array (PBGA) and low-pitch chip scale package (CSP) technologies. It then presents assembly thermal cycle reliability test results for assemblies of PBGA packages with 256 and 1156 I/Os with 1-mm pitch, a CSP package with 192 I/Os, a small flip chip die, two sizes of newly available microlead frame packages (MLFs), two thin small outline packages (TSOPs), and three resistor sizes: 0603, 0402, and 0201. Packages were assembled onto printed wiring board (PWB) using standard tin-lead solder alloy approved for NASA applications. Finally, the report provides QA indicators and qualification guidelines generated based on the test results for the high-I/O and low-pitch packages and assemblies. The qualification guidelines based on test results will facilitate NASA projects to use very dense and newly available packages reliably, allowing more processing power in a smaller board footprint and lower system weight.

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1. Organization and Topics of Report

This report first provides a body of knowledge (BoK) survey for designing, manufacturing, and testing high-input/output (I/O) and low-pitch area array packages. It then presents test data on design, assembly, and environmental evaluation results for various newly available electronics packages assembled onto printed wiring boards (PWBs). Packages included plastic ball grid arrays (PBGA) with I/Os up to 1156 and 1-mm pitch, high-I/O chip scale packages (CSPs), low-pitch flip chip, microlead frame/quad flat no lead (MLF/QFN), and small resistors to 0201 size. Finally, it summarizes lessons learned from test results for assembly and environmental testing along with optical, scanning electron microscopy (SEM), and x-ray photomicrographs showing damage progress. Topics discussed in this report are as follows:

- Executive summary providing key background information, test results, and lessons learned.
- Summary of key parameters that affect assembly reliability of PBGA and flip-chip BGA (FCBGA) with tin-lead solder based on a comprehensive literature search.
- Literature survey and test results for a commercial-off-the-shelf (COTS) PBGA 676 I/O package assembly with various ball/solder alloys representing the current migration of industry to lead-free. A number of test vehicles assembled and supplied by an engineering manufacturing services (EMS) company were subjected to thermal cycling evaluation as part of a collaboration activity.
- Quality assurance documentation of manufacturing processes, including solder paste volumes and photomicrographs of paste deposition showing uniformity and distribution. Representative processing data for high-I/O, low-pitch, QFN, and passive chip resistors were presented.
- Reliability test results including shock and shear test data for the test vehicle jointly designed in collaboration with a university.
- Quality assurance documentation of solder joint assembly for the test vehicle built at the Jet Propulsion Laboratory (JPL) using tin-lead solder paste and reflowed using a vapor phase reflow machine.
- Quality assurance documentation of solder joint damage progress due to thermal cycling performed under three cycle conditions. Thermal cycles were in the range of -55° to $+100^{\circ}\text{C}$, -55° to $+125^{\circ}\text{C}$, and $-120^{\circ}/+85^{\circ}\text{C}$.
- X-ray characterization of thermally cycled assemblies to determine quality assurance indicators and to establish if x-rays can detect damage due to thermal cycling.
- Optical microscopy characterization of assemblies with visible solder joints, including thin small outline packages (TSOPs), QFNs, and resistor at intervals was performed to document damage progress for various thermal cycling conditions.
- SEM microscopy evaluation of thermally cycled assemblies at higher magnifications with a better resolution than optical microscopy was performed. SEM was generally performed only prior to a test sample cross-sectioning.
- Destructive cross-sectional photomicrographs of thermally cycled area array packages, including hidden solder joints under the package to determine damage progress due to three different thermal cycle conditions and to determine failure locations.

2. Executive Summary

This report presents solder joint reliability test results for high-input/output (I/O) and low-pitch plastic ball grid array (PBGA) packages as well as other active/passive parts assembled onto printed wiring/circuit boards (PWB/PCB). It also includes reliability tests performed in collaboration with a university and an engineering manufacturing services (EMS) company. Figure 1 shows representative area array packages evaluated, including a high-I/O PBGA (1156 I/Os) with 1-mm pitch and a low-pitch chip scale package (CSP) (192 I/Os) with 0.4-mm pitch.

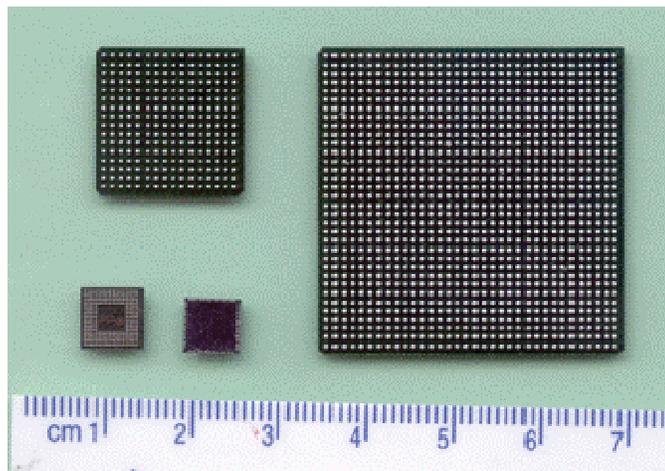


Figure 1. Area array plastic packages from high 1156 I/Os with 1-mm pitch to low 192 I/Os with 0.4-mm pitch.

BGAs with 1.27-mm pitch (distance between adjacent ball centers) or lower are the only choice for packages with higher than 300 I/O counts, replacing leaded packages such as the quad flat pack (QFP). These types of packages are also used for lower lead counts. In addition to size reduction, the area array packages also provide improved electrical and thermal performance, more effective manufacturing (improved manufacturability), and ease-of-handling compared to the conventional surface mount (SMT) fine-pitch leaded parts.

CSPs (a.k.a fine-pitch BGAs, FPBGAs) are further miniaturized versions of BGAs, leaded, and leadless packages with pitches less than 1.27 mm. These electronic packages have low mass and small chip sizes, and are generally used for low I/Os (<100) for memory and have the potential for use in higher (>300) I/Os. They also provide improved electrical and thermal performance, more effective manufacturing, and ease-of-handling compared to the conventional surface mount leaded parts such as thin small outline packages (TSOPs). Quad flat no-lead (QFN) and wafer-level packages are other packages designed for better heat dissipation and size reduction. However, compared to conventional packages, BGAs/CSPs have some key issues (mainly inspection, individual ball reworkability, and in some cases reliability) with the implementation of the new area array packages for high reliability applications.

Solder joint reliability of wire-bond PBGA and other packages were evaluated in this investigation. It was shown that this category of PBGA with 256 and 1156 I/Os, fully populated balls, and 1-mm pitch have acceptable thermal cycle reliability when using conventional tin-lead eutectic solder paste for their assembly. Thermal cycle reliability of other package assemblies, including flip chip die, ultra chip scale package (UCSP) with 0.4-mm pitch, two sizes of microlead frame (MLF), and two sizes of small outline packages (TSOP) varied. Process difficulty in assembling a flip chip and UCSP side-by-side using a conventional stencil print approach also played a role in poor reliability results for fine-pitch packages. Passive chips with various sizes from 0603, 0402, and 0201 showed acceptable solder joint reliability. However, difficulty was encountered in assembling 0201 resistors with no workmanship defects.

The key drawbacks of PBGA and fine-pitch array packages remain the same, i.e., inspection capability for interconnection integrity (cracks) and individual solder ball reworkability. In addition, most array packages are commercial-off-the-shelf (COTS) packages and are required to be subjected to additional stringent screening with added cost at the package level prior to their acceptance for high reliability applications. The issues with PBGA COTS packages are essentially the same as other COTS issues, including package die source and materials variations from lot-to-lot, availability of packages with radiation hard die, and outgassing for materials, and so on. Acceptability of ball integrity attachment before and after burn-in and coplanarity is also an issue to be considered. Assembly/inspection-related issues are additional key aspects of such implementation. Other issues include challenges of manufacturing of fine-pitch array packages and extremely small passives.

In this report, thermal cycle reliability of test vehicles (TVs) with daisy chain configuration under three thermal profiles is discussed in detail, including the nature and extent of damage and level by optical, x-ray, and cross-sectional photomicrographs. The report also provides a summary of test results performed in collaboration with industry and a university. Key findings based on a survey and test results are presented in the conclusion section. Key requirements for implementation of National Aeronautics and Space Administration (NASA) electronics systems are discussed in the NASA application section.

3. Background Information

3.1 Introduction

Ball grid arrays (BGAs) and chip scale packages (CSPs) are now widely used for many electronic applications, including portable and telecommunication products [1]. BGAs with 1.27-mm pitch are implemented for high reliability applications, generally demanding more stringent thermal and mechanical cycling requirements. The plastic BGAs introduced in the late 1980s and implemented with great caution in the early 1990s, further evolved in the mid 1990s to the CSP (also known as fine-pitch BGA) having a much finer pitch from 0.4 mm down to 0.3 mm. Because of these developments, it has become even more difficult to distinguish different area array packages by size and pitch.

Extensive work has been carried out by a National Aeronautics Space Administration (NASA)-led consortium in understanding technology implementation of area array packages for high reliability applications. The work included process optimization, assembly reliability characterization, and the use of inspection tools, including x-ray and optical microscopy, for quality control and damage detection due to environmental exposures. Lessons learned by the Jet Propulsion Laboratory (JPL)-led team and others have been previously published [2–11].

BGA packages with large 1.27-mm pitch have been the package of choice for commercial applications for many years. The BGA inputs/outputs (I/Os)/itches have continuously increased/decreased and now high-I/O packages with 1-mm pitch or lower are common. Area arrays come in many different package styles, including the plastic ball grid array (PBGA) with ball composition of eutectic $\text{Sn}_{63}\text{Pb}_{37}$ alloy or slight variations such as $\text{Sn}_{60}\text{Pb}_{40}$. The ceramic BGA package uses a higher melting ball ($\text{Pb}_{90}\text{Sn}_{10}$) with eutectic attachment to the die and board. The column grid array (CGA) or ceramic column grid array (CCGA) is similar to a BGA except that it uses column interconnects instead of balls. The lead-free CCGA uses a copper instead of high melting lead/tin column. The flip-chip BGA (FCBGA) is similar to the BGA, except that internally a flip chip die rather than a wire-bonded die is used.

Three array configurations are popular—a) full array, b) staggered array, and c) peripheral array. Plastic packages come in all styles, whereas ceramic packages are generally limited to a full array configuration. The plastic packages with 1-mm pitch generally come in full array ball population in order to accommodate the size reduction demand. Fully populated array packages present some significant routing challenges if a conventional PWB with plated-through-hole vias (PTHVs) is used for the design. Peripheral plastic packages have been developed to reduce solder joint failures at the die edge due to the significant coefficient-of-thermal-expansion (CTE) mismatch as well as to improve routing characteristics.

This report provides both a literature survey and comprehensive process/reliability test results for a test vehicle configuration performed at JPL as well as a summary of various test results performed in collaboration with university and industry partners. First, a summary is presented of key parameters that affect assembly reliability of PBGAs and fine-pitch CSPs based on a comprehensive literature search, including the effect of package I/O, die size and configuration, pitch, and double-side effects on reliability for tin-

lead solder balls and solder attachment. It then includes a brief discussion with some background information on microlead frame (MLF) process and assembly reliability presented in the literature.

In addition, numerous test vehicles (TVs) were built to determine issues associated with process and reliability of various high-I/O and low-pitch PBGA packages. Process variations for these types of packages as well as MLF and passives resistors were documented. Furthermore, results for thermal cycle reliability of TVs with daisy chain configuration under three profiles are presented and discussed in detail, including optical, x-ray, and x-sectional photomicrographs showing damage progress. A summary of test results performed in collaboration with industry and university is also included. Finally, key findings based on the literature survey, and test results are presented in the conclusion section. Also, key requirements for implementation of the new area array packaging technologies for NASA electronics systems are discussed in the NASA application section.

3.2 Area Array Packages

Area array packages, e.g., BGAs (see Figure 2) and CCGAs with 1.27-mm pitch (distance between adjacent ball centers) and finer pitch versions with 1-mm pitch, are the only choice for packages with higher than 300 I/O counts, replacing leaded packages such as the quad flat pack (QFP). Area array packages also provide improved electrical and thermal performance, more effective manufacturing, and ease-of-handling compared to conventional surface mount (SMT) leaded parts. Finer pitch area array packages (FPBGA), a.k.a CSPs, are further miniaturized versions of BGAs, or smaller configurations of leaded and leadless packages with pitches generally less than 1 mm.

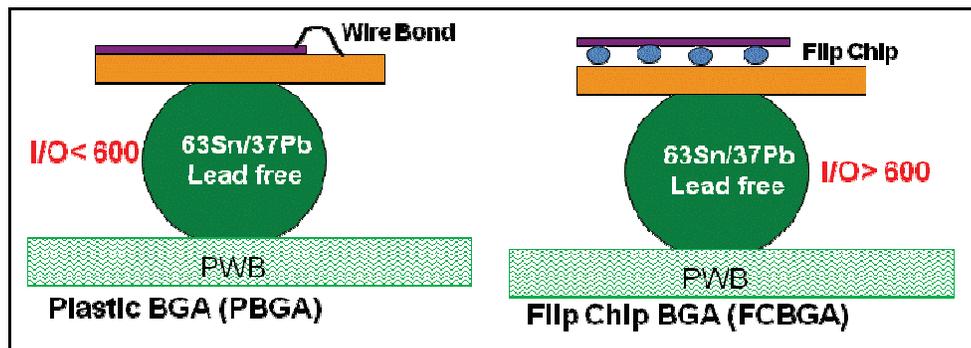


Figure 2. Typical plastic ball grid array with internal wire-bond and flip-chip die for low and high-I/O package configurations, respectively.

3.2.1 Advantages of Area Array Packages

Area array packages offer several distinct advantages over fine-pitch surface mount components having gull wing leads, including:

- High-I/O capability (100s to approximately 3000 balls can be built and manufactured, but gull-wing leads are limited to less than 300 I/Os.)

- Higher packaging densities (This is achievable since the limit imposed by package periphery for the gull wing leads is not applicable in the case of area array packages because area rather than periphery is used; hence, it is possible to mount more packages per the same board area.)
- Faster circuitry speed than gull wing surface mount components (SMCs) because the terminations are much shorter and therefore less inductive and resistive
- Better heat dissipation because of more connections with shorter paths
- Conventional SMT manufacturing and assembly technologies such as stencil printing and package mounting

Area array packages are also robust in processing. This stems from their higher pitch (typically, 0.8–1.27 mm), better lead rigidity, and self-alignment characteristics during reflow processing. This latter feature, self-alignment during reflow (attachment by heat), is very beneficial and opens the process window considerably.

3.2.2 Disadvantages of Area Arrays

Area array packages, however, are not compatible with multiple solder processing methods, and individual solder joints cannot be inspected and reworked using conventional methods. In ultra low volume SMT assembly applications, the ability to inspect the solder joints visually has been a standard inspection requirement and is a key factor for providing confidence in the solder joint reliability. Advanced inspection techniques, including x-ray, need development to provide such confidence for BGA and FPBGAs.

The four chief drawbacks of area array packages are:

- Lack of direct visual inspection capability
- Lack of individual solder joint re-workability
- Interconnect routing between the chip and the PWB requiring a multilayer PWB
- Reduced resistance to thermal cycling due to use of rigid balls/columns

3.3 Review of Chip Scale Package (CSP)

The trend in microelectronics has been toward ever increasing I/Os on packages, which is, in turn, driving the packaging configuration of semiconductors. Key advantages and disadvantages of CSPs compared to bare die are listed in Table 1. Chip scale packaging can combine the strengths of various packaging technologies, such as the size and performance advantage of bare die assembly and the reliability of encapsulated devices.

The advantages offered by chip scale packages include smaller size (reduced footprint and thickness), lesser weight, relatively easier assembly process, lower overall production costs, and improvement in electrical performance. CSPs are also tolerant of die size changes, since a reduced die size can still be accommodated by the interposer design without changing the CSP's footprint.

CSPs have already made a wide appearance in commercial industry as a result of these advantages, and now, even their three-dimensional (3D) packages are being widely implemented. Unlike conventional BGA technology at typically 0.8–1.27 mm pitch,

CSPs utilize lower pitches (e.g., currently, 0.8 to 0.3 mm) and hence, will have smaller sizes and their own challenges.

Table 1. Pros and cons of chip scale package (CSP).

Pros	Cons
<ul style="list-style-type: none"> • Near chip size • Widely used • Testability for known good die (KGD) • Ease of package handling • Robust assembly process <ul style="list-style-type: none"> • Only for area array version • Accommodates die shrinking or expanding • Standards • Infrastructure • Rework/package as whole 	<ul style="list-style-type: none"> • Moisture sensitivity • Thermal management <ul style="list-style-type: none"> • Limits package to low I/Os • Electrical performance • Routability <ul style="list-style-type: none"> • Microvia needed for high I/Os • Pitch limited to use standard PWB • Reliability is poor in most cases • Underfill required in most cases to improve reliability • Array package version <ul style="list-style-type: none"> • Inspectibility • Reworkability of individual balls

In an effort to systematically characterize the CSP as a package group, they may be classified into categories or types including: 1) the flex circuit interposer type; 2) the rigid substrate interposer type; 3) the custom lead frame type; and 4) the wafer-level package (WLP) type. A typical chip scale packaging process starts with the mounting of the die on the interposer using epoxy, usually of non-conductive type (although conductive epoxy is also used when the die backside needs to be connected to the circuit). The die is then wire bonded to the interposer using gold or aluminum wires. Wire bond profiles must be as low and as close to the die as possible in order to minimize package height. Plastic encapsulation to protect the die and wires then follows, usually by transfer molding. After encapsulation, solder balls are attached to the bottom side of the interposer, then the package is marked, and finally, the parts are singulated from the lead frame.

In summary, several different approaches are being employed by different companies to meet the packaging challenge of mounting high pin count integrated circuits(ICs) to substrates. Each of these approaches has its own merits and drawbacks.

- *Mount the IC internally, wire bond or flip-chip, on a flexible/rigid organic or ceramic substrates and package the chip into a suitable package material. Apply small solder bumps to the bottom of package, flip over, and mount onto suitable mounting pads on the PWB.* This is commonly referred to as ball grid array, or BGA, technology. If the package dimensions are nearly the same as those of the IC, this technology is called chip scale packaging, or CSP. The principal advantage of BGA and CSP are their ability to protect the IC (with package) and their close similarity to flip-chip.

- Attach the IC die to the bare PWB and wire bond from the die bonding pads directly to bonding pads of the PWB. This is commonly referred to as chip-on-board (COB) or chip-and-wire direct-chip attachment (DCA).
- Permanently attach small solder bumps to the bottom of the IC die, flip it over, and then mount it onto suitable mounting pads on the PWB. This is commonly referred to as direct flip-chip.

Figure 3 shows flip-chip die bond, chip-and-wire direct chip attachment, and chip scale package configurations.

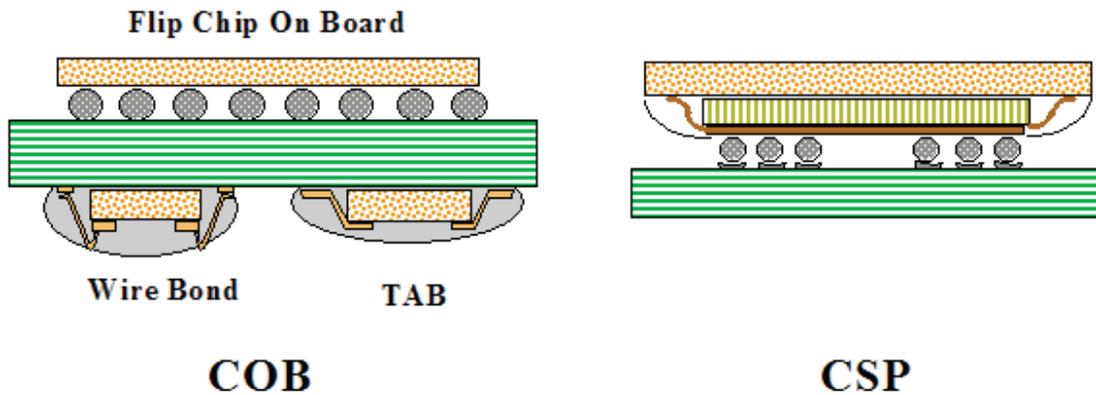


Figure 3. Chip-on-board/flip-chip die attachment and chip scale package configurations.

3.4 MLF Packages

Figure 4 shows a number of no-lead package configurations. The *MicroLeadFrame*® package (MLF®) evaluated in this investigation is a near CSP plastic encapsulated package with a copper lead frame substrate. It is a leadless package where electrical contact to the PWB is made by soldering the lands on the bottom surface of the package to the PWB, instead of the conventionally formed perimeter leads. The wide conductive bottom pad in this package technology enhances the thermal and electrical properties of the package.

The exposed die attach paddle on the bottom efficiently conducts heat to the PWB and provides a stable ground through down bonds and electrical connections through conductive die attach material. The design also allows enhancement of electrical performance by enabling the standard 2 GHz operating frequency to be increased up to 10 GHz with some design modifications.

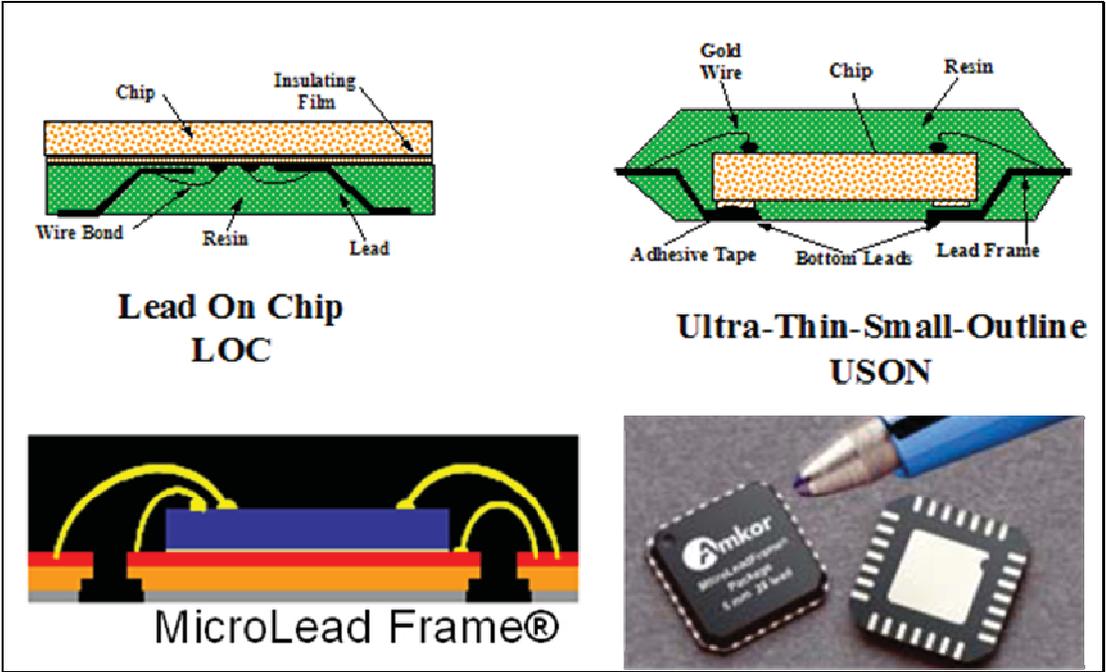


Figure 4. Examples of no-lead packages, including MLF® package photo and cross-sectional drawings.

4. PBGA Reliability

4.1 Background

Reliability of plastic and ceramic ball/column grid arrays has been assessed as part of the previous National Aeronautics and Space Administration Electronic Parts and Packaging (NEPP) activities. The most critical variables incorporated in the various investigations have been package types, ceramic column/ball and plastic; board materials, FR-4 and polyimide; surface finishes, OSP, HASL, and Ni/Au; solder volumes, low, standard, and high; and environmental conditions.

Plastic ball grid arrays (BGAs) with a variety of sizes and shapes are abundantly available, and are used widely by commercial industry for a variety of applications from benign office environments to high-end server applications. Military and avionic industries are also using them selectively after they have reached an acceptable level of maturity. Because of their wider applications, reliability of these packages is generally characterized by suppliers and verified by industry. Numerous excellent publications and references are available through IEEE CPMT, SMTA, IMAPS, and IPC proceedings and journals such as the Micro-electronic Reliability Journal.

This section categorizes the second-level assembly reliability for a number of plastic ball grid arrays (PBGAs) based on various parameters. Reliability data from researchers as well as suppliers will be tabulated for a number of packages from low to very high input/outputs (I/Os). This section also presents and compares reliability test results from a Jet Propulsion Laboratory (JPL)-led consortium to those from the literature for single and double-sided assemblies.

4.2 Plastic Package Assembly Reliability

Table 2 lists cycles-to-failure (CTFs) for a number of plastic packages with different configurations, selected from those reported in the literature [12–17]. Thermal cycle test results are for tin-lead balls with tin-lead solder, only even though most recent data generated by industry are for lead-free balls/solder. Lead-free packages/solders are yet to be fully adopted for high reliability applications. However, in order to update the literature survey and link behavior of the two solder alloys, data for the full array PBGA 676 I/Os are compared in reference 10 and briefly discussed under test results. The following section presents the effect of a few key parameters on solder joint reliability are presented.

Table 2 clearly shows the effect of thermal cycle range on CTFs; as ΔT increases, CTF generally decreases. Maximum and minimum temperature and dwell time at these temperatures contribute to failures. For example, the CT1%F (cycles-to-one percent-failure) for PBGA 256 I/O and 1.27-mm pitch in the range of 0° to 100°C was more than 9000 cycles (case #2); it was significantly reduced to approximately 2000 cycles when the temperature range increased to -40°/125°C (case #10)

Package size, thickness, configuration, internal die attach type, and I/Os also play a significant role in CTF. For example, in comparing case #2 to case #3, a significant decrease in CT1%F is shown when package I/O increased from the 256 I/Os, 1.27 mm, to 1849 I/Os (>9000 vs. 3095 cycles in the range of 0 to 100°C). Note that package configuration is also different for the higher I/O package; it has flip-chip die rather than wire-bond die attachment.

Die size and its relation to package size and ball configuration affect PBGA packages whereas, it has a lower effect on ceramic ball grid array / ceramic column grid array (CBGA/CCGA) CTF. This is not apparent from the cases presented in Table 2, but the die and package sizes are listed for the purpose of identifying such correlation. The comparison of case #7 and #8 indicates an increase in CTF when die size is increased. These results, contrary to general trends, may be due to the confounding effects of adding a heat sink for case #8.

Printed wiring board (PWB) thickness/stiffness also affects PBGA CTF. Preferred thickness was defined as 2.3 mm in IPC 9701⁽¹⁸⁾ since it is known that, generally, packages assembled on thinner PWBs show higher CTFs. Comparison for PBGAs with 1.27 mm in the range of 0°C to 100°C is difficult since most test data are generated using IPC PWB thickness values and also since most low I/O packages survived a large number of cycles. For example, PBGA 256 I/O showed no failures to 9000 cycles (case #2); one reason may be the use of thinner PWB for assembly.

Table 2. Cycles-to-failure data for tin-lead/tin-lead ball/paste illustrating the effect of a number of key variables.

Case No.	Package (I/O, pitch)	Pkg Size (die size, mm)	Thermal Cycle Condition (ramp, dwell, cycle/hr)	First Failure	Mean Life (N _{63.2%})	Comments
1	PBGA-119-1.27	27 × 27 ? (17.8 × 17.8 × 0.3)	0°C/100°C (10 min, 5 min, 2)	6260 (1% failure)	12215	27 Pkg Ref. Mawer [12]
2	PBGA-256-1.27	27 × 27 (10 × 10)	0°C/100°C (10 min, 5 min, 2)	No failure to 9000 cycles	No failure to 9000 cycles	PWB 1.6 mm Thk Ref. Amkor [13]
3	FCBGA-1849-1.27	??	0°C/100°C	3095 (1% failure)	4710	Ref. Shiah [16]
4	PBGA-256-1.0	17 × 17 (8.80 × 7.9)	0°C/100°C (10 min, 5 min, 2)	3687 (1% failure)	N/A	Full Array PWB, 2.3 mm Thk Ref. Altera [14]
5	PBGA-676-1.0	27 × 27 (17.8 × 17.8 × 0.3)	0°C/100°C (10 min, 5 min, 2)	4686	6012	30/30 Fail, PWB, PWB 2.36 mm Thk Ref. Xilinx [15]
6	PBGA-900-1.0	31 × 31.5 (17 × 17 × 0.3)	0°C/100°C (10 min, 5 min, 2)	4405	5344	28/28 fail PWB 2.36 mmThk. Ref. Xilinx [15]
7	FCBGA-1020-1.0	33 × 33 (22.6 × 19.9)	0°C/100°C (2 cycles/hr)	5670 (1% failure)	N/A	PWB Thk 2.3 mm 6 layer build up BT Ref. Altera [14]
8	FCBGA-1020-1.0	33 × 33 (17.9 × 16.7)	0°C/100°C (2 cycles/hr)	2770 (1% failure)	N/A	PWB Thk 2.3 mm 6 layer build up BT+ Cu heat sink Ref. Altera [14]

Case No.	Package (I/O, pitch)	Pkg Size (die size, mm)	Thermal Cycle Condition (ramp, dwell, cycle/hr)	First Failure	Mean Life ($N_{63.2\%}$)	Comments
9	PBGA-313-1.27	35 × 35 (13 × 13)	-30°C to 100°C (25 min, 15 min, 0.75)	3310 (1% failure)	4000	13 Pkg, PWB 1.6 mm Thk Ref. Evans / Ghaffarian [17]
10	PBGA-256-1.27	27 × 27 (10 × 10)	-40°C–125°C (15 min, 15 min, 1)	~2000 (1% failure)	3164	PWB 1.6 mm Thk Ref. Amkor [13]
11	PBGA-676-1.0	27 × 27 (17.8 × 17.8 × 0.3)	-40°C–125°C (15 min, 15 min, 1)	1341	1830	27/32 Fail, PWB 1.6 mm Thk Ref. Xilinx [15]

Double-sided, mirror image PBGA assemblies have significantly lower CTF compared to their single-sided version. Table 3 shows an example of the effect of double-sided mirror image on CTFs for a 175 I/O flip-chip package [5, 19, 20]. Recently, Chaparala, et al. [21] performed experimental and modeling analyses to verify results presented by Ghaffarian in his 1999 article published in Chip Scale Magazine. Ghaffarian reported that the mean time to failure for mirror-imaged CSP assemblies in thermal cycling is 40–60% less than that observed for single-sided CSP assemblies. He identified the factors differentiating double-sided assemblies from single-sided assemblies as an increase in assembly standoff due to a second reflow pass, an increase in assembly stiffness, and thermal disturbance due to the package on the other side of the PWB.

Table 3. Comparison of TV-2 FPBGA thermal cycle test results (–55°/125°C) to literature data for 0 to 100°C thermal cycle range.

TV ID	Board Thickness (NSMD pad size)	Via Location (diameter)	Thermal Cycle Range (total time)	Weibull Scale (no.)	Weibull Shape (m)	Acceleration Ratio
175 I/O FPBGA-enhanced Single-Side Condition 1 Condition 2	1.57 +/-0.2 (300 μm) (400 μm)	On pad (125 μm)	0°C to 100°C (32 min)	4331 3525	11.1 9.1	N/A
175 I/O FPBGA-standard Double-Side Condition 1 Condition 2	(300 μm) (400 μm)			1616 1163	17.6 10.5	N/A
TV-2 175 I/O FPBGA 9 data points 8 data points	1.27 (300 μm)	On pad (100 μm)	–55°C to 125°C (68 min)	1126 1134	6 11.9	3.8

5. Experimental Approaches

5.1 Package and Assembly Variables

The purpose of this aspect of the investigation was to characterize the reliability of high input/output (I/O) and low pitch of various package assemblies using tin-lead solder paste. Figure 5 shows photos of representative packages used in this investigation. A design of experiments (DOE) technique was used to cover various aspects of processing and packaging assembly reliability.

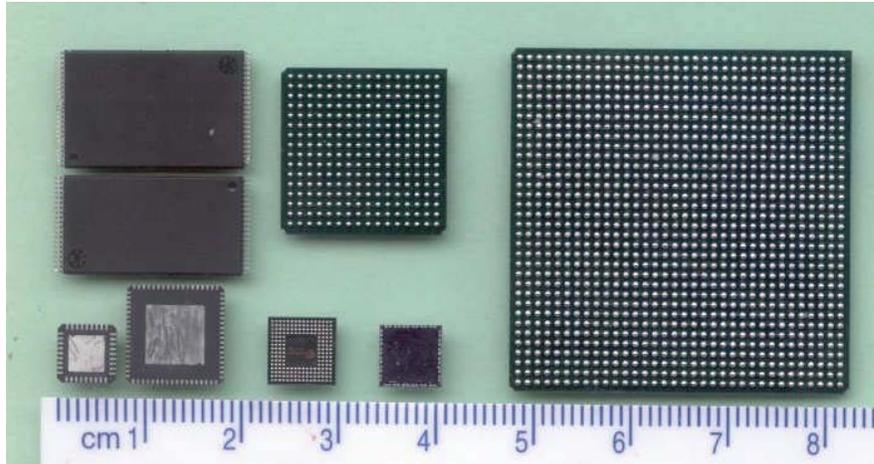


Figure 5. Photograph of PBGA, CSP, QFN, and TSOP packages included in the test vehicle for evaluation.

The following packages and parameters were evaluated as part of a larger DOE implementation:

- Two plastic ball grid arrays (PBGAs) were assembled with tin-lead solder balls both with 1-mm pitch and fully populated balls; one with 256 and the other with 1156 I/Os. Numerous daisy chains were designed on board to compliment daisy chains on a package in order to generate complete chains for solder joint failure monitoring.
- Two fine-pitch packages were included in the evaluation. A CSP package known as ultra chip scale packages (UCSP) had 192 I/Os with 0.4-mm pitch and 7-mm² body size. Also, flip chip die with 0.45-mm and 0.25-in² body size were directly assembled on board. No solder paste was used for either UCSP or flip-chip die attachment.
- PBGAs, UCSP, and flip-chip packages were not underfilled.
- Microlead frame (MLF) packages had 36 and 72 bottom leads with 0.5-mm pitch and body size of 0.6 and 1 mm², respectively. Tin-lead solder paste was used both on peripheral pads and central ground pads.
- A this small outline package (TSOP) package with two-sided leads on the width had 40 and 48 pins with 0.5-mm pitch and body size of 10 × 18.4, and 12 × 18.4 mm, respectively.

- Passive resistors with sizes of 0603, 0402, and 0201 were assembled on board using tin-lead solder paste.
- Boards were made from high Tg FR-4 materials with 0.062-inch thickness. They had an IAg (immersion silver) surface finish in order to also accommodate lead-free PBGA package assembly.
- A standard 6-mil-thick stencil was used for tin-lead solder paste print. Solder volume was measured at four corners and center for several assemblies to document actual paste print volume and solder paste release efficiency.
- Packages were assembled in a vapor phase reflow machine at a Jet Propulsion Laboratory (JPL) facility. Conventional reflow ovens were utilized by collaborators.

The assemblies were subjected to three thermal cycle profiles. Both the process and reliability results for various package assemblies, including PBGAs and CSPs, are discussed below.

5.2 Test Vehicles

Figure 6 shows a test vehicle assembly fully populated with high-I/O and low-pitch area array packages as well as TSOPs, quad flat no lead (QFNs), and passives including 0201. High Tg FR-4 boards with 0.093 inch thickness were used for the tin-lead assemblies. All packages had internal daisy chains where pairs of pads were connected by additional wire bonds. Compliment specific pairs of PWB pads were designed so that their connections within package daisy chain pairs completed a specific daisy chain pattern for solder joint failure monitoring. One or more daisy chains for each package were used for monitoring during thermal cycling and at intervals. Additional pads were added at each side of the package for manual probing and narrowing failures locations. Passive resistor components were also daisy chained by connecting them in a row and using the two ends of the chain for probing.



Figure 6. PWB design showing PBGA packages, CSPs, and other packages and resistors.

5.3 Solder Paste Volume

An RMA paste, Type III (-325+500) mesh, was used for paste deposition on the PWB pad's patterns using a paste print machine with standard parameters, including paste print speed. After deposition, each paste print was visually inspected for gross defects such as bridging or insufficient paste. For 1156 and 256 I/O PBGAs, on rare occasion, print quality was improved by adding a small amount of paste when insufficient paste was detected and by removing a small amount of solder paste between the pads to leave it open when bridging was discovered. For UCSP packages, the paste print volumes were inconsistent; therefore, only flux was used after a few unsuccessful trial test vehicle builds with paste. The paste print quality for the extremely small 0201 resistors was also inconsistent; only a limited number were corrected in order to achieve daisy chain connectivity for daisy chain monitoring in subsequent thermal cycling.

Solder paste areas and heights were measured using a laser profilometer with a three-dimensional (3D) measurement capability. Measurements were made at numerous locations—including corner and peripheral center pads—to gather solder volume data and their corresponding distributions.

An example of photomicrographs of PBGA 1156 pads after paste deposition with solder paste and solder paste characteristics parameters, including heights and areas, is shown in Figure 7. Figure 8 shows color-coded height distribution of solder paste print for this set of pads and another test vehicle. A similar distribution was achieved for solder deposition of PBGA 256 I/Os with 1-mm pitch. Overall, no major manufacturing issues were encountered with the paste depositions for PBGAs with 1-mm pitch.

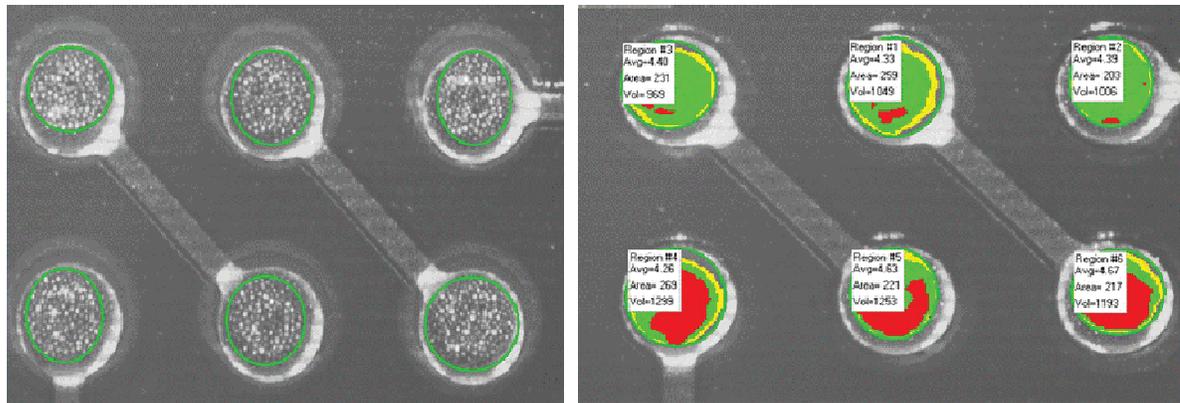


Figure 7. Solder paste print quality and estimated volumes for PBGA 1156 I/Os using a laser profilometer.

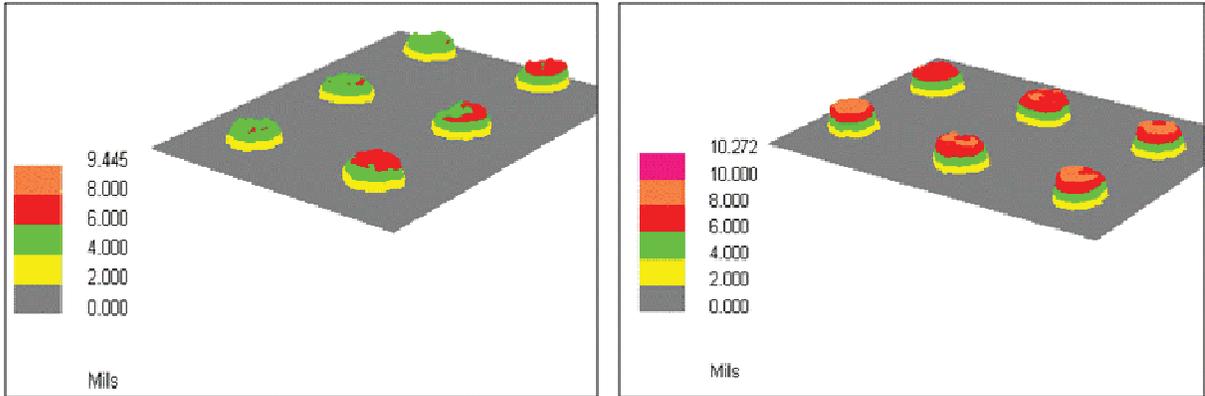


Figure 8. Examples of plots of color-coded solder height distribution for PBGA 1156 I/Os.

Figure 9 shows an example of photomicrographs of solder paste print and color-coded height for UCSP 192 I/O with fine pitch. The variation shown for solder paste print quality is unacceptable. Use of solder paste for this package was abandoned after a few trial paste depositions and only solder flux was used for assembly. Representative plots of solder paste distribution and color-coded heights for other packages/passives are shown in Figure 11. Quality of paste print was generally acceptable for leaded and leadless packages. The stencil design for MLF 72 I/Os was corrected to achieve higher solder volume after first paste prints. The pad design was smaller than those generally required and the stencil was designed based on PWB pads with such characteristics.

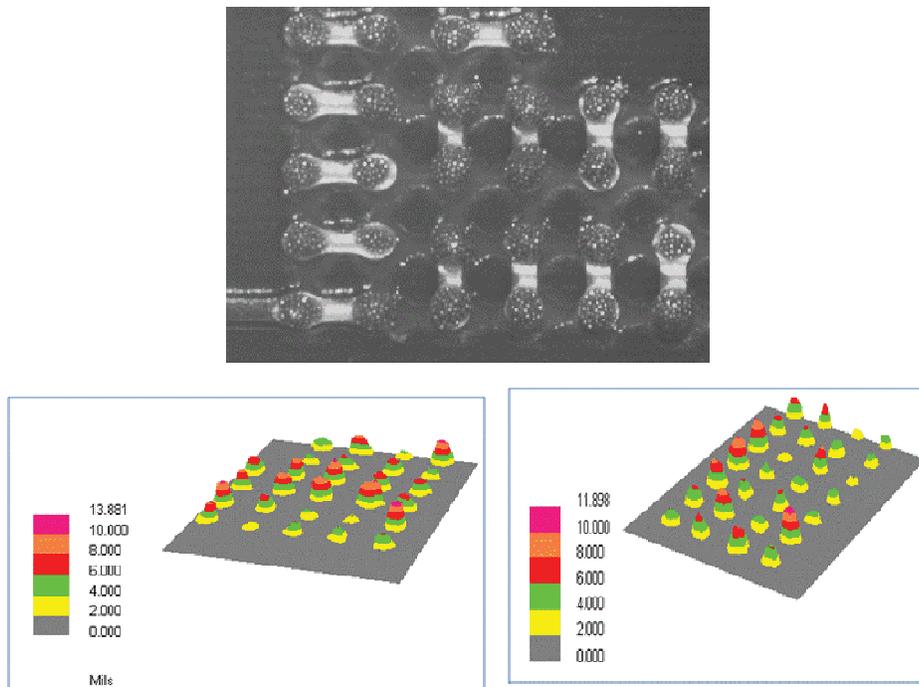


Figure 9. Examples of plots of solder paste print quality and volumes for UCSP 192 I/Os using a laser profilometer.

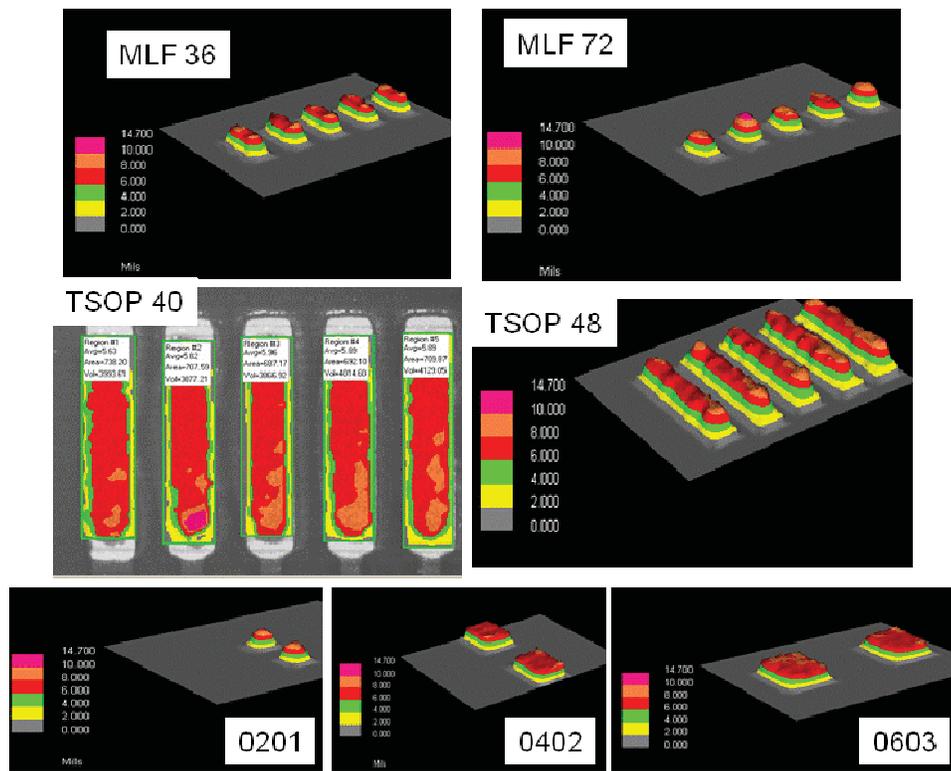


Figure 10. Examples of plots of solder paste print quality, estimated solder volumes, and color coded height for leaded and leadless packages using a laser profilometer.

5.4 Attachment Procedures

To assemble various packages, including plastic area array packages, paste deposition was carried out using a stencil with 6-mil thickness and appropriate aperture opening size to achieve estimated levels of solder paste volumes. Package placement was accomplished, including PBGAs, using an automatic placement machine. Solder paste reflow was performed using a vapor phase reflow machine. Reflow profiles were based on a previous profile that was tailored using a sample run with the attached thermocouple generating the reflow thermal profile. Vapor phase consists of an infrared preheating followed by a constant temperature boiling vapor zone. Infrared preheating temperature time and time in vapor phase are the only key parameters that can be modified to achieve better solder attachment quality.

5.5 Thermal Cycle Test Profiles

Three different thermal cycles were used with the following thermal profiles:

1. Cycle A: Ranged from -55° to 100°C with a 2° to $5^{\circ}\text{C}/\text{min}$ heating/cooling rate. Dwells at extreme temperatures were 15 minutes.
2. Cycle B: Ranged from -55° to 125°C with a 2° to $5^{\circ}\text{C}/\text{min}$ heating/cooling rate. Dwells at extreme temperatures were at least 10 minutes with duration of 159 minutes for each cycle.

3. Cycle C: Ranged from -120° to 85°C with approximately $5^{\circ}\text{C}/\text{min}$ heating/cooling rate and 10-minute dwells.

The criteria for an open solder joint specified in IPC-9701A were used as guidelines to interpret electrical interruptions. Generally, once the first interruption was observed, many additional interruptions within 10% of the cycle life also occurred. This was especially true for the ceramic packages. Opens were manually verified after removal from the chamber at the earliest convenient time.

5.6 X-ray

Real time x-ray systems are categorized as 2D and 3D x-ray systems. The 2D system is a standard x-ray inspection system with a microfocus source and a stationary image intensifier as the detector, capable of producing offset pseudo 3D features. The 2D system utilized has stationary microfocus source intensity, but the detector had off-axis rotational capability. The transmission x-ray captures everything between the x-ray source and image intensifier since x-rays are emitted from the source and travel through the sample. The higher the density of the sample (e.g., solder balls in PBGAs), the fewer x-rays will pass through and be captured by the image intensifier. The detected x-rays are displayed in a grayscale image, with the lower density (such as voids) areas appearing brighter than the higher density areas. The voltage and current of the x-ray's intensity can be adjusted to reveal features of most sections of the sample.

The 2D x-ray systems are very effective in testing single-sided assemblies. With the use of a sample manipulator, an oblique view angle enhances inspection of both single and double-sided assemblies with some loss of magnification due to increase in distance between source and detector. Experience is needed in discerning between bottom-side board elements and actual solder and component defects. This can be very difficult or even impossible on extremely dense assemblies. In any case, only certain solder-related defects such as voids, misalignments, and solder shorts are easily identified by transmission systems. However, even an experienced operator can miss other anomalies such as insufficient solder, apparent open connections, and cold solder joints.

The x-ray system with a rotational detector allows oblique generation of x-ray images with a higher magnification and a better intensity resolution since the focal spot remains the same and there is, therefore, no loss of magnification. An isocentric manipulator keeps the field of view unchanged when the oblique view mode is used. This feature allows better characterization of some defect features, including wettability and void location in area array packages.

6. Test Results

6.1 Inspection after TV build

For high reliability electronic applications, visual inspection is traditionally performed by quality assurance (QA) personnel at various levels of the packaging and assembly, known as mandatory inspection points (MIPs). Solder joints are inspected and accepted or rejected based on specific sets of criteria. Further assurance is gained by subsequent short-time environmental exposure, by thermal cycling, vibration, and mechanical shock, and so forth. These screening tests also allow detection of anomalies due to workmanship defects or design flaws at the system level. For space applications, generally 100% visual inspection is performed for the hybrid package presealing (precap) and after assembly prior to shipment.

Visual inspection is of limited use for plastic ball grid arrays (PBGA) packages since it is difficult to inspect peripheral balls and impossible to inspect hidden balls under the package. X-ray evaluation is needed for area array packages. Visual inspection was performed for thin small outline packages (TSOPs), microlead frames (MLFs), and passive resistors. Every daisy chain's resistance was measured and documented. Figure 11 depicts representative photomicrographs showing quality of solder joints and workmanship defects for packages with visible solder joints. The 0201 resistor showed the most workmanship defects, including missing resistors and tomb stone. The 0402 showed tomb stone also, but no tomb stone was detected for the 0603 assemblies. MLF 36 showed acceptable solder joint quality with bulbous solder joints because of high solder volume deposition due to the pad design. This was not the case for the MLF 72 input/outputs (I/Os) since the pads had relatively small sizes compared to the package dimension and castellation. Copper exposures were apparent for many MLF 72 I/O packages near the top of the package pad. Solder joints were generally acceptable for the TSOPs with the exception of the lead toe's face showing no solder wetting.

For PBGAs with 1156 I/Os and 1-mm pitch, the accessible peripheral balls were inspected with no apparent evidence of opens. Figure 12 documents representative photomicrographs taken after assembly. Quality of solder joints were acceptable, which was also verified by daisy chain continuity. All PBGA assemblies showed acceptable daisy chain continuity resistances; therefore, it is assumed that they had acceptable quality with no solder joint opens. To reduce cost, quality is verified after thermal cycling by cross-sectioning.

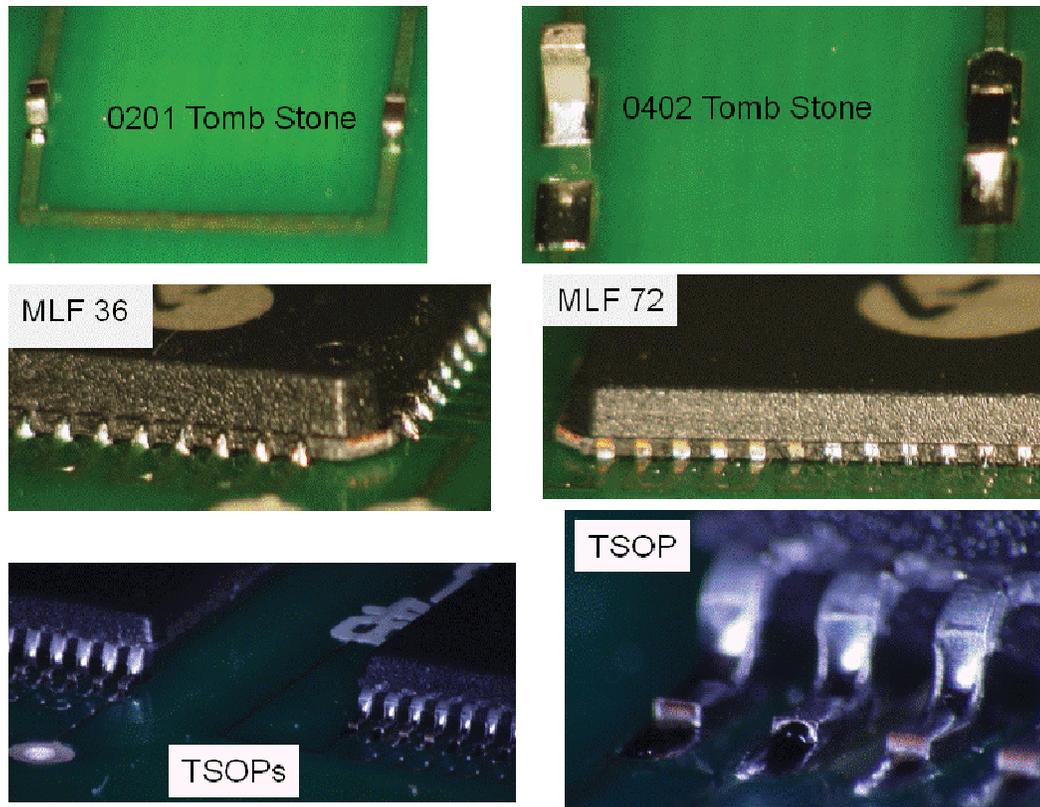


Figure 11. Representative photomicrographs of solder joints for packages with visible solder joints, showing solder joint quality and defects, including tomb stone and exposed pads/leads.

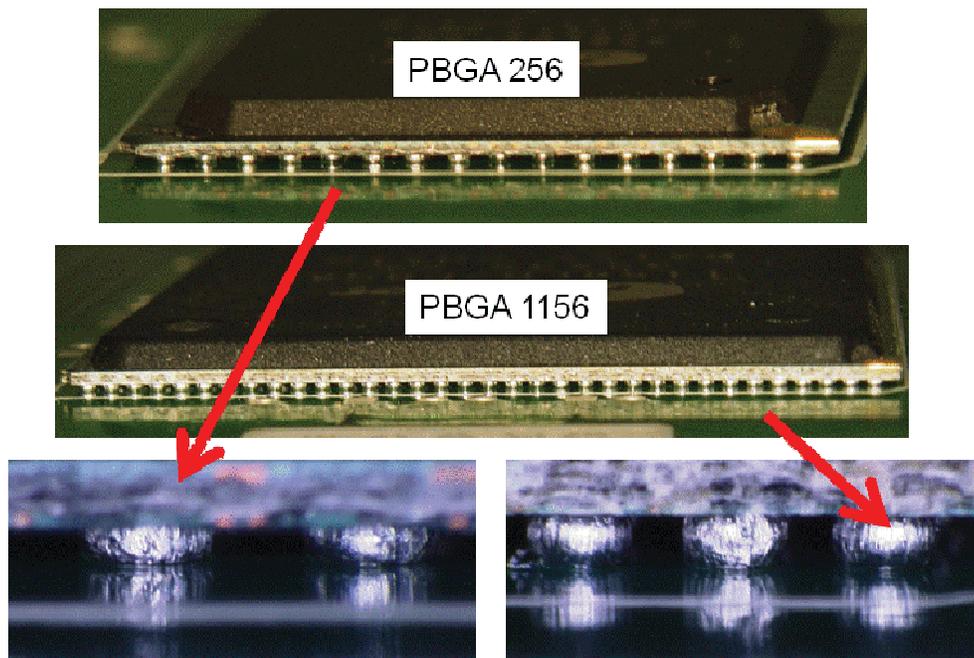


Figure 12. Representative solder joints for PBGA 1156 and 256 I/Os with 1-mm pitch.

Figure 13 shows optical photomicrographs for UCSP 192 and flip-chip die assembly. It is extremely difficult, if not impossible, to determine the integrity of solder joint quality. Only process control and possibly 3D x-ray may be able to shed light on the integrity of the joints. Assemblies showed daisy chain continuity in most cases. As stated, use of solder paste for UCSP causes shorts among the adjacent pads.

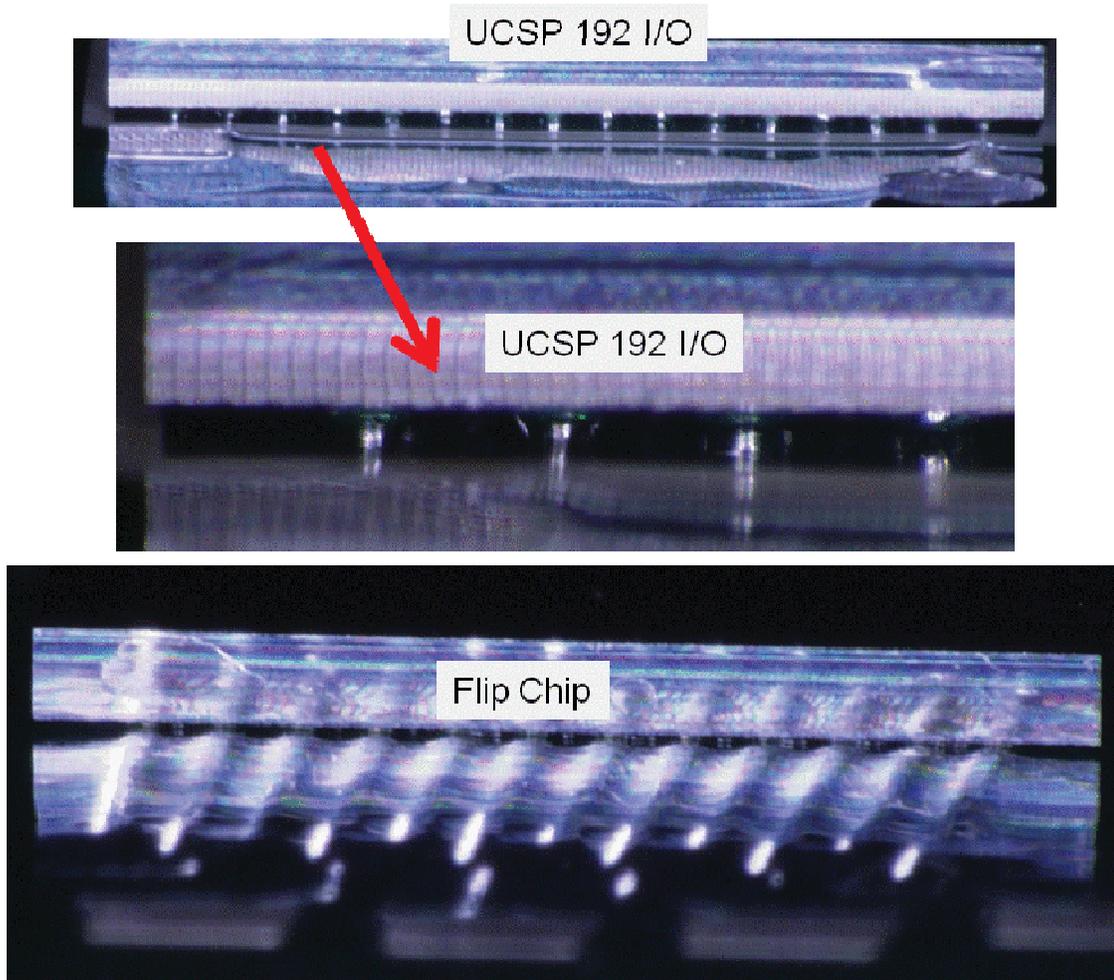


Figure 13. Representative photomicrographs of UCSP and flip-chip die solder joint assemblies.

6.2 Optical Microscopy during Cycling

Three representative boards from three cycle conditions were selected for a more detailed characterization, including x-ray, optical microscopy, SEM, and cross-sectioning. Optical microscopy evaluation rarely reveals PBGA and chip scale package (CSP) failures during thermal cycling. Failure of TSOPs and resistors, however, can be verified by optical microscopy. Detection of MLF failure is more challenging. Figure 14 shows photomicrographs of representative TSOP 40 I/Os where failure occurred during thermal cycling (-55° to 125°C). Failure of the corner lead on one side of the package and heavy stresses on

the lead heels are apparent. A similar crack initiation at the heel was observed for the quad flat package having similar configuration, but different sizes. Figure 14 also includes two resistors with workmanship defects—double-deck resistors with a hidden tiny 0201 resistor under an 0603 resistor showing signs of solder joint stress, but no signs of microcracking.

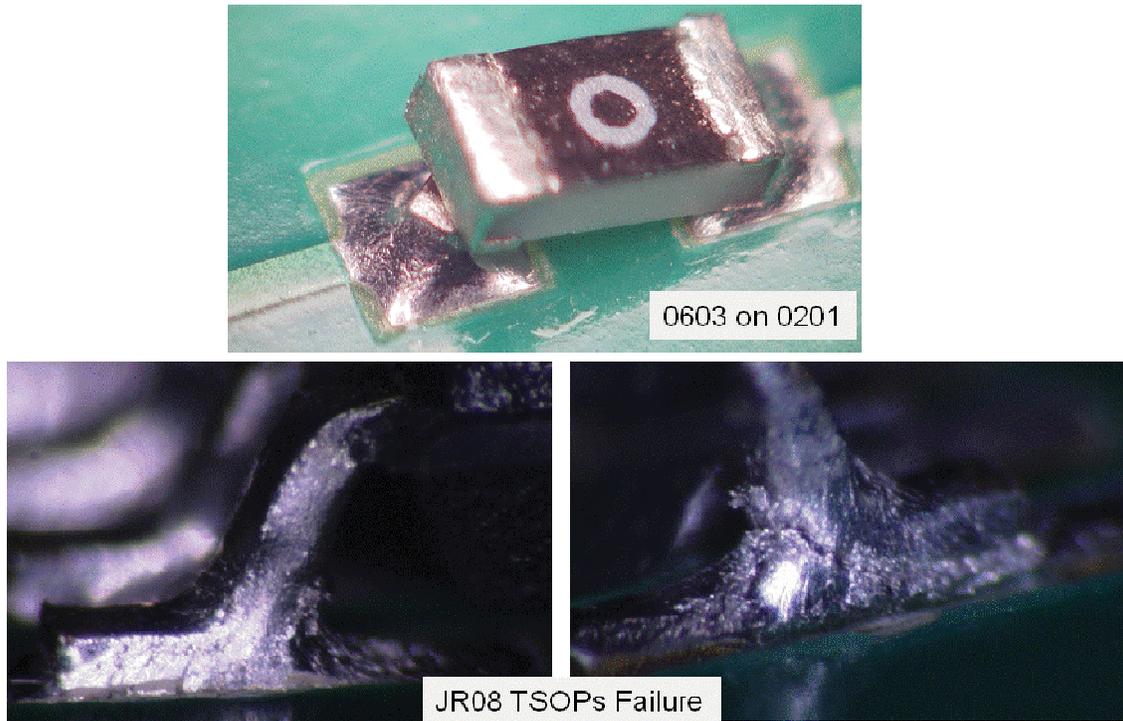


Figure 14. Photomicrographs showing failure of TSOPs at the corner leads (bottom photos) after thermal cycling and only signs of stress for a hidden 0201 resistor under an 0603 resistor (top photo).

Representative optical microphotographs after thermal cycling for package assemblies with visible solder joints were documented. Assemblies were subjected to Cycle A, B, and C conditions with relatively the same time length, but various numbers of thermal cycles. Figure 15 shows 0201, 0402, and 0603 resistor assemblies subject to Cycle A (-55° to 100°C) and Cycle B (-55° to 125°C) conditions. The 0201 and 0402 solder joints showed some minor signs of stress marks, which were more prominent for Cycle B conditions. For 0603, minor damage under Cycle A and more appreciable damage with microcracks were apparent under Cycle B. In both cases, parts remain intact with no signs of metallization degradation. In either case, there were no daisy chain continuity failures.

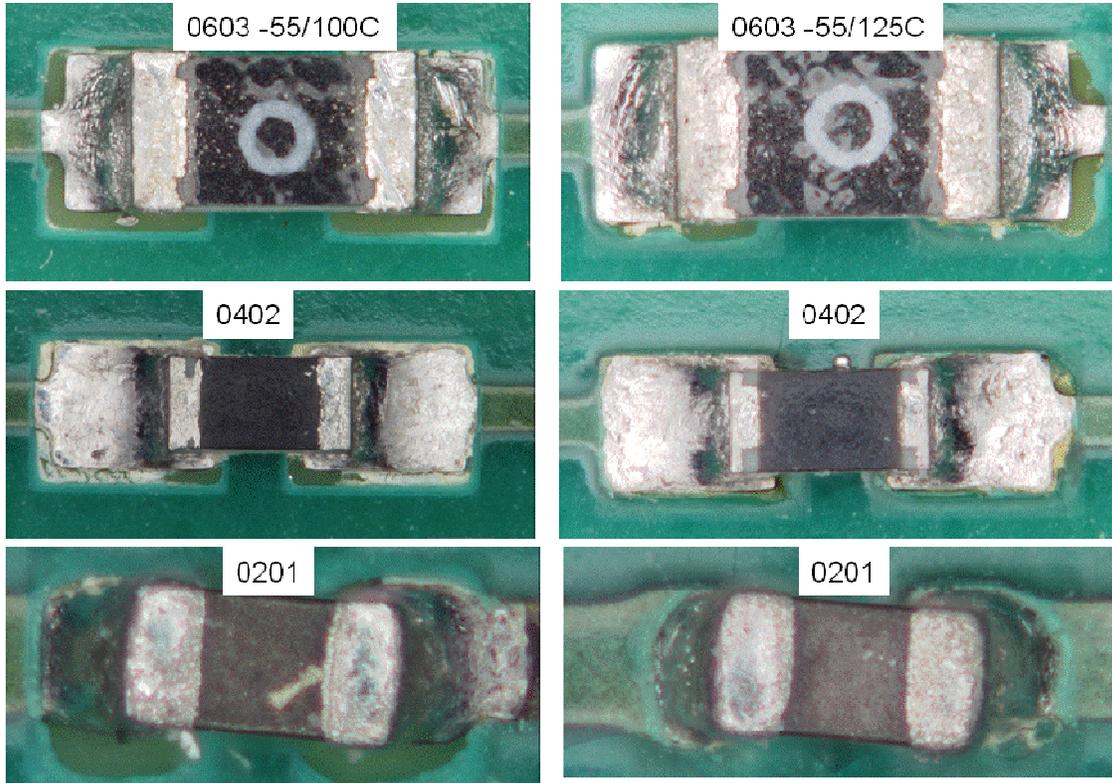


Figure 15. Photomicrographs of 0603, 0402, and 0201 resistors after being subjected to Cycle A (-55° to 100°C) and Cycle B (-55° to 125°C) conditions.

Figure 16 shows solder and part damage due to the Cycle C (-120° to 85°C) condition, which is an extreme cold environment not representative of conventional environmental conditions. It is, however, a realistic environment for space electronics applications. For this condition, in addition to solder damage and microcracks, in some cases, even resistor metallization showed signs of damage with partial or full peeling. Peeling was the worst for 0402 with some for 0603 and none for 0201 resistors. Further investigation is required to determine root cause of this failure; however, the weak resistor metallization and bonding exposure to cold temperature may have played a key role since this was not observed for milder cold temperature exposure. Thus, cold temperature excursion with cycling appears to have exacerbated the damage.

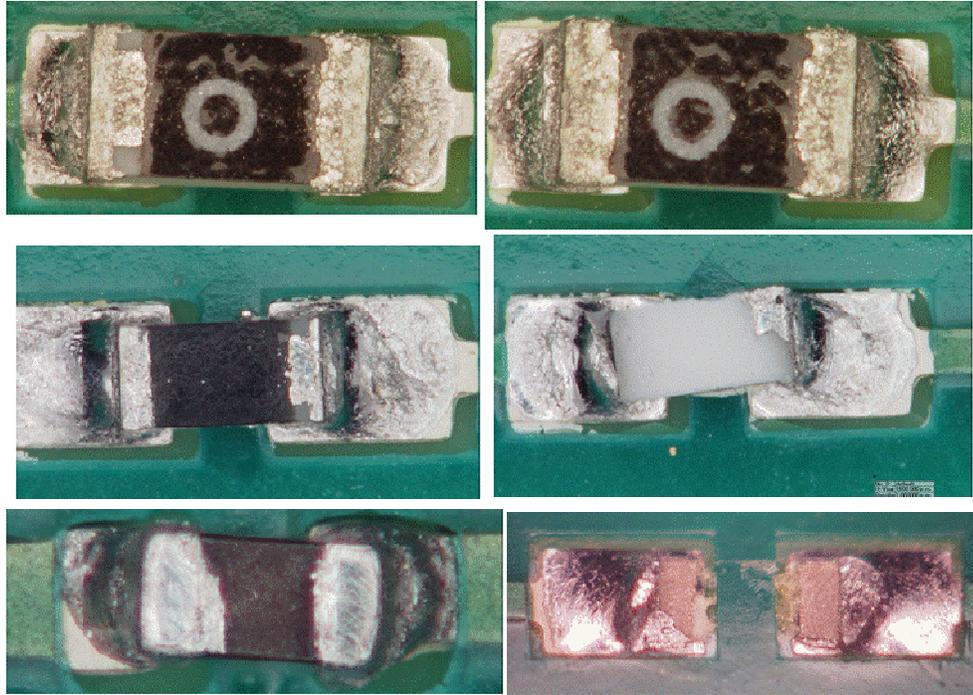


Figure 16. Photomicrographs of 0603, 0402, and 0201 resistors after being subjected to Cycle C (-120° to 85°C) condition and a failure of sheared resistor.

Figure 17 shows photomicrographs of solder joints for MLF 36 and 72 I/Os, subjected to Cycles A, B, and C conditions. No daisy chain failures were apparent for this level of cycles. Some microstructural changes, however, were apparent for the 72 I/O packages, whereas solder joints for the 36 I/O assemblies were relatively shiny with minimum solder joint degradation. Contrary to previous castellated leadless packages, it is difficult to determine crack initiation and propagation for this style of package assembly.

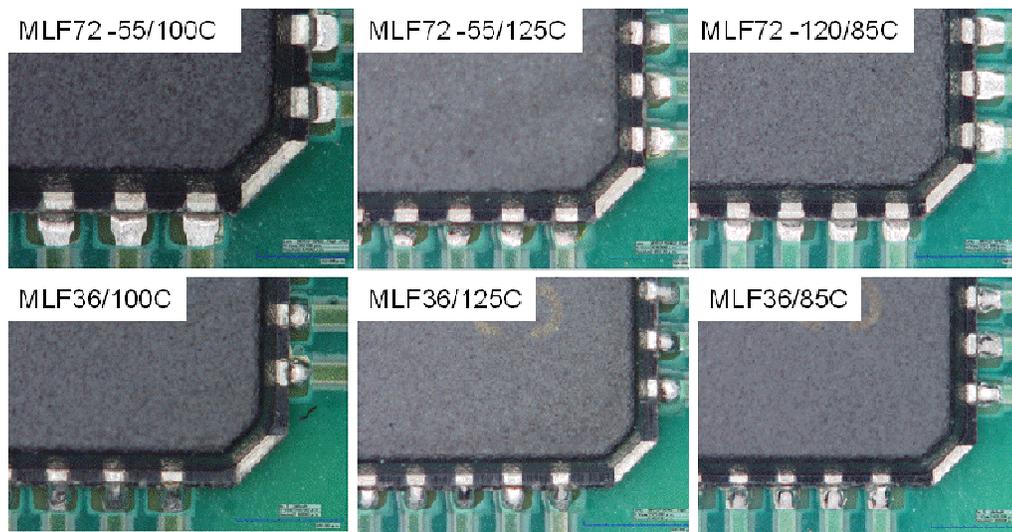


Figure 17. Photomicrographs of MLF 36 and 72 I/Os subjected to Cycles A (-55° to 100°C), B (-55° to 125°C), and C (-120° to 85°C) conditions.

Figure 18 compares solder joint damage of several leads, including corner leads for the TSOP 40 and 48 I/Os under Cycle A, B, and C conditions. Figure 19 provides photomicrographs of corner leads showing solder joint cracking and failures. The 40 I/O TSOP assemblies showed some signs of microcracks in solder joints at the lead heel under the Cycle A condition, whereas the solder failed at the heel under Cycles B and C conditions. Solder joints at the corner leads with the highest stress conditions are generally first to fail as apparent from Figure 19. TSOP 48 I/Os generally showed less signs of damage and cracking in comparison to its 40 I/O package version as evident from photomicrographs in the two figures. Damage is expected to be more severe for the TSOP 48 I/Os, which is a larger package than the 40 I/O package, if package size was the dominant factor in solder joint damage introduction. X-rays, on the other hand, shed some light on the further nature of such results.

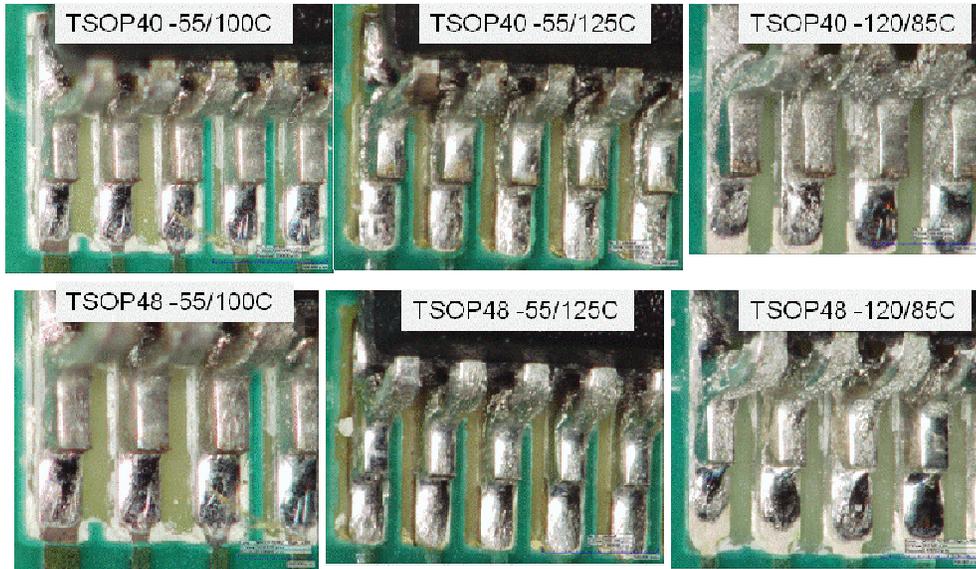


Figure 18. Photomicrographs of a number of TSOP 40 and 48 leads subjected to Cycles A (-55° to 100°C), B (-55° to 125°C), and C (-120° to 85°C) conditions.

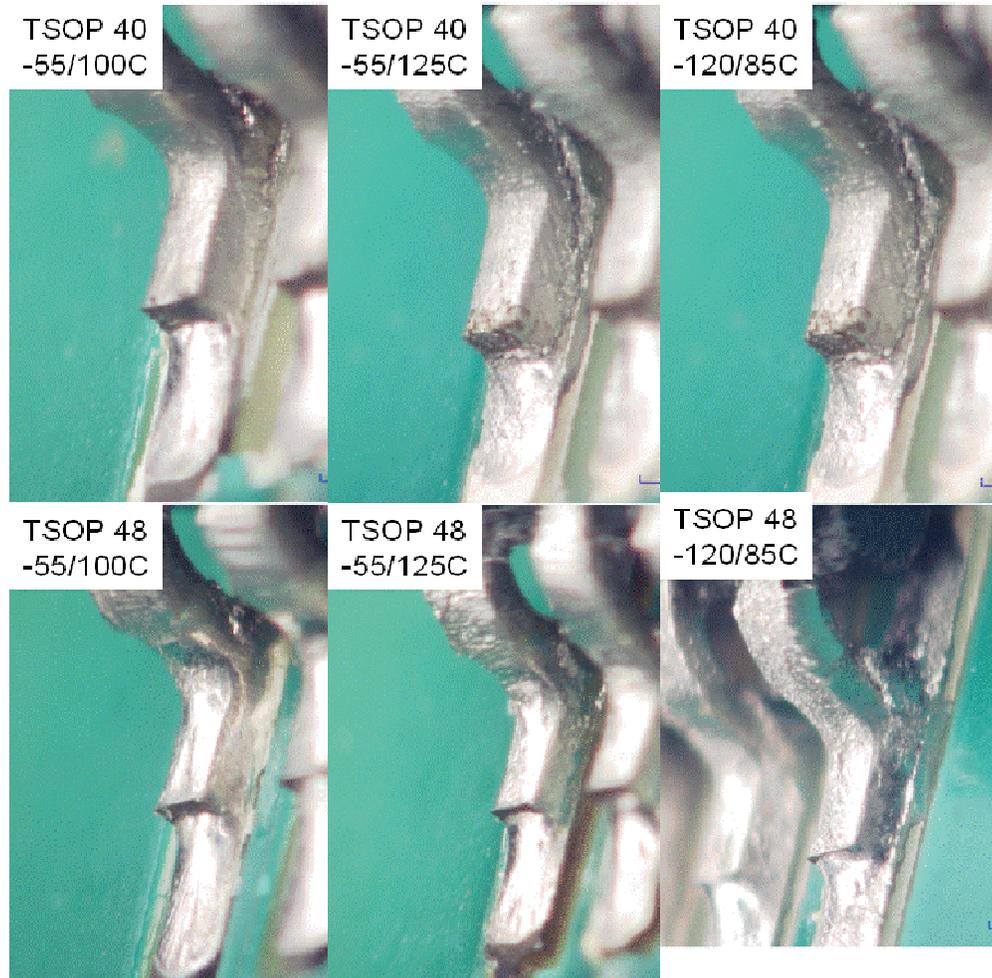


Figure 19. Photomicrographs of corner leads of TSOP 40 and 48 I/Os subjected to Cycles A (-55° to 100°C), B (-55° to 125°C), and C (-120° to 85°C) conditions.

6.3 X-ray Characterization

X-ray inspection was performed on a cycled test vehicle to determine various package/assembly conditions. The 2D microfocuss x-ray transmission system with rotational detector was utilized for this inspection. Even though optical microscopy was used to document exposed solder joints, x-ray is required to determine other package and solder joint characteristics such as void levels. Therefore, no attempt was made to determine damage condition of solder joint quality for assemblies, including 0201, 0402, and 0603 resistors; MLF32 and MLF72 packages; and TSOPs 40 and 48 I/Os. However, quality of voids, package configuration, and die were identified.

Figure 20 shows the condition of MLF package assemblies as revealed by x-ray. MLF solder joints showed some voids which are much lower than voids in the center conductor pads. Void levels for TSOPs are much lower. Note, different die configurations and sizes for the TSOP 40 and 48 I/Os. The die is much larger for the TSOP 40 leads. The passive resistors show no signs of voids possibly because of their tiny sizes, which makes detection difficult.

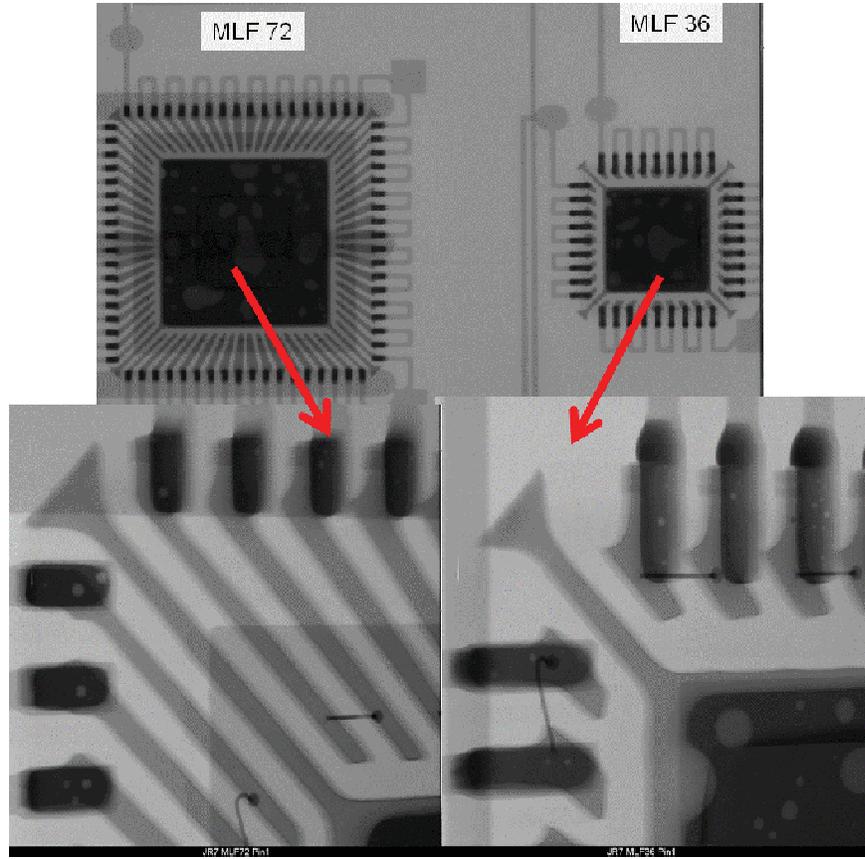


Figure 20. X-ray photomicrographs of MLF 36 and 72 I/Os.

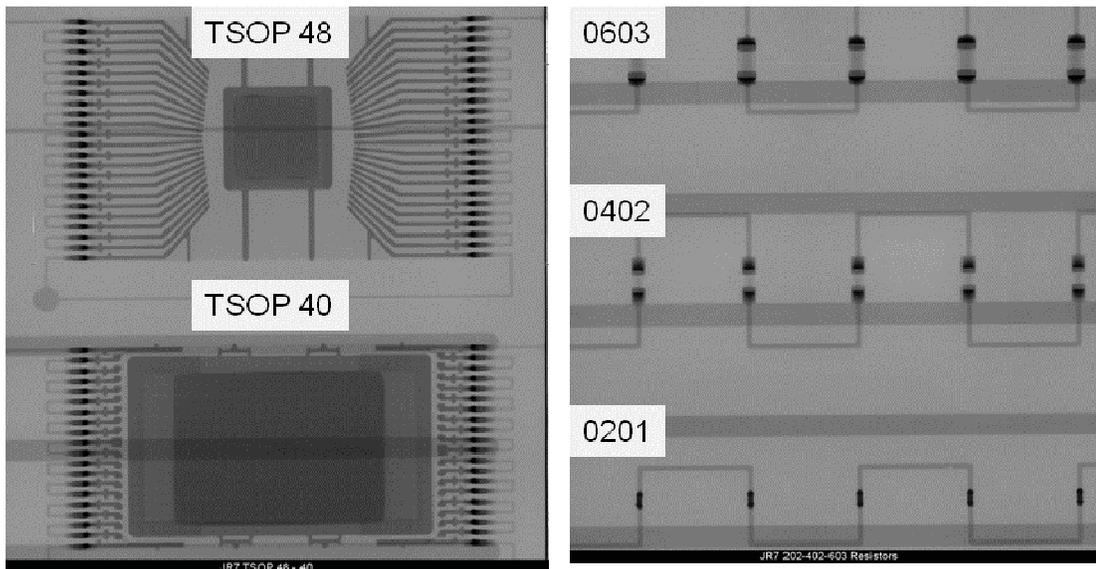


Figure 21. 2D X-ray photomicrographs of MLF TSOP 40 and 48 I/Os and 0603, 0402, and 0201 resistors.

Figure 22 shows x-ray photomicrographs for UCSP and flip-chip die attachment. UCSP 192 I/O initially showed numerous shorts in a trial build (solder paste rather than flux was used to assemble test vehicles [TVs]). No shorts were apparent for the flip-chip die assembly.

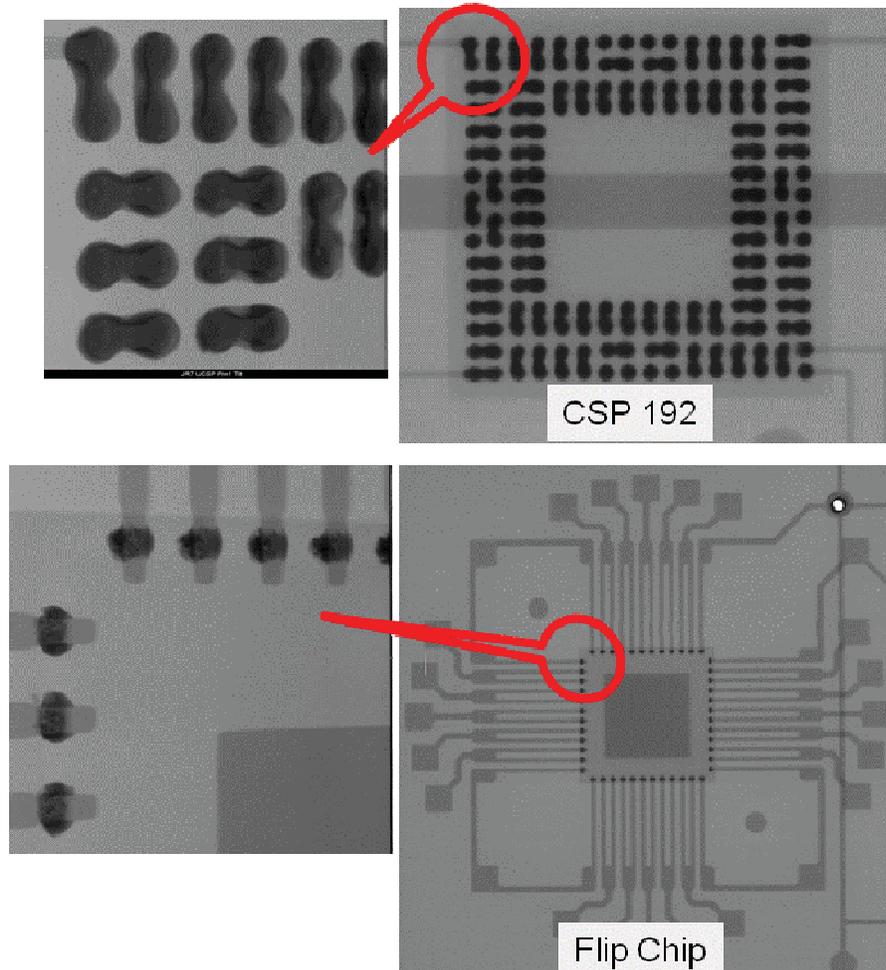


Figure 22. X-ray photomicrographs of UCSP and flip-chip die attachments.

PBGAs with 1156 and 256 I/Os showed minimum voids, but no shorts or other anomalies were apparent (see Figure 23). Real time x-ray inspection of all solder balls during evaluation revealed no signs of anomaly or damage. Generally, it is difficult to detect solder joint microcracks/damage by x-ray as previously discussed.

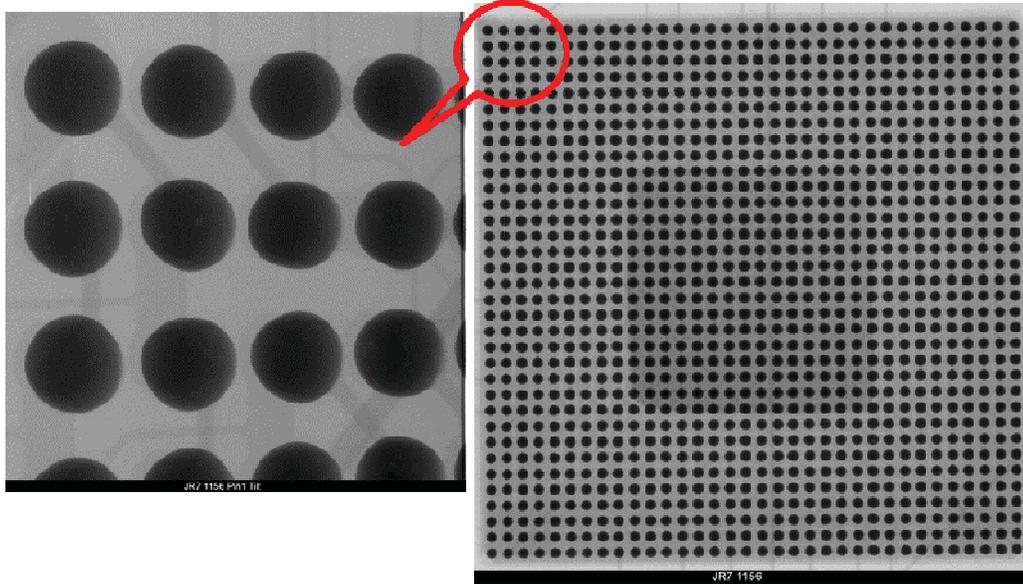


Figure 23. X-ray inspection of PBGA 1156 I/Os.

Even though x-ray revealed no significant damage, it clearly identified other parameters of packages that can help better analyze observed failure data. For example, it clearly shows that internal structures of the two TSOPs are different, which may provide the reason for observing earlier failures of TSOP 40 compared to TSOP 48 I/Os under various thermal cycling conditions.

6.4 SEM Microscopy Characterization

Solder joints for the TSOPs and other packages with visible solder joints were inspected by optical microscopy at intervals during thermal cycling to determine their state and progress of damage. The optical microscopy photomicrographs for these assemblies were documented and presented in the previous section. To perform scanning electron microscopy (SEM) evaluation, representative PBGA 1156 I/Os were cut from the TV, close to the package edge, in order to be able to mount on the SEM mounting fixture and rotate the sample for full characterization at higher magnifications. Figure 24 shows representative SEM photomicrographs for PBGA 1156 I/Os prior to cross-sectioning at various magnifications. Microcracks within the balls and fine microcracks at the package interfaces are apparent. Contrary to ceramic column grid arrays (CCGAs), the outer rows do not represent the most severe stress condition; therefore, these SEM photomicrographs may not be representative of internal damage especially for ball interconnections at the package die periphery.

6.5 X-sectional Verification

Figure 25 shows representative SEM photomicrographs of the PBGA 1156 I/Os sample after (see Figure 24 for prior to) x-sectioning diagonally through the center of the pack-

age in order to reveal the microstructure of internal interconnections. It specifically shows balls under the die that were expected to exhibit more severe stress conditions due to a larger thermal cycling coefficient-of-thermal-expansion (CTE) mismatch. Except for very fine microcracks at the package interfaces, no severe degradation was observed, either under the die or throughout the x-section. Minor separation apparent at the die attachment may be either due to die bond separation or edge effects due to mounting of the sample and subsequent polishing.

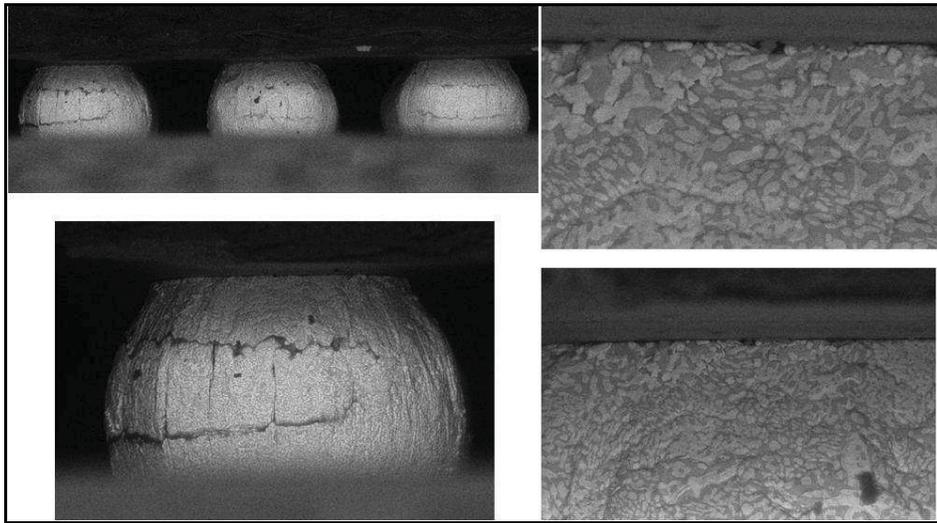


Figure 24. Representative SEM photomicrographs of a PBGA 1156 assembly after thermal cycling and prior to cross-sectioning.

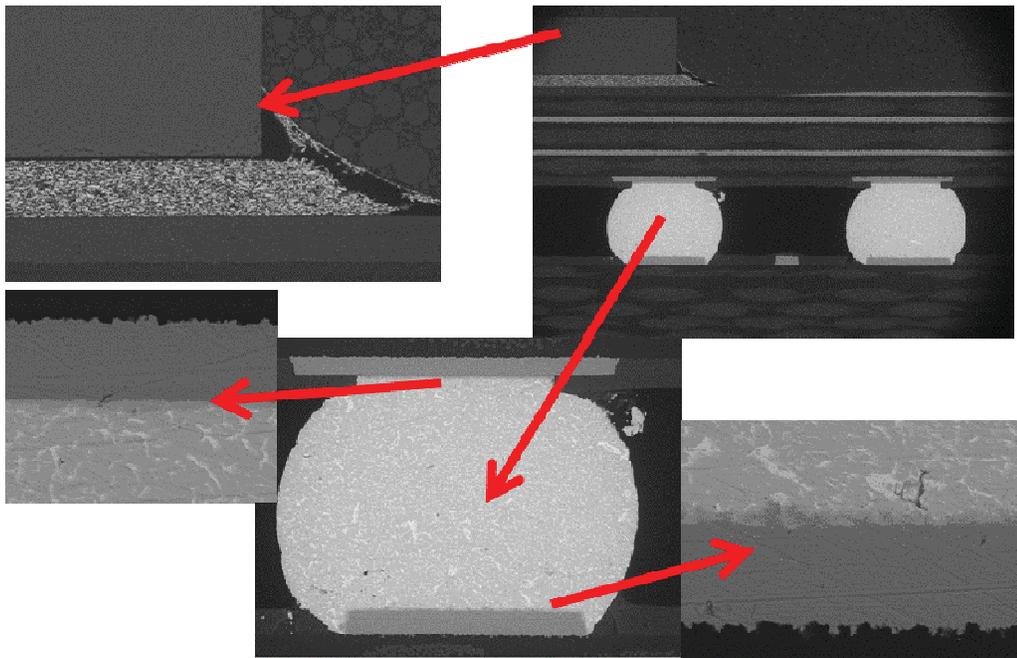


Figure 25. Cross-sectional SEM photomicrographs of PBGA 1156 I/Os assembly after thermal cycling.

6.6 Summary of Test Results by RIT University

A paper [11] was jointly published with the Rochester Institute of Technology (RIT) Center for Electronics Manufacturing and Assembly (CEMA), presenting aspects of process optimization and reliability evaluation. A large number of TVs using the same TV design and packages presented in this document were used to optimize the process not only for tin-lead, but also for a lead-free solder alloy. The investigation also included both forward and backward compatibility. In addition, assembly behaviors under isothermal aging and mechanical shock were also characterized.

A full factorial design was used in the investigation, with three factors—solder paste, component finish, and PWB surface finish. Eutectic Sn-Pb paste (63–37% wt) and SAC305 (Sn3.0%Ag0.5%Cu) solder pastes were used as Pb-containing and Pb-free levels respectively. For component finish metallization, Sn-Pb termination finish/bump composition was used for the Pb-containing level while Sn termination/SAC 405 bump composition represents the Pb-free level. Immersion silver (IAg) and electroless nickel immersion gold (ENIG) surface finish on PWB was used for testing and analysis.

The solder joints were subjected to isothermal aging followed by mechanical shock test, attempting to establish a relationship between the intermetallic growth at the solder/PWB interface and the mechanical integrity of the solder joint. The compounding of the tests, unlike singular test methods, provides a more realistic estimate of the reliability and life of the joints in the field. The assemblies were cross-sectioned after the tests and the microstructure of the solder joints were analyzed to study the intermetallic growth upon isothermal aging.

This research provided insight into the process development and manufacturing of mixed circuit-card assembly. Various stages in the development of the final product were studied. A general clear inference cannot be drawn from the test results under the specific test conditions as to which assembly combination is superior in performance, possibly because various package types and processes had compounding effects. The following are a few trends observed:

- Leadless device assemblies performed better than that of area array device assemblies under repeated shocks before and after isothermal aging.
- Area array assemblies with solder paste showed much higher mechanical shock resistance than those assembled with no solder paste.
- Assemblies that used IAg surface finish on PWB showed slower deterioration due to isothermal aging than the ENIG assemblies.

6.7 Summary of Test Results for PBGA 676 I/Os

A paper [10] was jointly published with Celestica, Inc. that provided a literature survey on fully populated PBGA 676 I/Os with 1.27-mm pitch built with tin-lead and lead-free solder alloys. The effects of various parameters, including type of solder alloys, reflow maximum temperature, dwell time, and monitoring techniques, are discussed in detail. Results of Jet Propulsion Laboratory (JPL) data performed under three different thermal cycles, including one cool down to -120°C , are also presented. Celestica Inc.'s most recent data generated for the same package/assembly (RIA3 TV) using a preferred thermal cycle profile recommended by IPC 9701 are also presented.

The literature thermal cycle reliability test results show that for the mild thermal cycle condition (0° to 100°C), the test results from Solectron, Xilinx, and Celestica Inc. are the same. For harsh thermal cycle conditions (-55° to 125°C), test results indicate that tin-lead solder may perform better than lead-free based on Xilinx and Celestica Inc. data, even though daisy chain monitoring techniques for failures were different. Celestica showed that electrical failures were earlier than when Dye and Pry failure characterization was performed. The status of thermal cycle test results performed at JPL using RIA3 test vehicles passed 200 thermal Cycles A (-55° to 100°C), B (-55° to 125°C), and C (-120° to 85°C) conditions.

7. Conclusions

The conclusions, based on the results of thermal cycling under three conditions using limited plastic ball grid array (PBGA) 1156 input/output (I/O) and other package assemblies, are as follows:

- The two-dimensional (2D) x-ray system used in this investigation did not reveal any solder damage for area array package assemblies due to thermal cycling. Visual inspection provided good indication of solder damage for leaded thin small outline packages (TSOPs) and resistors, but it was more difficult to detect microcracking for the microlead frame (MLF) solder joints. Visual inspection of outer row balls of high-I/O array package with 1-mm pitch was somewhat possible whereas for fine pitches it was almost impossible.
- Resistors with 0603, 0402, and 0201 sizes showed various solder joint degradations when subjected to Cycle A (-55° to 100°C), Cycle B (-55° to 125°C), and Cycle C (-120° to 85°C) conditions for about the same overall time duration, but different number of thermal cycles. Solder joint degradation increased from Cycles A to B and C.
- The key degradation difference between Cycle B and Cycle C was that the 0402 resistor package showed package metallization peel off in some cases. Further investigation is required to understand the root cause of such behavior.
- MLF 36 and 72 I/O showed no solder joint failures for the number of cycles under the three thermal cycle conditions. They showed, however, various levels of voids especially for under package conductor solder attachment.
- The TSOP with 40 leads generally showed higher signs of solder joint damage compared to TSOP 48, possibly due to differences in die size and package configuration as determined by x-ray.
- The TSOP with 40 leads showed some signs of microcracks at the corner leads under Cycle A condition, whereas complete cracks and failure were observed for the Cycle B and C conditions. Failures were generally at the corner leads initiated from the heel fillet similar to quad flat package assemblies.
- None of the PBGA 1156 I/Os and 256 I/Os with 1-mm pitch showed daisy chain failures to 500 thermal cycles under the three cycle conditions.
- The 2D x-ray system used in this investigation did not reveal the level of solder damage due to thermal cycling.
- Prior to x-sectioning, scanning electron microscopy (SEM) evaluation of the outer rows of PBGA 1156 I/O assembly revealed signs of fine microcracks in solder joints. Note that solder joints at the outer rows are exposed to less severe stress conditions compared to the joints at the die periphery in a PBGA assembly.
- After x-sectioning along package diagonal, SEM evaluation of PBGA 1156 I/O revealed signs of fine microcracks for the ball interconnections under the die. Damage for this thermally cycled PBGA was minimum.
- A summary of test data generated in collaboration with university and industry partners along with references to joint publications on these subjects were also presented.

8. NASA Application

This report covered qualification and verification steps and tools for high-input/output (I/O) and low-pitch plastic ball grid array (PBGA) packages as well as other active/passive parts assembled onto printed wiring boards (PWBs). Prior to design, it is recommended to review numerous industry standards on this subject including IPC 7095 and IPC 97xx (including 9701A) covering qualification approaches for thermal and mechanical characterizations. It is also recommended to review National Aeronautics and Space Administration (NASA) specifications, including NASA-STD-8739.3 (Soldered Electrical Connections) and NASA-STD-8739.2 (Workmanship Standards for Surface Mount Technology) and note applicable areas for quality, process controls, and solder. Applicable guideline documents for devices, as well as BGAs and CSPs published under the NASA Electronic Parts and Packaging (NEPP) Program (<http://nepp.nasa.gov>), should also be reviewed. Recommendations for NASA mission implementation are as follows:

- Ensure that all constraints on the use of plastic packages, including BGAs and CSPs are well understood.
 - ✓ Use hermetic seal packages such as CQFPs and CCGA, if possible.
 - ✓ No pure tin finish is allowed. Use of lead-free alloys shall be approved for applications.
 - ✓ Use hot air solder leveling (HASL) surface finish for PWB and avoid immersion gold on Ni or other exotic finishes.
- Define the overall NASA mission environmental requirements, including radiation, mechanical, thermal, life cycle, mechanical shock, vibration, etc.
- Define appropriate potential package technology and types, including ceramic packages, low and high PBGA, low-pitch CSP, flip chip, leaded package, and MLF. Review build up, materials, solder geometry and alloys, heat distribution, etc. using package supplier data and application notes.
- Determine if package properties are within the envelope of mission environmental requirements in order to avoid early overstress failures. Examples include radiation capability of die, temperature limits of package materials including softening temperature (glass transition temperature, T_g), and junction temperature. Determine if special handling, bake out, assembly process, and tools are required.
- For life thermal cycle qualification, determine life cycle requirements for mission. For the purpose of further narrowing package selection, consider the following four categories of NASA missions.
 - ✓ A: Benign thermal cycle exposure with short mission duration (e.g., Space Shuttle Missions)
 - ✓ B: Benign thermal cycles with long mission duration (International Space Station, Hubble Space Telescope, Mars Reconnaissance Orbiter [MRO], Grail, etc.)
 - ✓ C: Extreme thermal cycles with short mission duration (Mars Exploration Rover [MER], etc.)

- ✓ D: Extreme temperature cycle exposure with long mission duration (Next Generation Space Telescope [NGST], Mars Science Laboratory [MSL], etc.)
- If details on life cycle requirements are not available, then use the following rules-of-thumb to estimate the number of accelerated thermal cycles for NASA missions.
 - ✓ For A and B missions, thermal life cycle requirements are estimated to vary from 100 to 500 accelerated cycles in the range of -55°C to 100°C (NASA cycle).
 - ✓ For C and D missions, estimate the flight allowable temperature ranges and multiply mission cycles by 3. If mission cycle duration is short, add an additional 20 NASA cycles to include the cycle consumption for ground testing.
- Review heritage and package supplier's data for package- and second-level solder joint reliability. Use the following generic guidelines for meeting the requirements.
 - ✓ No flight heritage exists for high-I/O PBGA and low-pitch CSP packages even though contract manufacturers may have already implemented use of lower I/O PBGAs in their electronic systems. Generally, these categories of packages have been shown to have adequate thermal cycle resistance.
- High-I/O PBGAs with internal wire bond attachments meet most non-extreme NASA environmental requirements (A and B conditions). Use of PBGA requires additional part/die qualification and verification for application.
 - ✓ Flip-chip die PBGA packages were not evaluated in this investigation and shall be evaluated since they are commonly used in even higher I/O PBGAs and may not have adequate reliability.
- Use of CSP and flip-chip die direct attachment should be restricted and, only after careful review of vendor data and acceptability, be qualified for specific applications.
- Passives with 0603 and 0402 sizes can be assembled using conventional paste print deposition and reflow machines. Additional paste deposition evaluation is required for the extremely small 0201 passive.
- Passives construction shall be evaluated to ensure stability during reflow and also under extreme environmental exposure.
- MLF 36 and 72 I/O showed no significant issues during assembly. They showed however, various levels of voids especially for under package conductor solder attachment. Inspection for quality is difficult especially for smaller versions.
- TSOP assemblies showed low cycles-to-failure (CTF) data especially for packages with larger internal die. TSOP may have sufficient solder joint reliability under conditions A and B, but should be verified for use in conditions C and D.
- Use a daisy chain package as the test article for accelerated thermal cycle tests as specified in IPC 9701A. Daisy chain packages are generally built using similar materials and layup as the functional package with the exception of using a dummy die with even/odd pad connections. Die size affects solder joint reliability and, therefore, should be the same size or larger than the flight-like package.

- Design double-sided assembly if it mimics flight configuration. However, note that double-sided, mirror-image assemblies show major reduction in solder joint reliability.
- Optimize reflow thermal profile, especially for a mixed technology assembly. Remember that process optimization and process control are key parameters that control solder attachment integrity for area array packages, not optical/visual inspection, as commonly used for most other electronic packages at NASA. Refer to NASA standards for use of flux, solder paste quality test, and cleanliness requirements.
- Perform real time x-ray and optical inspection, if possible. Use of an x-ray machine with laminography capability is recommended.
 - ✓ The 2D x-ray system used in this investigation did not reveal the level of solder damage due to thermal cycling.
- Prior to x-sectioning, SEM evaluation of the outer rows of package assembly should be performed to reveal damage not detected by optical microscopy. X-section should be performed to reveal internal damage and crack formation.

In summary, it was shown that wire-bonded PBGA with 256 and 1156 I/Os, fully populated balls, and 1-mm pitch have acceptable thermal cycle reliability when using conventional tin-lead eutectic solder paste for their assembly. Thermal cycle reliability of other package assemblies, including flip chip die, ultra chip scale package (UCSP) with 0.4-mm pitch, two sizes of micro-lead frame (MLF), and two sizes of thin small outline packages (TSOP) varied. Passive chips with various sizes from 0603, 0402, and 0201 showed acceptable solder joint reliability. Difficulty was encountered in assembling 0201 resistors with no workmanship defects, however.

The key drawbacks of PBGA and fine-pitch array packages remain the same, i.e., inspection capability for interconnection integrity (cracks) and individual solder ball reworkability. In addition, most array packages are commercial-off-the-shelf (COTS) packages; they are required to be subjected to additional stringent screening with added cost at the package level prior to their acceptance for NASA applications.

9. Acronyms and Abbreviations

AAP	Area Array Packaging
BGA	Ball Grid Array
BoK	Body of Knowledge
CBGA	Ceramic Ball Grid Array
CCGA	Ceramic Column Grid Array
CGA	Column Grid Array
CEMA	Center for Electronics Manufacturing and Assembly
COB	Chip on Board
COTS	Commercial-off-the-shelf
CSP	Chip Scale (Size) Package
CTE	Coefficient of Thermal Expansion
CTF	Cycles to Failure
Cu	Copper
DCA	Direct Chip Attachment
DOE	Design of Experiment
EDX	Energy Dispersive X-ray
EMS	Engineering Manufacturing Service
ENIG	Electroless Nickel Immersion Gold
FCBGA	Flip Chip Ball Grid Array
FPBGA	Fine Pitch BGA, a.k.a. Chip Scale Package (CSP)
FC/DCA	Flip-Chip Direct Chip Attach
HASL	Hot-Air Solder Leveling
HDI	High Density Interconnect
I _{Ag}	Immersion Silver
IC	Integrated Circuit
Im _{Ag}	Immersion Silver
I/O	Input/Output
iNEMI	International Electronics Manufacturing Initiative
IPC	Association Connecting Electronics Industries
IR	Infrared
JPL	Jet Propulsion Laboratory
KGD	Known Good Die
LCCC	Leadless Ceramic Chip Carrier
MER	Mars Exploration Rovers
MIP	Mandatory Inspection Point
MLF	Microlead Frame
MRO	Mars Reconnaissance Orbiter
MSL	Mars Science Laboratory

NASA	National Aeronautics and Space Administration
NEPP	NASA Electronic Parts and Packaging
NGST	Next Generation Space Telescope
Ni	Nickel
NSMD	Non Solder Mask Defined
OSP	Organic Solder Preservative
PBGA	Plastic Ball Grid Array
PTH	Plated-Through Hole
PTHV	PTH Via
PWA	Printed Wiring Assembly
PWB	Printed Wiring Board
QA	Quality Assurance
QFN	Quad Flat No Lead
QFP	Quad Flat Pack
RIT	Rochester Institute of Technology
RT	Room Temperature
SAM	Scanning Acoustic Microscopy
SEM	Scanning Electron Microscopy
SIP	Systems in a Package
SMC	Surface Mount Components
SMD	Solder Mask Defined
SMT	Surface Mount Technology
TC	Thermal Cycle
TCE	Also CTE, Thermal Coefficient of Expansion
Tg	Glass Transition Temperature
TMA	Thermal Mechanical Analysis
TSOP	Thin Small Outline Package
TV	Test Vehicle
UCSP	Ultra Chip Scale Package
WLP	Wafer-Level Package

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