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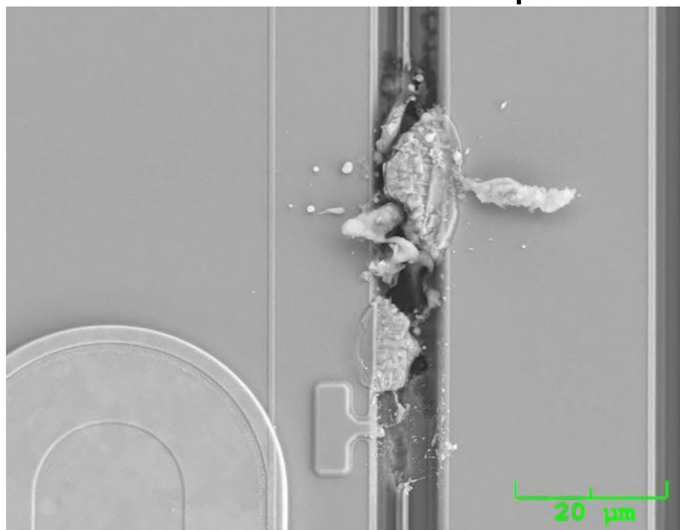
A Look at Failure: GaNFET Rupture



Testing a gallium nitride field-effect transistor (GaNFET) at the edge of the safe operating area results in rupture due to electrical overstress. JPL Failure Analysis Lab

Guidelines for Selection, Screening, and Qualification of Low-Voltage Commercial MLCCs for Space Programs

As EEE part commercial technology matures, establishing conditions necessary for insertion of new technologies into high-rel systems becomes more urgent. Commercial, low-voltage multilayer ceramic capacitors (MLCCs) manufactured using base metal electrode (BME) technology are currently at the stage where conditions of their use in military and space applications require serious attention. Analysis shows that the existing requirements for high quality ceramic capacitors for space (e.g., in MIL-PRF-123) can only provide a baseline, and they require substantial variations to accommodate the specifics of BME capacitors. These specifics are addressed in the recently published paper: "Guidelines for Selection, Screening and Qualification of Low-Voltage Commercial MLCCs," that is available at the NEPP web site:

https://nepp.nasa.gov/files/23923/Guidelines%20for%20selection%20of%20MLCCs%20rev.A.pdf

The guidelines include a brief description of failure mechanisms of BME MLCCs, recommendations for selection of part types, explanations of new requirements for construction analysis and destructive physical analysis (DPA), justification for additional lot acceptance and qualification testing, and requirements for assembly conditions specifically for manual soldering and rework. This document is open for discussions in the parts engineering community. For more information, contact

Alexander Teverovsky 301-286-6216

Flow-down of Derating Requirements

Derating requirements are generally required in contracts. They are intended to reduce the occurrence of stress-related failures and help assure long-term reliability of electronic components. Derating of electronic components provides a margin between the applied stress (electrical, radiation, mechanical, and thermal) and the actual capability of the part. However, it has been a practice for vendors to use their own derating policies, which may or may not be comparable to the derating policy flowed down by the contract. Therefore, precautions must be taken to ensure that acceptable derating factors are used in the design of the contracted products.

One should conduct a general comparison of the derating policy flowed down by the contract against the vendor's derating policy. The primary goal is to identify part types not addressed by the vendor's derating policy. The Jet Propulsion Laboratory (JPL) recently performed a comparison of its internal derating policy against a vendor's derating policy (MIL-STD-975M) and found that MIL-STD-975M did not provide derating factors for several part types including RF/microwave and stacked capacitors. The risk is that these parts may be part of the delivered product with no derating having been used (if MIL-STD-975M was followed).

MIL-STD-975M was cancelled without replacement on May 3, 1998. So, why do vendors continue to use Mil-Std-975M as their derating policy? One common answer is flight pedigree of a product design. Many product designs originated when Mil-Std-975M was widely used and still active, so all reliability analyses

were conducted using the derating factors of that standard. Therefore, the motivation to produce reliability analysis using the contract's derating policy is not high. Vendors often presume that MIL-STD-975M will be accepted as a comparable derating policy.

ECSS-Q-ST-30-11C, published by the European Cooperation for Space Standardization (ECSS), is a standard to be used for derating of electronic components. ECSS is a cooperative effort of the European Space Agency (ESA), national space agencies, and European industry associations. Unlike MIL-STD-975M, this derating policy does include recent technologies.

A comparison of policies often reveals that derating policies utilized by vendors and contractors are often less stringent. For example, in a comparison of ECSS-Q-ST-30-11C against JPL's internal derating policy, the temperature derating factor for power diodes in the ESA specification is less stringent and requires more investigation. One should consult with the parts engineering and reliability engineering personnel in your organization before accepting the vendor's derating policy as comparable to your own derating policy. Also consider design and vendor flight history, results of parts stress analysis and parts list review, application and environment, and findings of comparison assessments.

This article was provided by Elvis Merida of JPL. For more information, contact

Mark White at 818-393-4173

Xilinx Discontinues CGA Package on V4/V5

Xilinx will discontinue offering column grid arrays (CGAs) on the Virtex-4 and Virtex-5 FPGA QV ceramic flip chip, and they will offer them only in land grid arrays (LGAs) (without columns). The new package and assembly supplier are being qualified. See Xilinx XCN13005 for more details, including last time buy information. http://www.xilinx.com/support/documentation/customer_notices/xcn13005.pdf

For more information, contact

Doug Sheldon at 818-393-5113

Non-Hermetics in Space (Class Y)

The Class Y Task Group meeting was held in January 2013. A draft of 38535K with added Class Y requirements and other updates has been released. Comments were due by February 21, with a coordination meeting planned in April.

For more information, contact

Shri Agarwal at 818-354-5598

Static Burn-in and Electrical Test Circuits

Variation abounds in the way manufacturers implement static testing due to the lack of requirements in MIL-STD-883.

(i) Single circuit used with half of the inputs biased low and the other half biased high

Post static burn-in electricals done.

(ii) Two Circuits used.

All inputs low (Static I)

All inputs high (Static II)

Post static burn-in electricals done **after completion of both** (Static I and Static II) burn-ins.

(iii) Two circuits used.

All inputs low (Static I)

All inputs high (Static II)

Post static burn-in electricals done **after completion of each** static burn-in.

The JC13 Task Group has been asked to review and provide guidance, as well as clarify whether inputs refer to data, control, address, or clock.

For more information, contact

Shri Agarwal at 818-354-5598

Quality Leadership Forum 2013

In support of the NASA Office of Safety and Mission Assurance (OSMA), the Quality Leadership Forum (QLF) was coordinated by JPL's Assurance Technology Program Office and took place at the Radisson at the Port in Cape Canaveral, Florida on March 20 and 21, 2013. An excellent mix of presenters from the aerospace industry, NASA, and other governmental agencies were on hand to deliver topics ranging from lessons learned to quality best practices and industry quality issues. The number of attendees was approximately 175. The documentary film recently released by JPL, "The Changing Face of Mars," was exhibited at the KSC visitor complex to QLF attendees. In addition, the JPL-developed Counterfeit Parts Awareness training was provided by Lori Risse and Carlos Abesamis in conjunction with the forum.

For more information, contact

Diana Shellman at 818-393-0745

GIDEP Alerts/Advisories

Contact your GIDEP Representative for a copy of:

Suspect Coun-terfeit	D8Y-A-13-01 Network Processor; D8Y-A-13-02 Flash Memory; D8Y-A-13-03 SMBUS Temp Sensor D8Y-A-13-04 Small Switching Transistor; D8Y-A-13-05 Zener Diode. Q9-A-13-01 Graphics Chip; CBP-A-13-01 Connector, Cover, Fiber Optic
Misc.	H6-A-13-01 Hybrid, Power MOSFET Optocoupler, Open Circuit Failures; CET-P-13-01 Microcircuit, Hybrid, Digital, Multichip, Dual Channel, Driver-Receiver; M9-P-13-01 Failure to comply to specification requirements/ITAR requirements; VV-P-13-01 Internal Gas Analysis for Ammonia; BUP-A-13-01 Microcircuit, Dual Precision Monostable Multivibrator; GB4-P-13-01A Microcircuit, Digital, Rad Hard, Low Voltage CMOS, Minimum Skew One-to-eight Clock Driver; GB4-P-13-02 Microcircuit, Digital, CMOS, Rad Hard, 32-bit Fault-tolerant Processor, Monolithic Silicon

Reduced Schedule of Meetings

(Communication from DLA)

Due to "sequestration" and other budgetary negotiations in Congress and the associated contingency planning at DLA due to these negotiations, all travel that can be deferred will be deferred indefinitely. The publishing of the audit schedule will also be suspended during this time. For the rare exceptions to the travel deferment, you should hear from the responsible engineer/technician or Branch Chief directly. If you have any questions, please direct them to Joe Gemperline, (614) 692-0663, or Joseph.Gemperline@dla.mil.

NASA Parts Specialists Recent Support for DLA Land and Maritime Audits:

Audit performed at IRC, Corpus Christi, TX

One audit is scheduled at Crane Electronics, Redmond, WA

Upcoming Meetings

- Single Event Effects Symposium and Military and Aerospace Programmable Logic Devices Conference, La Jolla, CA, April 9–12, 2013 http://radhome.gsfc.nasa.gov/radhome/see_mapld/
- NEPP Electronics Technology Workshop, NASA-GSFC, Greenbelt, MD, June 10–13, 2013

Contacts

NEPAG
http://atpo.jpl.nasa.gov/nepag/index.html

Shri Agarwal 818-354-5598
Shri.g.agarwal@jpl.nasa.gov
Lori Risse 818-354-5131
Lori.a.risse@jpl.nasa.gov

ATPO http://atpo.jpl.nasa.gov
Chuck Barnes 818-354-4467
Charles.e.barnes@jpl.nasa.gov

JPL Electronic Parts http://parts.jpl.nasa.gov
Rob Menke 818-393-7780
Robert.j.menke@jpl.nasa.gov

Previous Issues:
JPL: http://atpo/nepag/index.html
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Public Link (best with Internet Explorer):
http://trs-new.jpl.nasa.gov/dspace/handle/2014/41402

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