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Gallium Nitride – Worth the Hype?

Gallium nitride (GaN) is a wide band gap (WBG) semiconductor with some properties well ahead of silicon for applications where speed and power are desired. A cursory review of Table I reveals that GaN has a numerical advantage in both managing electric fields (due to the higher band gap energy and critical electric field) and device speed (due to higher drift velocity). A typical polytype of silicon carbide (SiC), the other contender for power management and distribution (PMAD), is shown for comparison. The salmon cells in Table I highlight each technology's strong points for power applications.

Table I. Comparison of power semiconductor material properties. Numbers in the table are approximate.

Property	Si	GaN	3C-SiC
Bandgap, Eg (eV at 300 K)	1.12	3.4	2.4
Critical electric field, Ec (V/cm)	2.5×10^5	3×10^6	2×10^6
Thermal conductivity, (W/cmK at 300 K)	1.5	1.3	3–4
Saturated electron drift velocity, vsat (cm/s)	1×10^7	2.5×10^7	2.5×10^7
Electron Mobility, ìn (cm^2/Vs)	1350	1000*	1000
Hole Mobility, ìp (cm^2/Vs)	480	30	40
Dielectric constant	11.9	9.5	9.7

*** Greater than 1500 cm^2/Vs has been seen in 2DEG**

The advantage of GaN is more readily shown in a figure of merit (FOM) graph (Figure 1). An ideal device for PMAD applications would be at the highest breakdown voltage, i.e., toward the right side of the graph, and the lowest FOM, which is the product of resistance of the device when on and the charge needed to invert the gate or base of the device. The theoretical limit of GaN resides significantly closer to the optimal application area. Despite these encouraging numbers, GaN does lag behind silicon in the area of thermal conductivity. This aspect of GaN will present a design challenge in any device architecture.

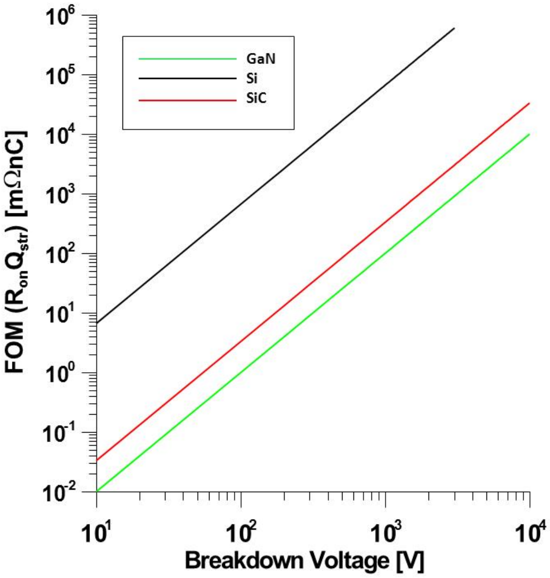

Figure 1. Theoretical limiting FOM of various PMAD technologies. Commercial silicon devices operate at their respective limit, while first-generation GaN devices are surpassing silicon.

So far, despite their advantages, GaN transistors have been hard to productize into a workable alternative to silicon PMAD solutions. One main reason for this lag has been the challenges in producing high quality substrates suitable for a GaN epitaxial (Epi) with controllable and repeatable properties. Unlike other technologies, GaN power devices are typically deposited on non-native substrates, typically Si or SiC. These challenges have recently been overcome sufficiently for commercialization, and devices are now industrially available. Cree, EPC, RFMD, and Sumitomo are some of the manufacturers providing commercially available GaN transistors. In all of the options from the aforementioned manufacturers, the architecture is a lateral high electron mobility transistor (HEMT). Figure 2 presents a typical HEMT structure in a field-effect transistor (FET) where the conduction between the source and drain of the device occurs in a two-dimensional electron gas (2DEG) and is controlled by the gate bias. Note that electron mobility is much higher in the 2DEG architecture of GaN. This design is easier to fabricate using a silicon substrate to reduce cost. This GaN HEMT design is very small, will be very fast, and can support current of the same magnitude as silicon power devices of comparable specification. However, some drawbacks have become evident. The nature of the HEMT structure results in a “normally on” operation, which is atypical for PMAD applications, but EPC has developed a “normally off” version of the HEMT called eGaN. Also, the gate junction in the HEMT device is very sensitive to breakdown, and therefore, voltage overstress of the gate is a serious reliability consideration. The failure in time (FIT) estimates of GaN devices are only starting to be studied as well as the thermal and wear-out effects on device lifetime.

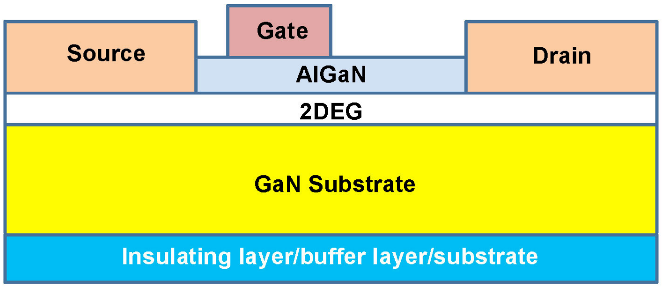

Figure 2. HEMT structure typical of a GaN FET.

To fully realize the switching power of GaN, a vertical device architecture would be a considerable step forward. These would be smaller, and they would have lower parasitic inductance, higher blocking voltage, and better thermal properties. These devices would be necessarily more complex than lateral devices; however, prototypical devices have been demonstrated. Further advancement to GaN FETs could be realized if gate isolation were introduced commercially, but it would have the added complexity of an additional layer at the gate with lattice mismatch, traps, and the potential to charge. At this time, GaN has no native dielectric to provide gate isolation.

Because of the mass, power, and speed advantages of GaN technologies, there is increasing interest in using GaN for designing high-efficiency, low-mass power supplies for space missions. Current GaN devices have shown promising radiation hardness, and future designs should have at least the hardening potential of silicon. The aforementioned reliability issues have been assessed as presenting a diminishing risk to most space applications.

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- NEPP Workshop (ETW) http://www.nepp.nasa.gov/workshops/etw2012; NASA/GSFC June 11–13, 2012
- Nuclear and Space Radiation Effects Conference (NSREC) http://www.nsrec.com; Miami, FL, July 16–20, 2012

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